2002

An analog OP-amp IP-core using 0.18 micrometer CMOS technology.

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An Analog Op-Amp IP-Core Using 0.18 Micrometer CMOS Technology

by

Zhengyu Liu

A Thesis

Submitted to the Faculty of Graduate Studies and Research

through the Department of Electrical and Computer Engineering

in Partial Fulfillment of the Requirements for

the Degree of Master of Applied Science at the

University of Windsor

Windsor, Ontario, Canada

September, 2002

To my mother for her constant encouragement,
my wife for her support and my son Byron.

Abstract

This thesis presents a new design for a 0.18μm CMOS analog Operational Amplifier. The most difficult design challenge for a low-voltage operationai amplifier is the design of a rail-to-rail input differential amplifier stage with a constant transconductance (g_m).

The main contribution in this thesis is the novel design methodology of a DC level shifter that enables the synthesis of a 0.18μm CMOS analog operational amplifier with a constant-g_m implementation over a common-mode voltage range from 0 to 1.8V.

The design of a 0.18μm CMOS low-voltage operational amplifier with constant overall transconductance g_m, which allows for a rail-to-rail input swing without degrading the common-mode rejection ratio (CMRR) or causing the slew rate to vary, is developed in this thesis. The DC level shifter circuit design methodology optimizes all the transistors of the DC level shifter to improve the overlapping of p-pair and n-pair tail currents.

The 1.8V CMOS operational amplifier has power consumption less than 178μw, a CMRR of 123.6 dB and a slew rate of 4V/μs. A total of 32 transistors were used in the final layout.

The purpose of this design is to build the operational amplifier as an Intellectual Property (IP) core suitable for System-on-Chip (SOC) implementation. This IP core can be repeatedly used in future designs and should also be able to easily inserted into any vendor technology or design methodology.

Acknowledgments

There are many people who have influenced me by providing technical advice, financial help and moral support for this thesis.

I would like to express my sincere appreciation and gratitude to Dr. W.C. Miller, my supervisor, for his constant support and guidance throughout the progress of this thesis. I would also like to thank my committee members Dr. Majid Ahmadi and Dr. Edwin Tam, for their invaluable advice during and after my seminars to improve many aspects of my project.

I would like to thank all of my peers at the RCIM Research Center for all the happy times we spent together during my work on this thesis in the University of Windsor.

Finally I would like to recognize CMC for providing and supporting the design software which made all the essential simulations of my project possible.

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Chapter 1

Introduction

1.1 The Need of CMOS Analog Op-Amp

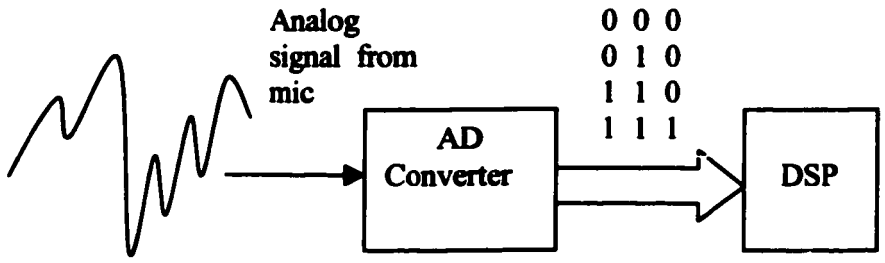
The term operational amplifier, abbreviated op-amp, was created in the 1940s to refer to a special kind of amplifier that, by proper selection of external components, can be configured to perform a variety of mathematical operations [9]. Early op-amps were made from vacuum tubes consuming lots of space and energy. Later op-amps were made smaller by implementing them with discrete transistors. Today, op-amps are monolithic integrated circuits, highly efficient and cost effective.

The need for analog circuits that can operate with low power-supply voltage has increased in recent years. For example, a high–quality microphone picking up the sound of human speech generates a signal which amplitude may vary from a few micro-volts to hundreds of milli-volts. In this application it is very difficult or even impossible to replace analog functions with their digital counterparts regardless of advances of technology.

In practice, the electrical version of natural signals coming from microphone may be too small for direct digitization by the AD

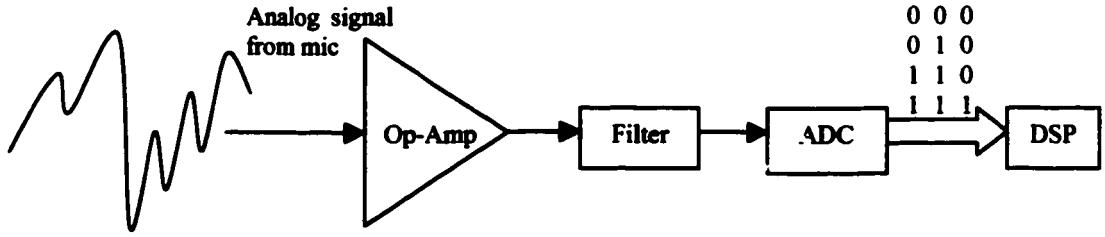
converter. Also, the signals are often accompanied by unwanted, out-of-band noises or interferers, as shown in Figure 1.1.

Figure 1.1 Difficult to Direct Digitize the Natural Signals



However, an op-amp can boost the signal level and an analog filter can suppress the out-of-band components, as in Figure 1.2 [23].

Figure 1.2 Addition of Amplification and Filtering for Higher Sensitivity



Therefore, the design of high-performance, low-power CMOS analog operational amplifiers is one of the hottest active researches today.

The increasing demand for these op-amps is also driven by smaller and smaller

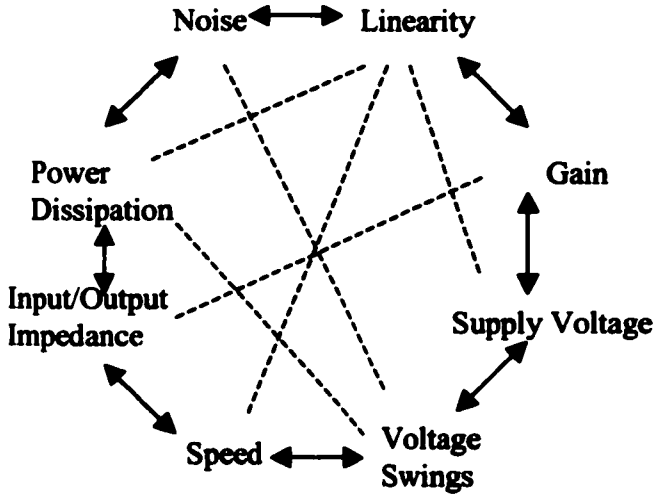
submicron technologies as well as the exploding market for portable, battery-operated electronic systems such as cellular phones, lap-top computers and camcorders, etc. Smaller dimensions require lower supply voltages to prevent high electronic fields which can cause devices to breakdown and degrade the reliability.

Portable electronics devices require low voltage power supply because it translates to fewer batteries which can minimizes the size and weight of such devices. Unlike digital circuits in which power consumption reduces proportional to the square of the supply voltage, operational amplifiers actually increase power consumption at lower voltage when performance is held constant [5]. Thus, the goal of this thesis is to tackle these challenges and design a robust rail-to-rail input and output low voltage and low power operational amplifier using a standard CMOS process.

1.2 Design Parameters of Op-Amp

The op-amp is a fundamental building block in analog CMOS integrated circuit design. We can define an op-amp as a "high-gain differential amplifier". Parameters in Figure 1.3 trade-off with each other, making the op-amp design a multi-dimensional optimization problem [23].

Figure 1.3 Analog Design Parameters

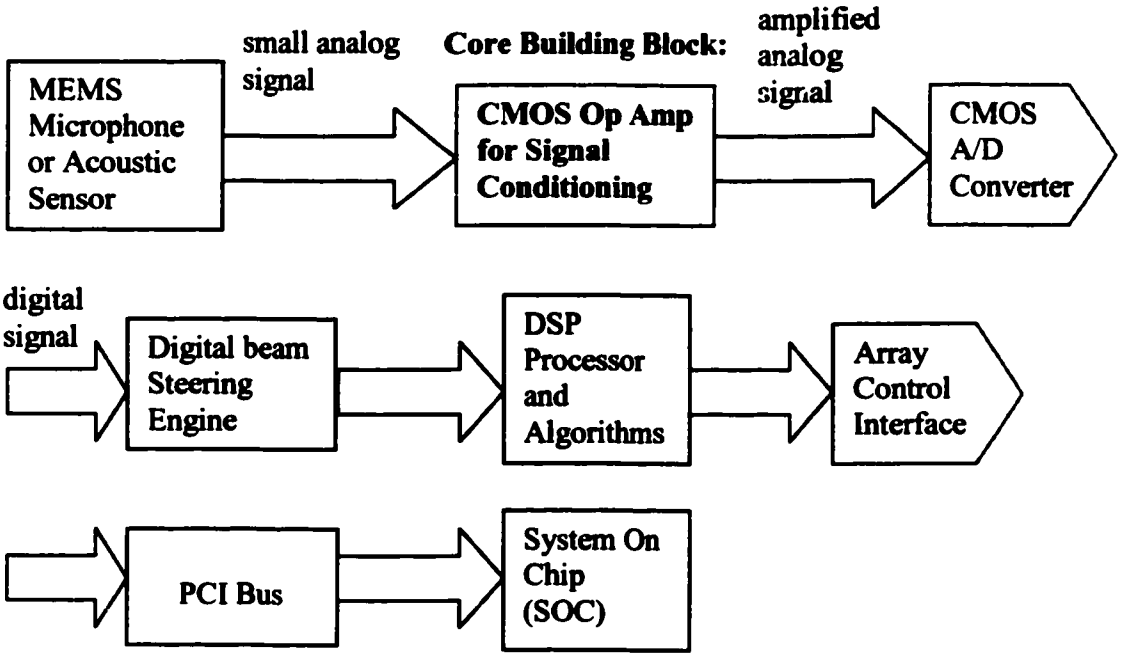


Such trade-offs present many challenges in the design of high-performance op-amps, requiring intuition and experience to reach an acceptable design. Therefore, the op-amp design problem can be expressed as a special form of optimization problem called geometric programming [20].

1.3 Building Blocks

Figure 1.4 shows the signal flow of the audible voice, which is picked up by a MEMS microphone or acoustic sensor. From these building blocks we can find that the core building block is the CMOS op-amp for signal conditioning. Without this analog signal conditioning, it is impossible for the analog signal to be converted to the digital one and then do the digital signal processing.

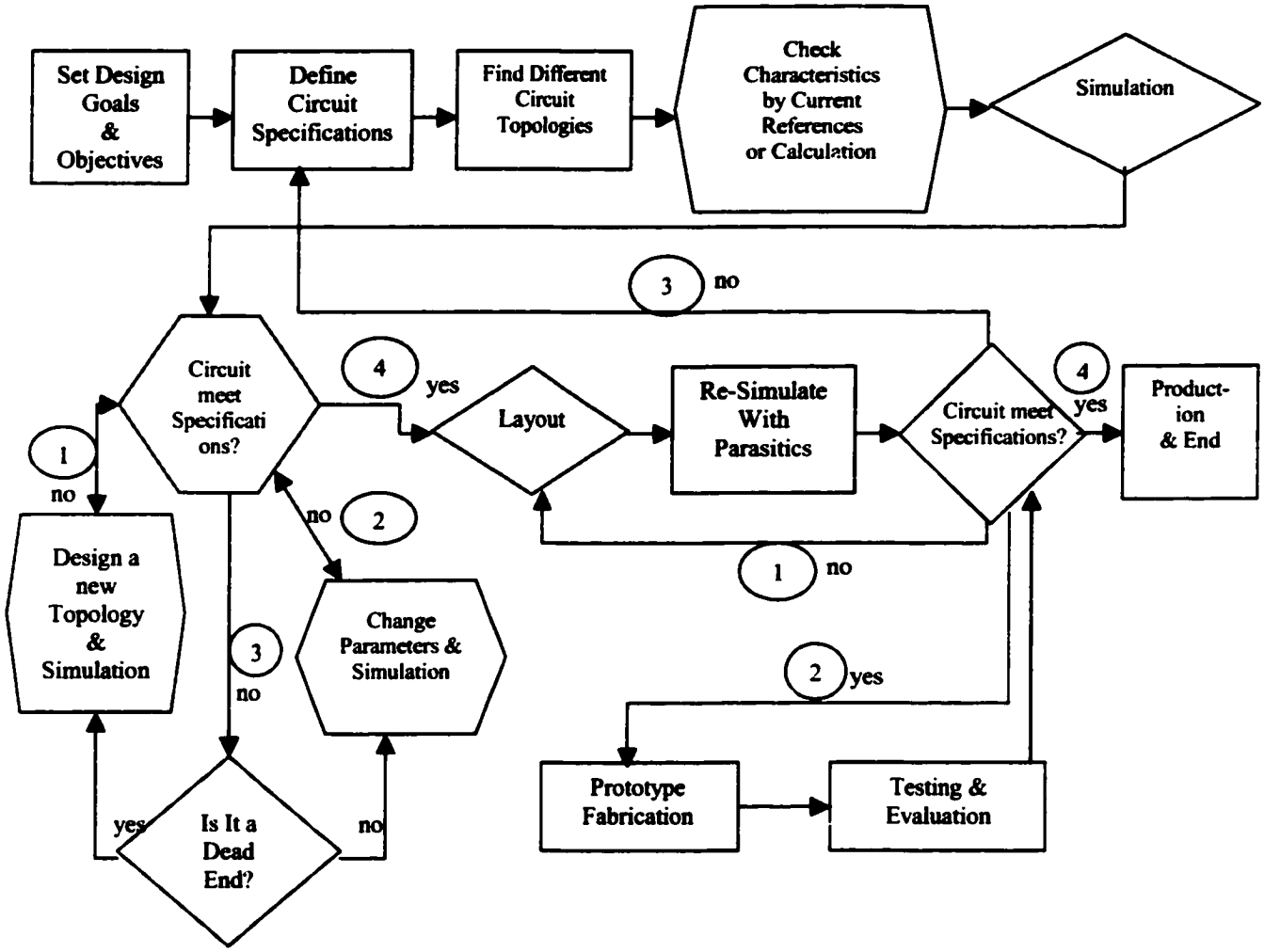
Figure 1.4 Building Blocks



1.4 CMOS Analog Op-Amp Design Flow

Figure 1.5 shows the typical diagrams of the 0.18μm CMOS op-amp design, simulation, test, verification, layout and fabrication sequences [7].

Figure 1.5 CMOS Analog Op Amp Design Flow:



Finding different circuit topologies which can meet our specifications is usually the primary step and most time consuming. However, by choosing a most suitable circuit topology for our design, much more time and effort can be saved later on in our simulation and verification.

1.5 Thesis Objectives

The work presented in this thesis has the main purpose of using 0.18μm CMOS technology to achieve a low voltage, low power rail-to-rail input and output operational amplifier, with constant total transconductance g_m [15][16]. This proposed op-amp should be able to build into an IP (intellectual property) core. An IP core is a block of logic or data that is used in making an application-specific integrated circuit (ASIC) for a product. As essential elements of design reuse, IP cores are part of the growing electronic design automation (EDA) industry trend towards repeated use of previously designed components in system-on-chip (SOC) implementation. One objective of this thesis is to build our own IP core; it should be entirely portable, be able to easily inserted into any vendor technology or design methodology.

SOC design is a complex IC that integrates the major functional elements of a complete end-product into a single chip or chipset [6]. In general, SOC design incorporates a programmable processor, on-chip memory, and accelerating function units implemented in hardware. Another objective of this thesis is to implement the designed op-amp in the system-on-chip (SOC) environment.

1.6 Thesis Organization

The organization of this thesis begins with the introduction (Chapter1) which indicates the basic need of analog op-amp, trade-offs between design parameters as well as the design flow; followed by Chapter 2, which covers different design approaches and proposed design specifications. Chapter 3 introduces design algorithms and the basic idea of rail-to-rail common-mode input range. Chapter 4 explains how to use DC level shifter to overlap transition regions in order to get constant-g_m. Chapter 5 examines the different stages of the op-amp and their frequency responses. Chapter 6 explains the simulation results of the total schematic and final layout. Chapter 7 concludes this thesis, clearly indicates the contributions of this thesis and suggestions for future work.

Chapter 2

CMOS Op-Amp Design Approaches

2.1 Design Approach

The design process of CMOS op-amp usually involves two distinct activities:

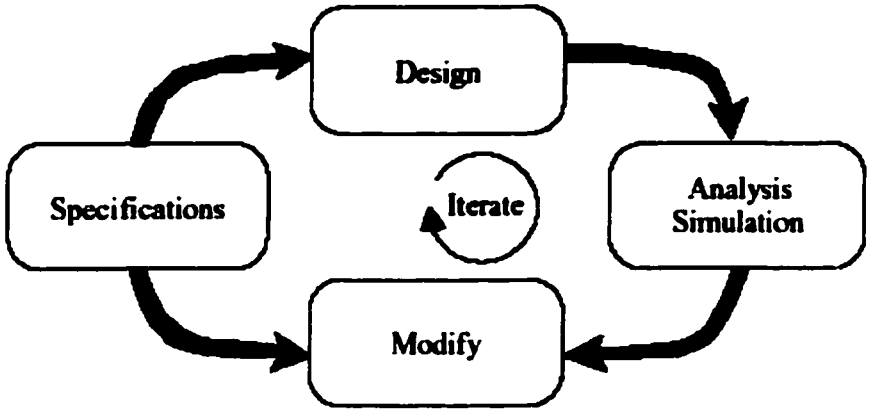
1. Architecture Design:
   - Find an architecture which already available and adapt it to present requirements
   - Create a new architecture that can meet our requirements

2. Component Design:
   - Design transistor sizes
   - Design compensation network

If available architectures selected do not meet our requirements, then an existing architecture must be modified, or a new circuitry has to be designed. Once a satisfactory circuit topology has been obtained, then the devices and compensation network must also be designed. All design approaches have been done repeatedly as many as hundred times in this thesis in order to meet all of the

design specifications. Figure 2.1 shows the flow chart of design approaches [4].

Figure 2.1 Iterated Design Approach



The most common design specifications of analog CMOS op-amp are listed below:

- Gain
- Output voltage swing
- Settling time
- Power dissipation
- Supply voltage
- Silicon area
- Bandwidth
- PSRR
- CMRR
- Noise
- Common-mode input range
- Slew Rate

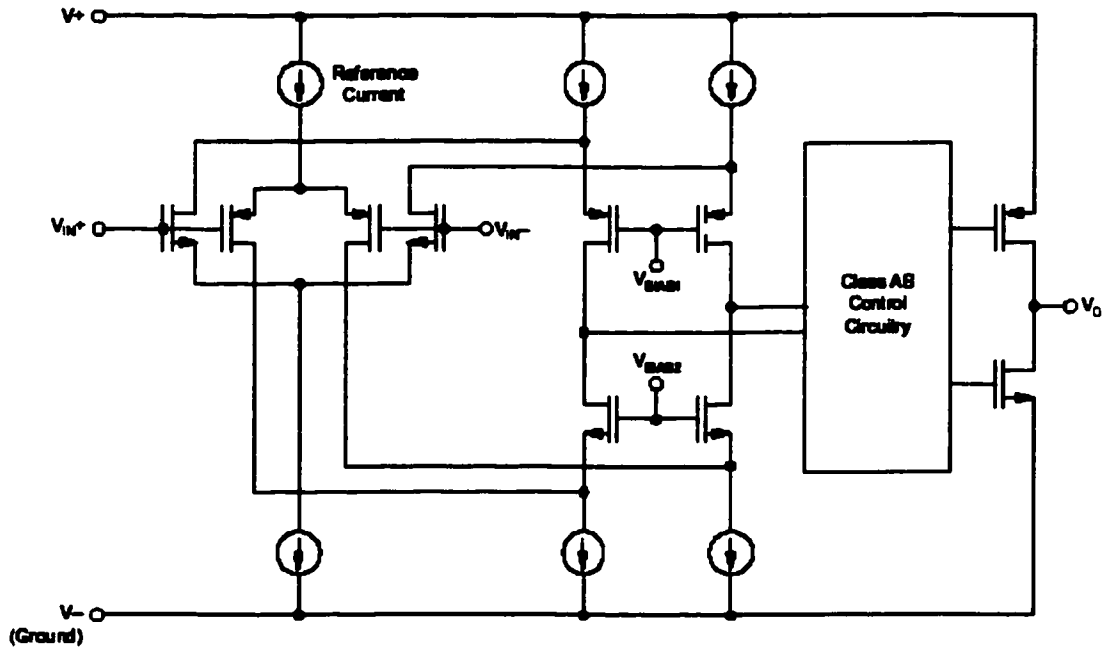
A design approach can be started from a design specification and system level model all the way through to physical layout. When we have completed all the design and verification steps, we should have a stream file to describe the mask layer information of our circuit.

2.2 Rail-to-Rail Input /Second /Output Stage

Rail-to-Rail Input Stage: The symmetry of the input stage is the key to its operation.

Each transistor pair should be matched as closely as possible. The OPA354 series of high-speed, voltage-feedback CMOS Op-Amps are developed by Texas Instruments for video and other applications requiring wide bandwidth [8]. The specified input common-mode voltage range of these series extends 100mV beyond the supply rails. This is achieved with a complementary input stage — an *N*-channel input differential pair in parallel with a *P*-channel differential pair, as shown in Figure 2.2. The *N*-channel pair is active for input voltages close to the positive rail, typically (V+) – 1.2V to 100mV above the positive supply, while the *P*-channel pair is on for inputs from 100mV below the negative supply to approximately (V+) – 1.2V. There is a small transition region, typically (V+) – 1.5V to (V+) – 0.9V, in which both pairs are on. This 600mV transition region can vary 500mV with process variation. Thus, the transition region (both input stages on) can range from (V+) – 2.0V to (V+) – 1.5V on the low end, up to (V+) – 0.9V to (V+) – 0.4V on the high end. A double-folded cascode adds the signal from the two input pairs and presents a differential signal to the class A-B output stage.

Figure 2.2 Simplified Schematic of OPA354 by Texas Instrument



Second Stage: The second stage converts output current of first stage I_{out1} into a voltage and provides frequency compensation. The second stage is a trans-resistance amplifier. There should be a capacitor, Cc, in the second stage to provide internal frequency compensation. It causes the gain to roll off as the frequency increases. Without Cc, external compensation is required to prevent the op-amp from oscillating in most applications.

Rail-to-Rail Output Stage: A class A-B, push-pull output stage with common-source transistors is used to achieve rail-to-rail output. For high-impedance loads (> 200Ω), the output voltage swing is typically 100mV from the supply rails. With 10Ω loads, a useful output swing can be achieved while maintaining high open-loop gain. The output stage provides current drive for the output load, with unit voltage gain. The output stage is a current amplifier.

2.3 Op-Amp Design Specifications

Selecting the right operational amplifier for a specific application requires us to have our design goals clearly in mind along with a firm understanding of what the published specifications mean. Table 2.1 shows the proposed design specifications set for this thesis.

Table 2.1 Proposed Op-Amp Design Specifications

Power Supply: 1.8V

Performance Parameters	Design Goals
Output Swing	rail to rail
Total power	<200μW
0.1% setting time	<150ns
Slew rate	>2V/μs
Voltage gain (DC)	>10K (80dB)
Gain bandwidth	≥10kHz
CMRR	>90 dB
Total Harmonic Distortion (THD)	<0.1%
Op-amp die area (core area)	<0.1mm^2

- **Input Common Mode Voltage Range**

Normally there is a voltage that is common to the inputs of the op-amp. If this common mode voltage gets too high or too low, the inputs will shut down and proper operation ceases. The common mode input voltage range specifies the range over which normal operation is guaranteed.

- **Input Offset Voltage**

Input offset voltage, V_{IO}, is defined as "the DC voltage that must be applied between the input terminals to force the quiescent DC output voltage to zero or some other level, if specified". If the input stage was perfectly symmetrical and the transistors were perfectly matched, $V_{IO} = 0$. Because of process variations, geometry and doping are never exact to the last detail, all op-amps require a small voltage between their inverting and non

inverting inputs to balance the mismatches.

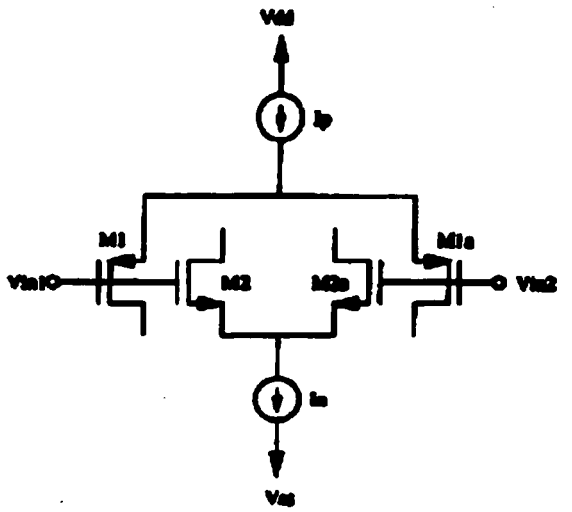
2.4 Obtaining Constant-g_m Rail-to-Rail Input Stage By Using Current Mirrors

Following design presents one of the methods to achieve the constant- g_m rail-to-rail input stage. Although this design is different from my way of design and simulation expressed in later chapters, the basic principle is same and it is also a good approach to explain how and why the constant-g_m is achieved.

Why a rail-to-rail input stage is needed?

In order to obtain a reasonable signal-to-noise ratio in low-voltage op-amp design, the input stage should be able to deal with common-mode input voltages from positive supply rail to negative supply rail. To achieve this, a complimentary *N*-channel and *P*-channel differential input pair in parallel is presented [13] in Figure 2.3

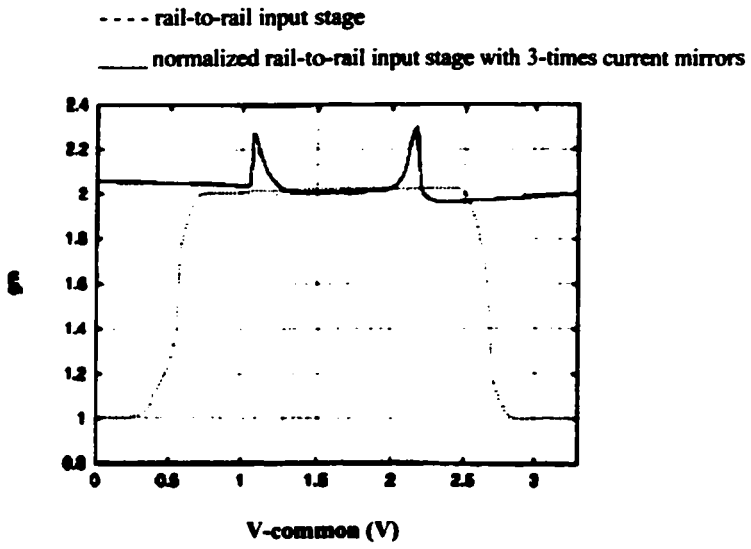
Figure 2.3 Schematic of a Complimentary Rail-to-Rail Input Stage



The *P*-channel input pair, M1-M1a, is able to reach the negative supply rail while the *N*-channel input pair, M2-M2a, is able to reach the positive supply rail.

However, a drawback of the rail-to-rail input stage is that its total trans-conductance g_m varies by a factor of "2" over the common-mode input range [1][2], as shown in Figure 2.4

Figure 2.4 Normalized g_m vs. Common-Mode Input Voltage



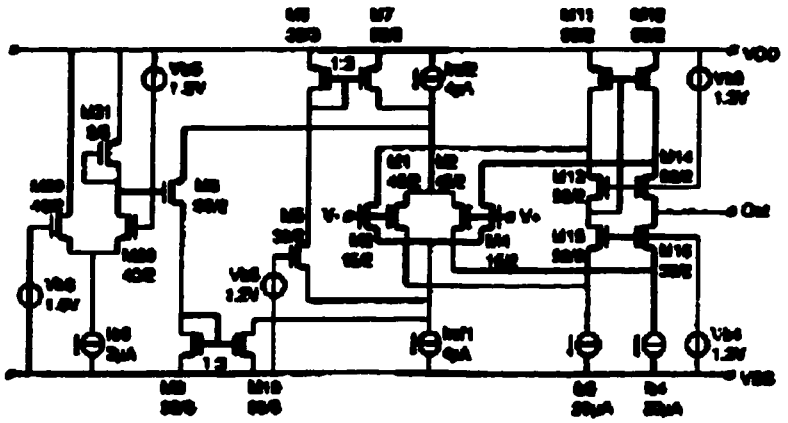
Why a constant-g_m is needed?

The variable g_m results in a variable unity-gain frequency, degrades the common-mode rejection ratio (CMRR) and causes the slew rate to vary. Therefore, to obtain a constant-g_m while keeping the rail-to-rail input swing is the key feature in my entire thesis.

From the dashed line of Figure 2.4 we can find, the g_m at the upper and lower part of the common-mode input range has to be increase by a factor of "2", in order to obtain a constant g_m over the whole common-mode input range. Due to the fact that total trans-conductance g_m of a CMOS transistor operating in strong inversion is proportional to the square-root of its drain current, the tail current of the input pair should be increased by a

factor of "4". This goal is realized in following circuit which g_m is controlled by three-times current mirrors, see Figure 2.5

Figure 2.5 Rail-to-Rail Input Stage With g_m Controlled By Three-Times Current Mirrors



Here is how the tail current Iref1 or Iref2 is increased by four times at the lower and upper part of the common-mode input range [1]:

When applying high common-mode input voltages, only the *N*-channel input pair is on. The *P*-channel current switch conducts while the *N*-channel current switch is off. The *P*-channel current switch takes away the current Iref2 and feeds it into the current mirror, *M9-M10*, where it is multiplied by a factor of 3 and added to the current Iref1. Because the *N*-pair and *P*-pair are perfectly match, Iref1= Iref2, so the tail-current of the N-channel input pair equals to 4Iref.

The same theory comes to *P*-channel when the low common-mode input voltages are applied. However the situation will be different when intermediate common-mode input voltages are applied.

When intermediate level common-mode input voltages are used, both *P*-pair and *N*-pair are on and both current switches are off. This result in the tail currents of both *N*-channel and *P*-channel input pairs are equal to Iref. By this way a constant g_m is obtained in full common-mode input range, as the solid line shown in Figure 2.4.

Chapter 3

Design Algorithm

3.1 Introduction

A novel method of achieving constant-g_m by overlapping transition regions is designed in this chapter. It is substantially different from the design approach of Section 2.4, in which the constant-g_m input stage was obtained by using current mirrors.

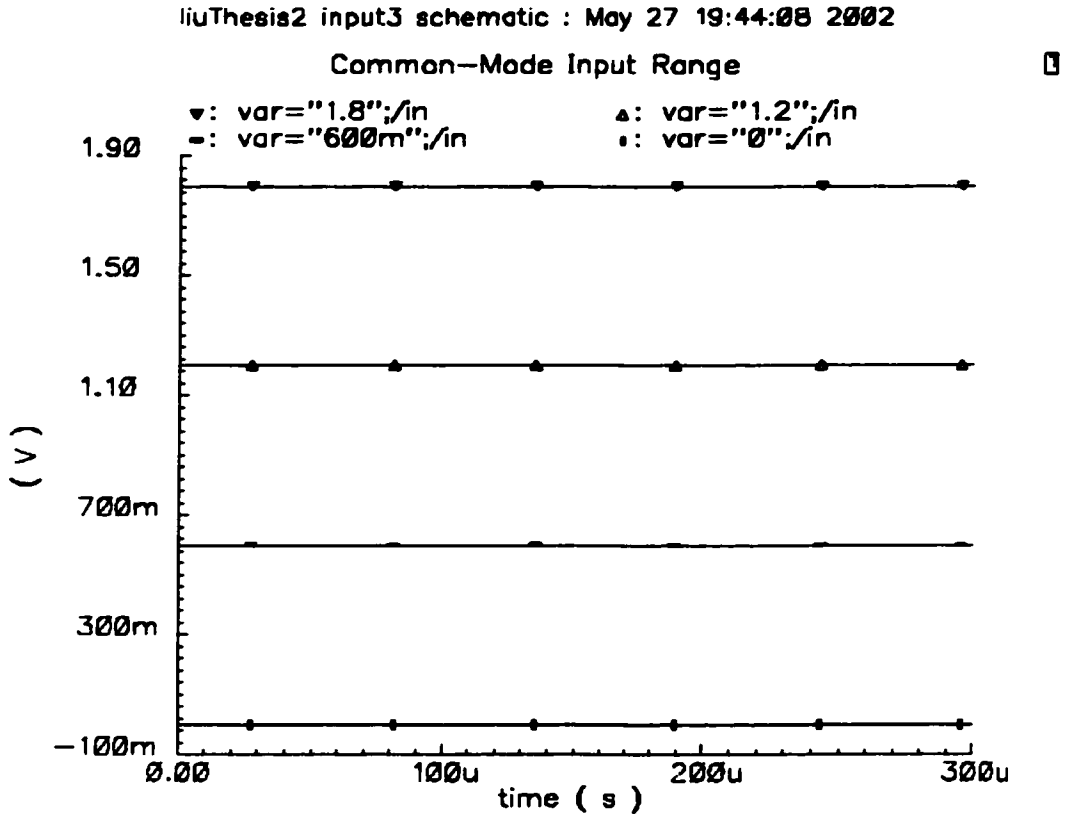
The technique used in Section 2.4 to achieve a constant-g_m rail-to-rail complementary *N-P* differential input stage requires complex additional circuitry as well as more chip area and power consumption [11]. In addition, the frequency response and common-mode rejection ratio (CMRR) are degraded. However, the proposed design in this chapter strategically overlaps the transition regions of the tail currents for the *N*- and *P*-pairs to achieve constant overall transconductance g_m.

3.2 Rail-to-Rail Common-Mode Input Range

The rail-to-rail common-mode input range denotes the common-

mode input signals can vary from the negative to positive supply rails by using the complementary differential pairs, see the following Figure 3.1

Figure 3.1 Common-Mode Input Range

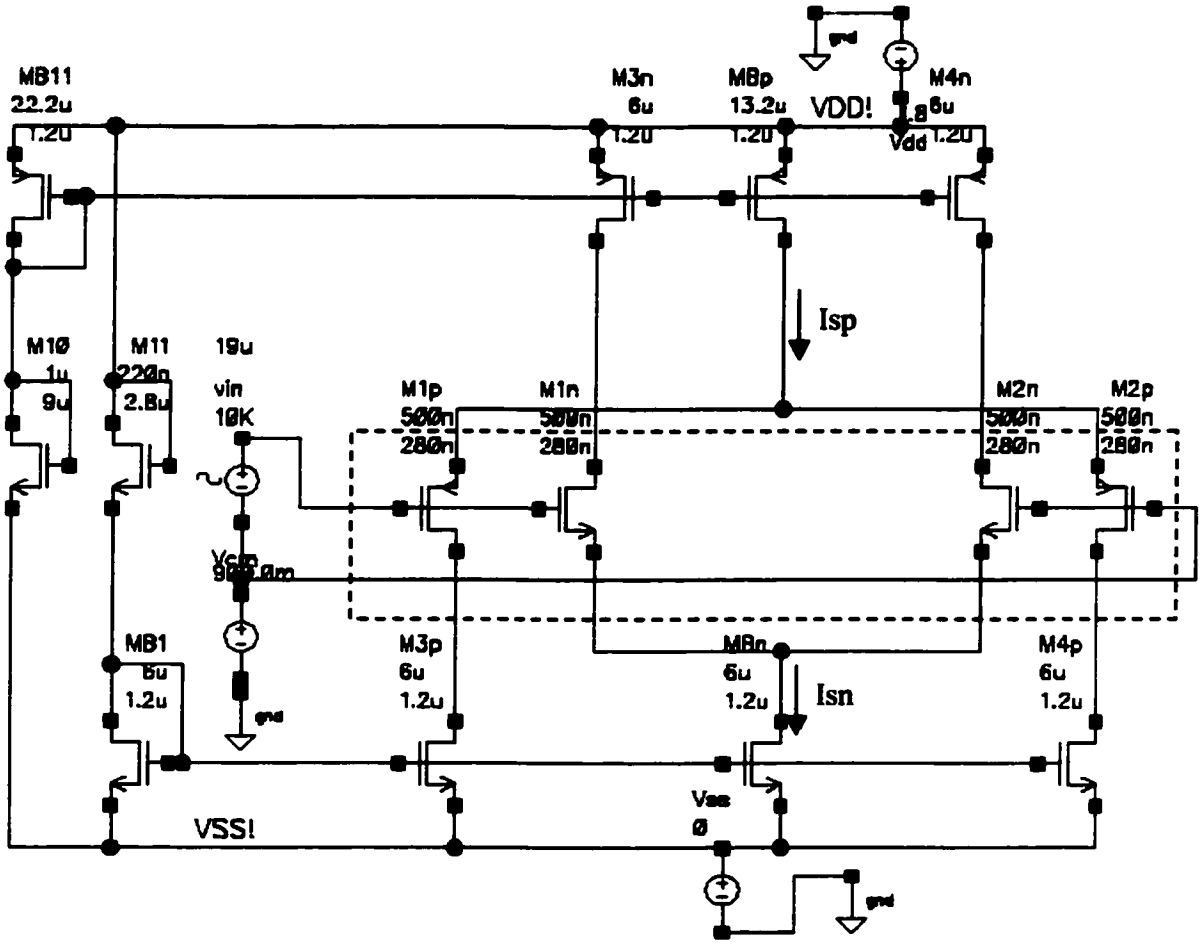


The four curves of input signals vary from 0 to 1.8 V, making a rail-to-rail input range. Due to the amplitudes of the four input sine waves are extremely small (only 19μV), we can only see four straight lines.

The proposed op-amp design requires that both unity-gain bandwidth and slew rate must be maintained constant over the full common-mode input range. But from the circuit in Figure 3.2 we can find that in a conventional rail-to-rail complimentary input stage, above goal cannot be achieved. This is because when the common-mode input signal is near one of the rails, only one of the pairs turns on; the other is cut off. At the middle of

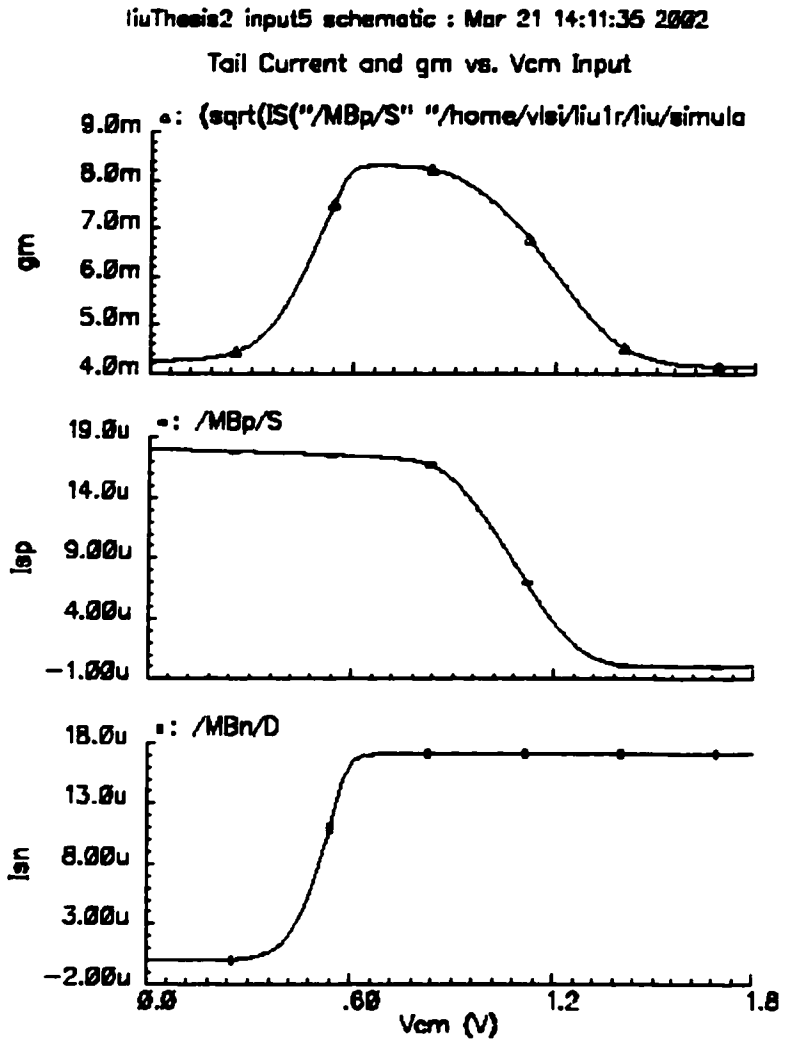
the common-mode input range, both the n-and p-pairs are on, and the g_m has been doubled, please refer to Figure 3.3 on next page.

Figure 3.2 Rail-to-Rail Input Stage Before Modifying



In above schematic, power supply ranges between 0-1.8 V, and the "0" V power supply in negative rail is for simulation purpose only. This is because the VSS! can not be shorted directly to the ground. Two differential input pairs M1n-M2n and M1p-M2p are indicated in the dashed area.

Figure 3.3 Doubled-g_m Over Common-Mode Input Range



3.3 Design Algorithm

From above analysis we know that in order to obtain constant-g_m, we must modify the circuit in Figure 3.2. It can be calculated that for each part of the common-mode input range the g_m is given by:

$g_m = \sqrt{(2\beta I_{ref})}$ (1)

with $\beta = \mu_n C_{ox}(W_n/L_n) = \mu_p C_{ox}(W_p/L_p)$ (2)

where μ is the mobility of the charge carriers, C_{ox} is the normalized oxide capacitance, W and L are the width and length of a transistor respectively [1]. The subscripts n and p refer to an N-channel or P-channel input transistor respectively.

Therefore from equation (1) and (2) we can derive that in our rail-to-rail input circuit (Figure 3.2) the overall trans-conductance should be the sum of N-pair and P-pair:

$g_m = \sqrt{(2\beta_n I_{sn})} + \sqrt{(2\beta_p I_{sp})}$ (3)

where $\beta_n = \mu_n C_{ox}(W_n/L_n)$

$\beta_p = \mu_p C_{ox}(W_p/L_p)$

I_{sn} and I_{sp} are the bias current for the N- and P-pair transistors respectively.

From (3) it can be observed that if we want to obtain a constant-g_m, the W over L ratio of the N-channel and P-channel input pair has to obey the following relation:

$\beta_n = \beta_p$, i.e.

$\mu_n/\mu_p = (W_p/L_p) / (W_n/L_n)$ (4)

If the ratio μ_n over μ_p differs from its nominal value because of process variations, the g_m will have an addition variation. For example, if μ_n over μ_p changes about 15%, the additional variation will be approximately 7.5%.

We can easily realize the equation (4) by choosing the W over L of P-channel and N-channel. Then from (3) it can be known that only if:

$\sqrt{I_{sn}} + \sqrt{I_{sp}} = \text{Constant}$ (5)

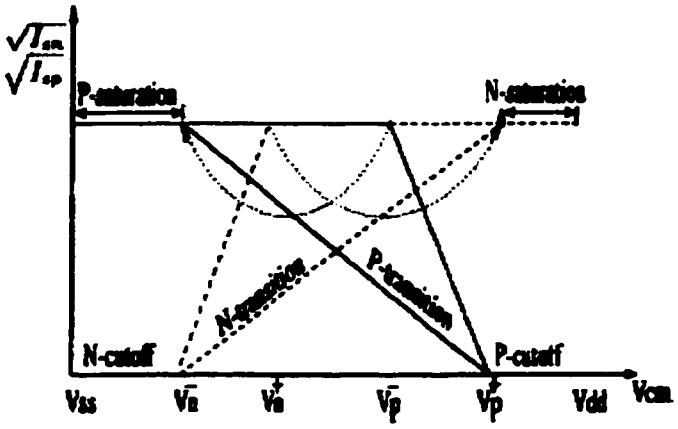
the g_m = Constant

Equation (5) finally simplifies the procedures for modifying the input stage in order to get constant-g_m.

3.4 Overlap Transition Regions

One way of obtaining constant-g_m is to overlap transition regions by moving Vp- left and Vn+ right [3] as shown in Figure 3.4,

Figure 3.4 Overlap Transition Region by Moving Vp- Left & Vn+ Right

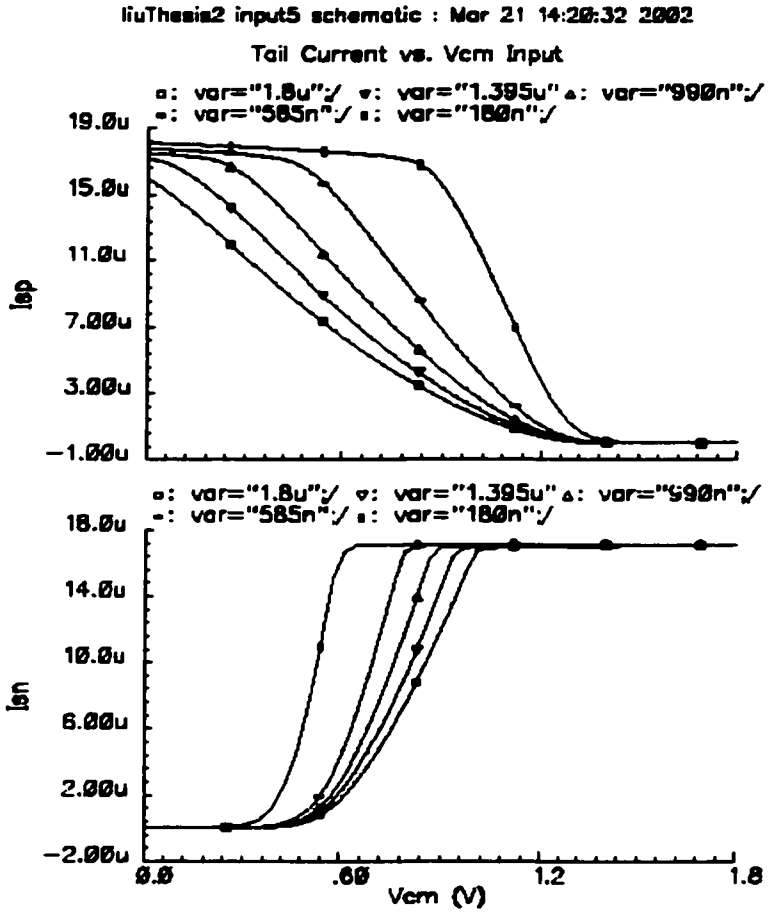


Simulation result can also verify this theory, see Figure 3.5. These curves were obtained by varying the width over length ratios of M1n, M1p, M2n and M2p in Figure 3.2 as follows:

Choose: W(M1n) = W(M1p) = W(M2n) = W(M2p) = 500nm,
and then vary their Lengths from 180nm up to 1.8μm, by 5 steps.

Of course these ratios must fulfill the equation (4) as well in order to get the constant-g_m.

Figure 3.5 Actual Curves of Moving Vp- Left & Vn+ Right

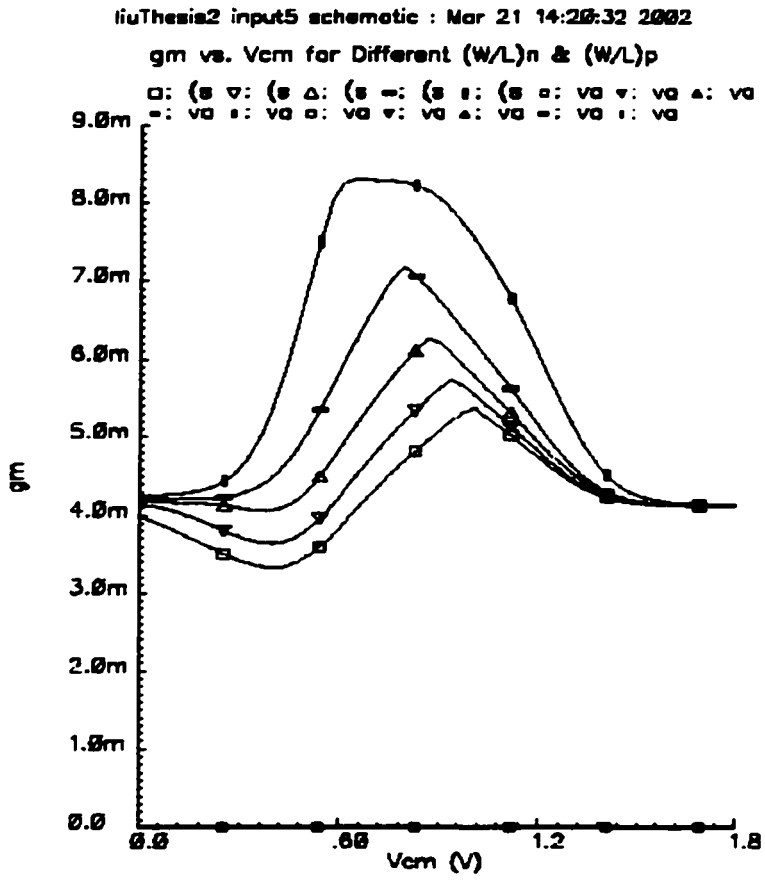


After overlapping the curves we can get the roughly constant-g_m curves; see the bottom curve comparing to upper curves in Figure 3.6. These g_m curves were drawn directly from the curves in Figure 3.5, using the equation (3).

We also find from Figure 3.5 and Figure 3.6 that, as the g_m curves become more flat, the aspect ratios of $(W/L)_n$ and $(W/L)_p$ of the input transistors of the differential pairs are smaller, it is even equal or less than one at bottom g_m curves. From equation (3) we know this means the β_n and β_p become smaller. These smaller βs widen and linearize the transition regions while the increasing $\sqrt{I_{sn}}$ and decreasing $\sqrt{I_{sp}}$ cancel each other, yielding a constant-g_m.

However, the noise performance of this circuit is degraded and the circuit is more sensitive to the mismatches between the differential pair transistors because of the small aspect ratios $(W/L)_n$ and $(W/L)_p$ [3].

Figure 3.6 g_m vs. Vcm Voltage for Different $(W/L)_n$ & $(W/L)_p$ Ratio



Chapter 4

Input Stage With DC Level Shifter

4.1 Introduction

Different from last chapter, which obtains constant-g_m by moving Vp- left and Vn+ right, in this chapter another unique technique of overlapping the transition regions to get constant-g_m without degrade the noise performance of circuit is introduced. Successful implementation and simulation of this technique using 0.18 μm CMOS technology under 1.8 V low power supply are the major breakthroughs and contributions of this thesis.

From the analysis in last chapter we know that constant-g_m can be achieved as long as the two transition regions are overlapped properly. In order to obtain these overlapped transition regions while keeping the original slope of I_{sn}, I_{sp} curves as well as original large β_n, β_p in the whole transition region, we now introduce a DC level shifter which strategically shifts the *P*-transition curve leftward to overlap the *N*-transition curve [3]; see the theoretical curve in Figure 4.1

Figure 4.1 Overlap Transition Regions by Shifting *P*-pair Curve Left

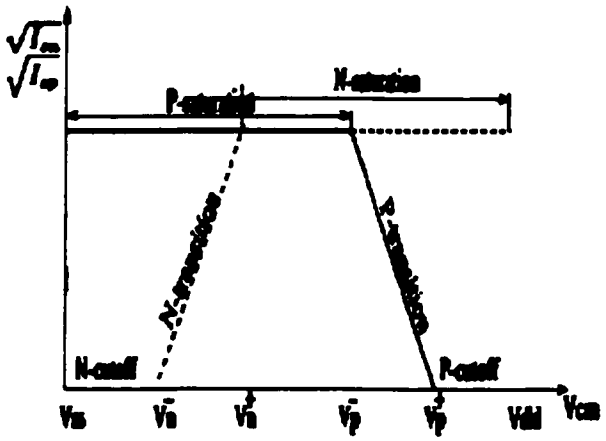
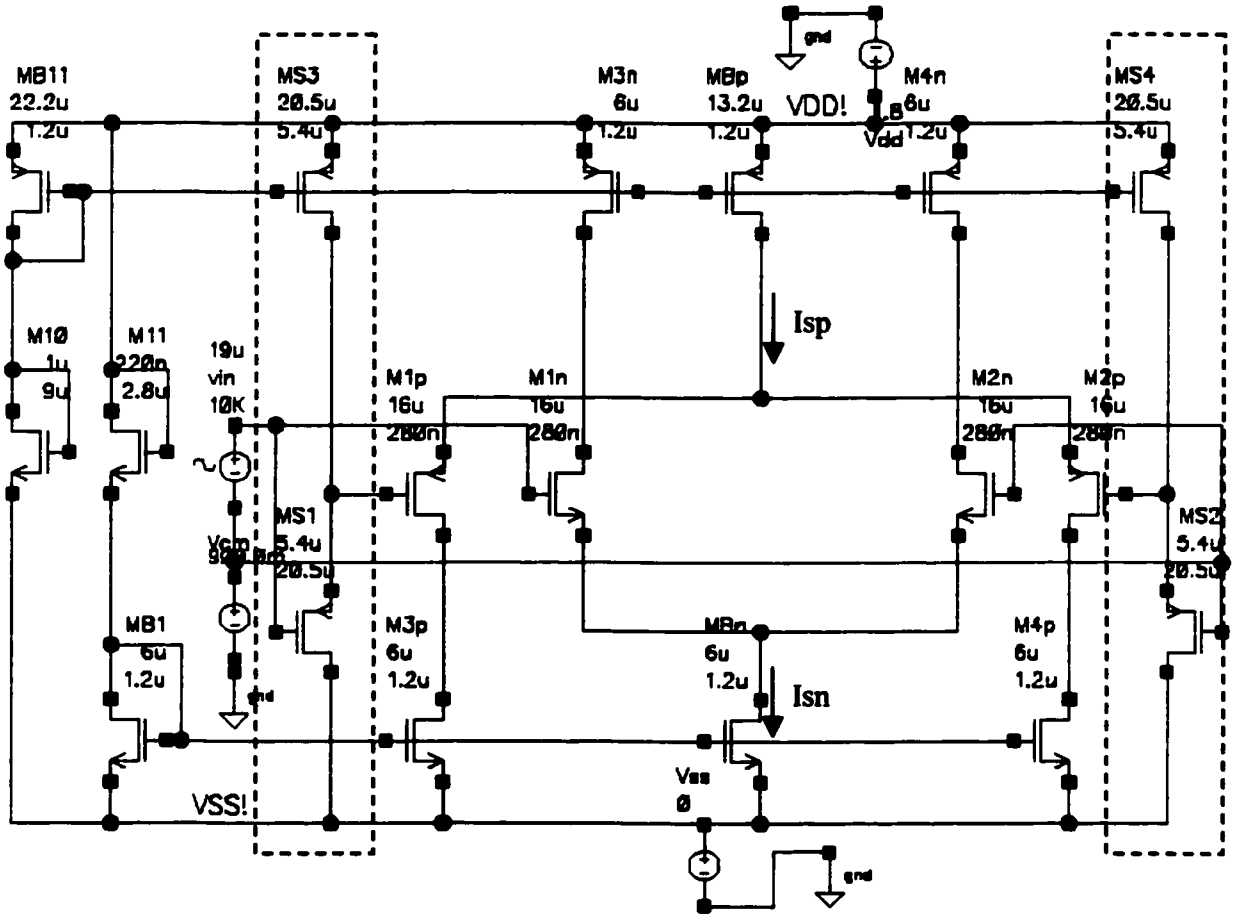


Figure 4.2 Schematic of DC Level Shifter In Complementary Input Stage



4.2 Schematic of Level Shifter In The Complementary Input Stage

Figure 4.2 shows the schematic of DC level shifter in the complementary rail-to-rail input stage. Indicated in dashed boxes, the two pairs of MS1, MS3 and MS2, MS4 form the DC level shifter. These two PMOS pairs are added into the original circuit (Figure 3.2) as source followers.

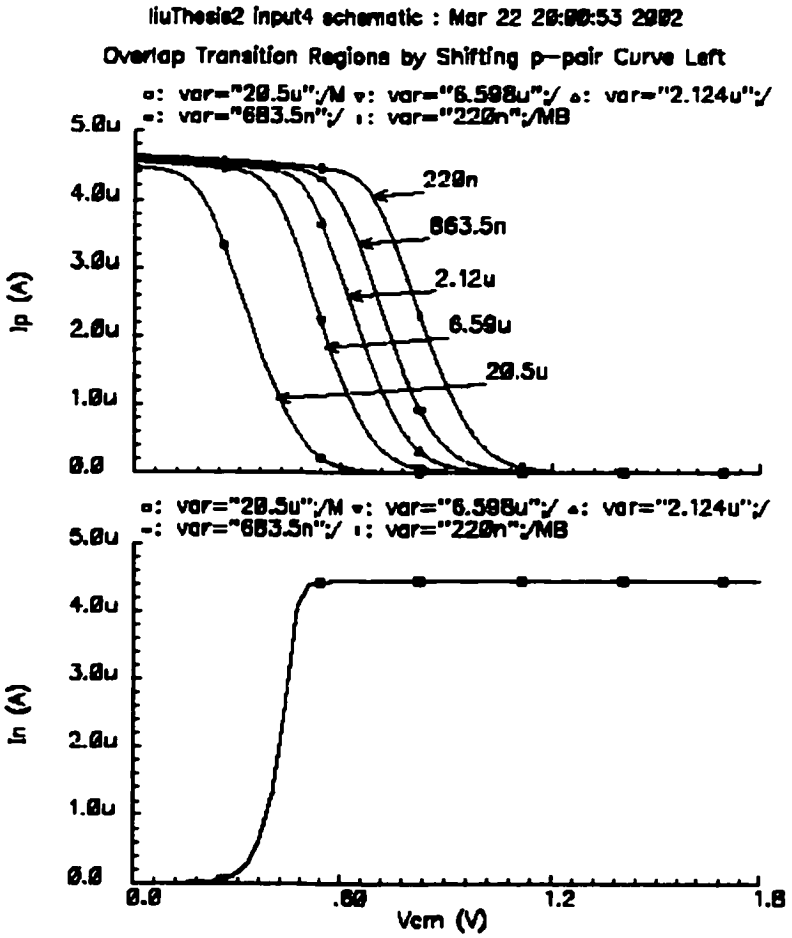
In order to shift the *p*-pair curves left more effectively, the sizes of all four transistors of DC level shifter are varied as follows:

1) $W_{MS1} = W_{MS2} = 5.4\mu m$

   $L_{MS3} = L_{MS4} = 5.4\mu m$

2) Vary $L_{MS1} = L_{MS2} = W_{MS3} = W_{MS4}$ from 220nm up to 20.5μm, by 5 steps, see Figure 4.3.

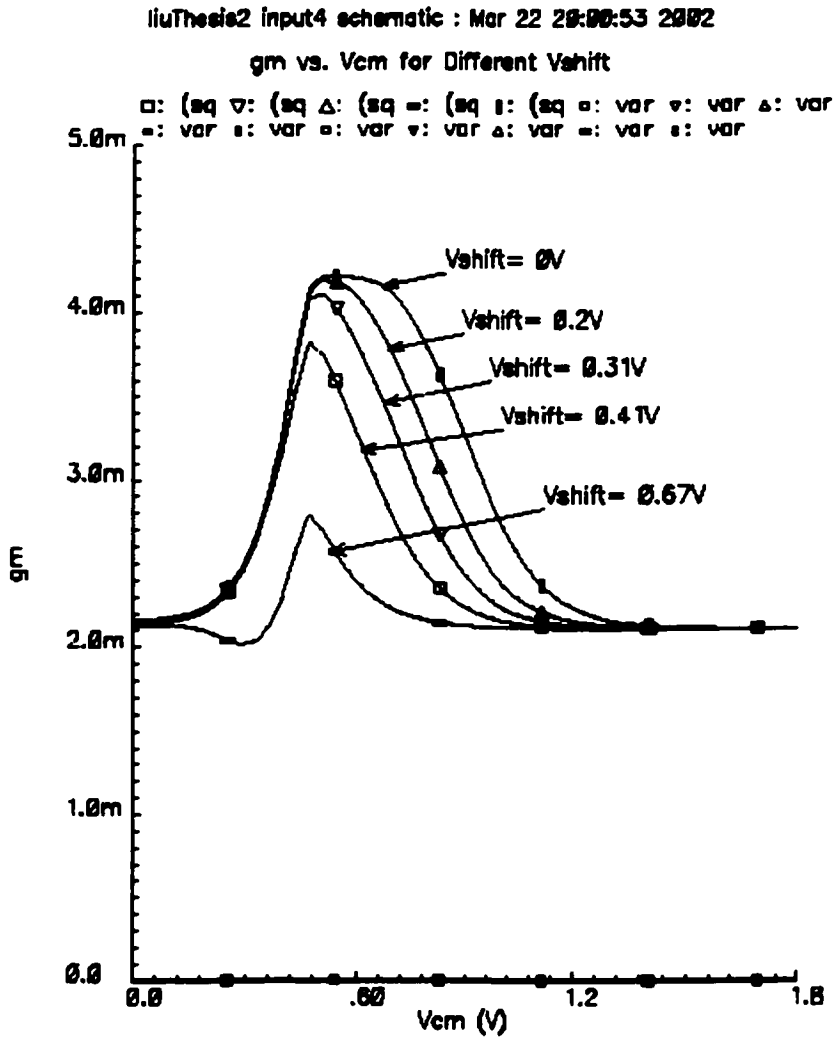
Figure 4.3 Shifting the *p*-pair Cures Left



From Figure 4.3 we can find that the original slope of the curves is preserved, i.e. the original large β is kept. We can also find that the DC level shifter only shifts p-pair curves left, it will not affect the position of n-pair curve.

We can prove from the curves that $\sqrt{I_{Sn}}$ is monotonically increasing within the transition region while $\sqrt{I_{Sp}}$ is monotonically decreasing. So if we can properly overlap the n- and p-pair transition regions, they can cancel each other to achieve a relatively constant $\sqrt{I_{Sn}}+\sqrt{I_{Sp}}$ or g_m. See Figure 4.4. This figure is directly from Figure 4.3, using the equation (3).

Figure 4.4 g_m vs. $V_{common-mode}$ For Different V_{shift}

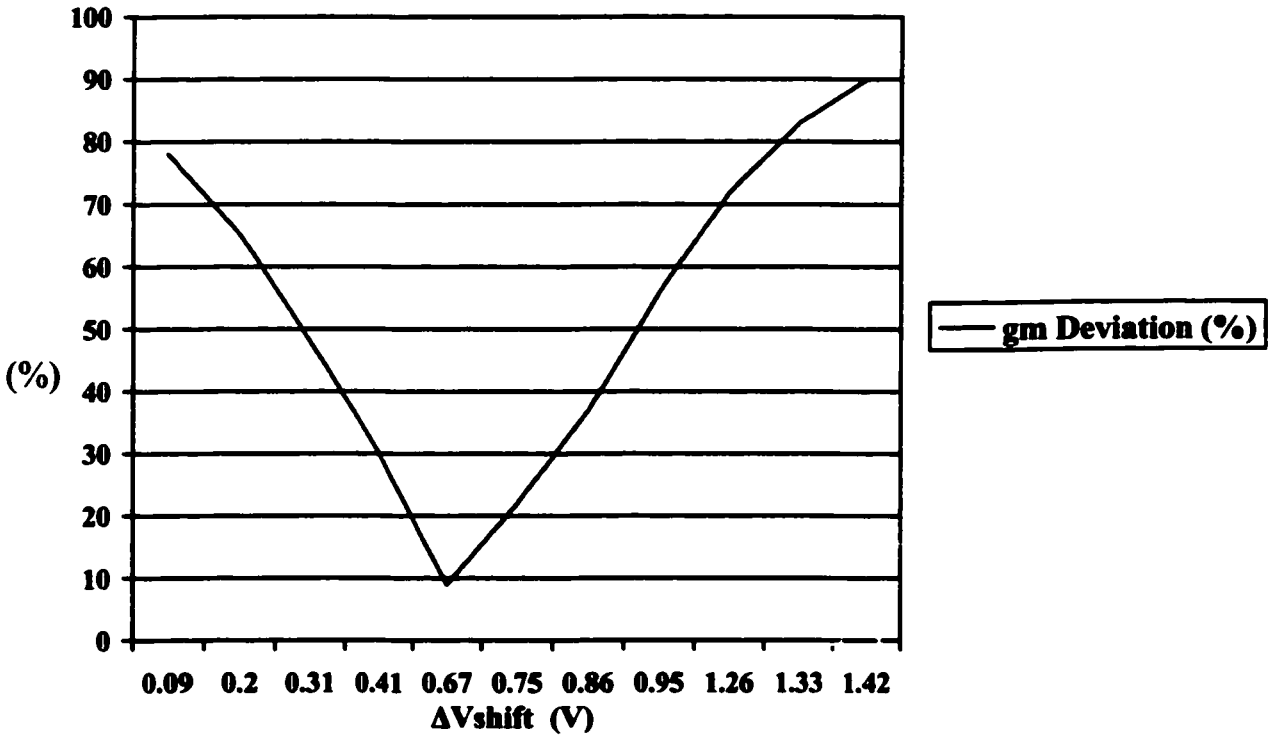


4.3 Optimization of the Shifting Voltage ΔV_{shift}

We can notice from Figure 4.4 that the variation of g_m is subject to the ΔV_{shift}, which in turn is controlled by the dimensions of two *p*-pairs level shifter. If the I_{sp} curve was shifted leftward insufficiently, the g_m is still not constant. However if the I_{sp} curve was shifted leftward too far, the tip of the g_m curve will go to negative: this is the optimization problem.

Only when the I_{sp} curve is shifted properly, a relatively constant-g_m can be achieved. Figure 4.5 denotes the relationship between the ΔV_{shift} and g_m deviation percentage. This curve is based on numerous simulation results.

Figure 4.5 g_m Deviation vs. ΔV_{shift}



From above curve we can easily indicate the best ΔV_{shift} voltage, which is 0.67V. The g_m

corresponding to the optimal shift voltage is constant within 8% of deviation. From the curve we know if the ΔV_{shift} is varied by ±0.6V, the g_m deviation will increase from its optimal 8% up to over 80%.

4.4 Optimal Constant-g_m Obtained

After simulations in Sections 4.2 and 4.3, we can finally choose the constant-g_m we desired. First we choose the dimensions of *p*-pairs level shifter:

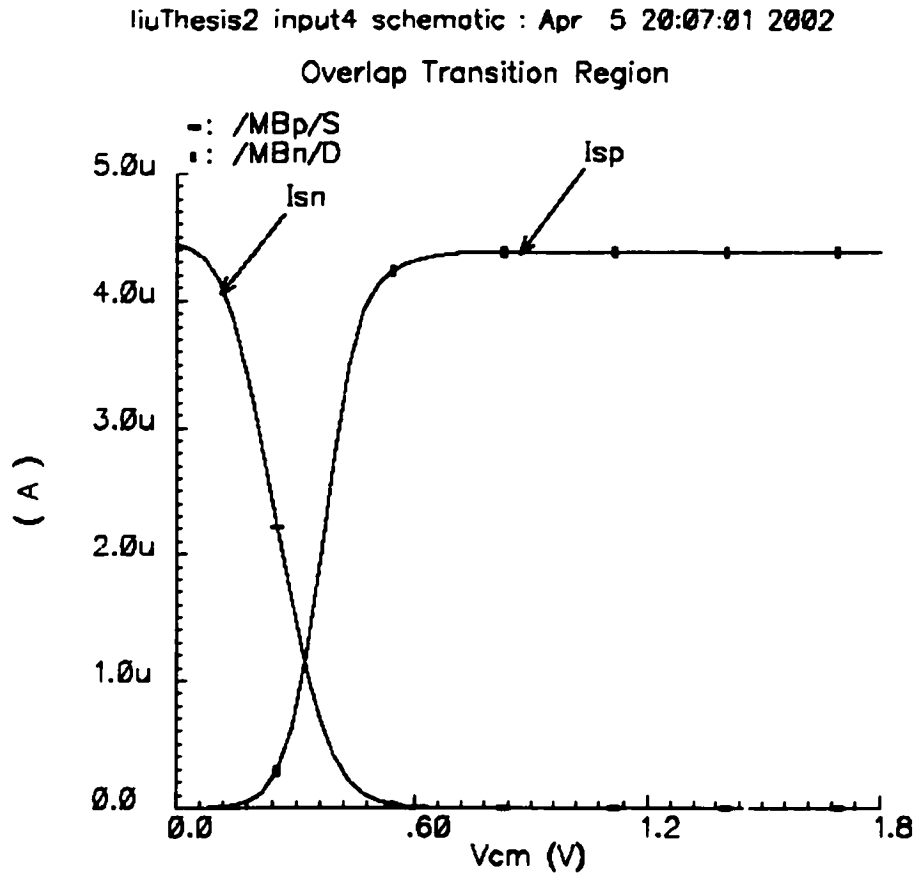
$W_{MS1} = W_{MS2} = 5.4\mu m$

$L_{MS3} = L_{MS4} = 5.4\mu m$

and $L_{MS1} = L_{MS2} = W_{MS3} = W_{MS4} = 20.5\mu m$

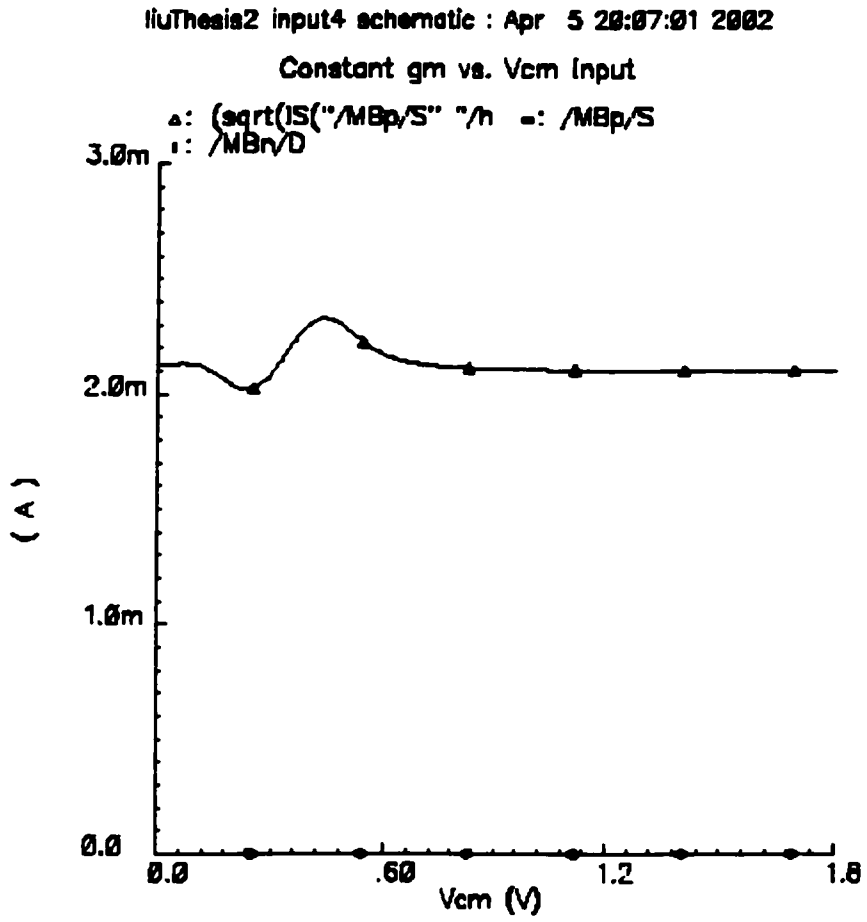
to shift the I_{sp} leftwards to its optimal position, as in Figure 4.6

Figure 4.6 Optimal Overlapped Transition Region



And then we can get the optimal constant-g_m, see Figure 4.7

Figure 4.7 Optimal Constant-g_m Obtained



Above figure is also directly from Figure 4.6. The g_m in above figure is deviated less than 8% and is quite acceptable by the rail-to-rail input stage of an op-amp.

One of the important goals of this thesis is to obtain the reliable constant-g_m, so that by using complementary rail-to-rail input stage, following requirements can be fulfilled:

- the gain of op-amp will not vary
- the unity-gain frequency will be constant
- common-mode rejection ratio will be kept high
- the slew rate will not vary

Chapter 5

Complete Op-Amp

5.1 Introduction

The op-amp designed in this thesis consists of three stages:

1) First stage (including complementary input stage)
2) Folded cascode stage
3) Class A-B output stage

Detailed discussion has been done for input stage in the previous chapters. The folded cascode stage provides high gain while keeping the input and output swing high. At last, the class A-B output stage ensures rail-to-rail output swing [24].

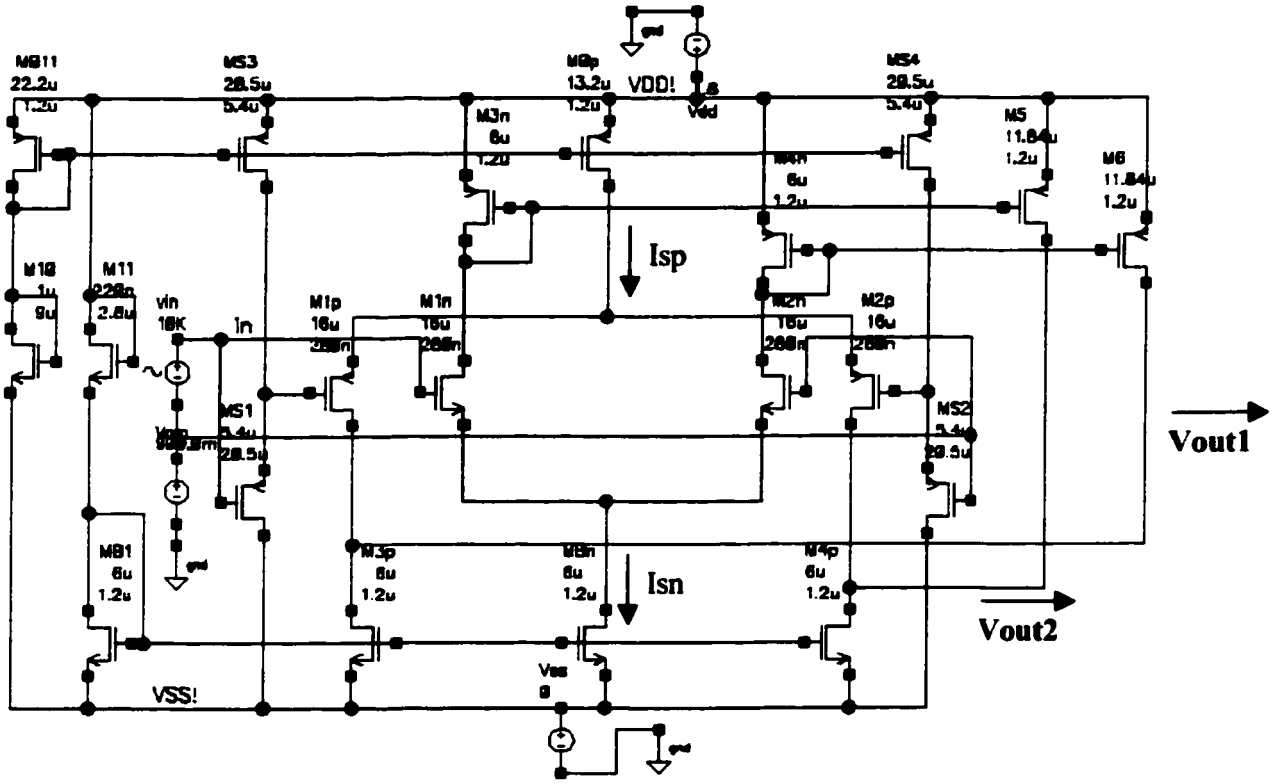
A true rail-to-rail output stage capable of sourcing and sinking equal amounts of current is desired in this thesis. To make efficient use of the supply voltage and supply current, an op-amp requires a complementary push-pull class A-B biased output stage connected in a common-source configuration. Moreover, the class A-B control should be compact to efficiently use die area.

A drawback of the class A-B control is that the quiescent current of the output transistors depends on supply voltage variations [1].

5.2 First Stage

Figure 5.1 shows the first stage (including input stage) of the proposed op-amp:

Figure 5.1 First Stage of the Op-Amp (Including Input Stage)



The input signal is a sine wave with following data:

- f = 10k Hz
- $V_{amplitude}$ = 19μV
- AC magnitude = 1

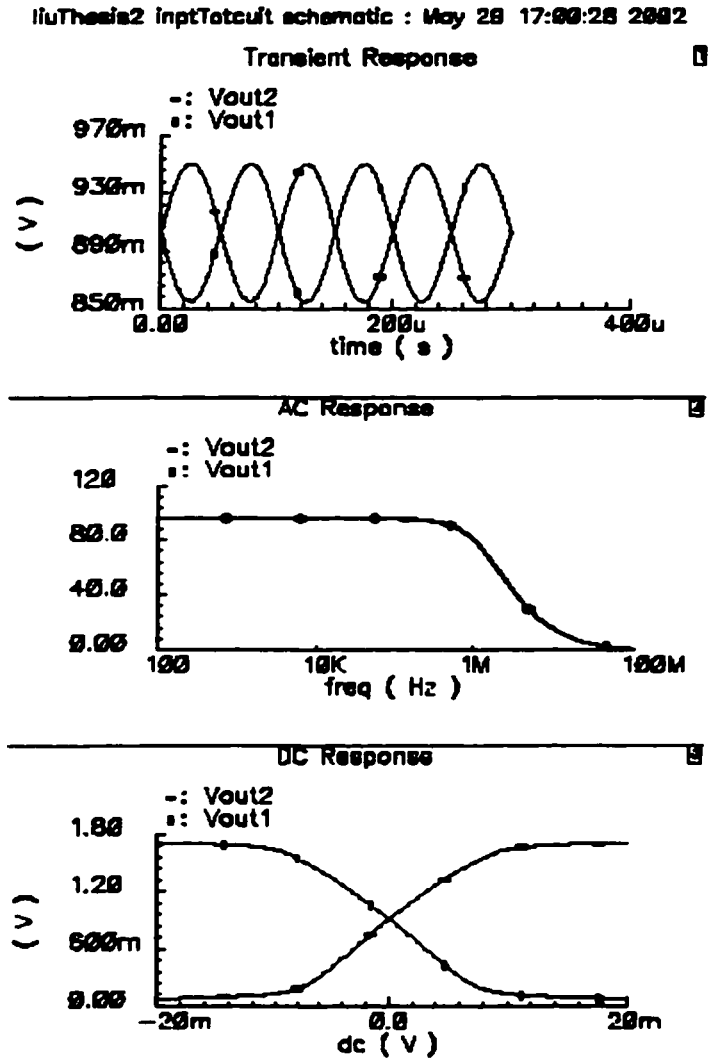
connected to Vin+ and Vin- of the differential pairs respectively.

Common-mode voltage V_{cm} = 0.9V

Power supply is 1.8V DC, connected to VDD!. Another power source connected to the ground is still for simulation purpose only, as indicated before.

Output signals are collected from Vout1 and Vout2 as in Figure 5.1, the simulation result is shown in following Figure 5.2

Figure 5.2 Output Response of First Stage



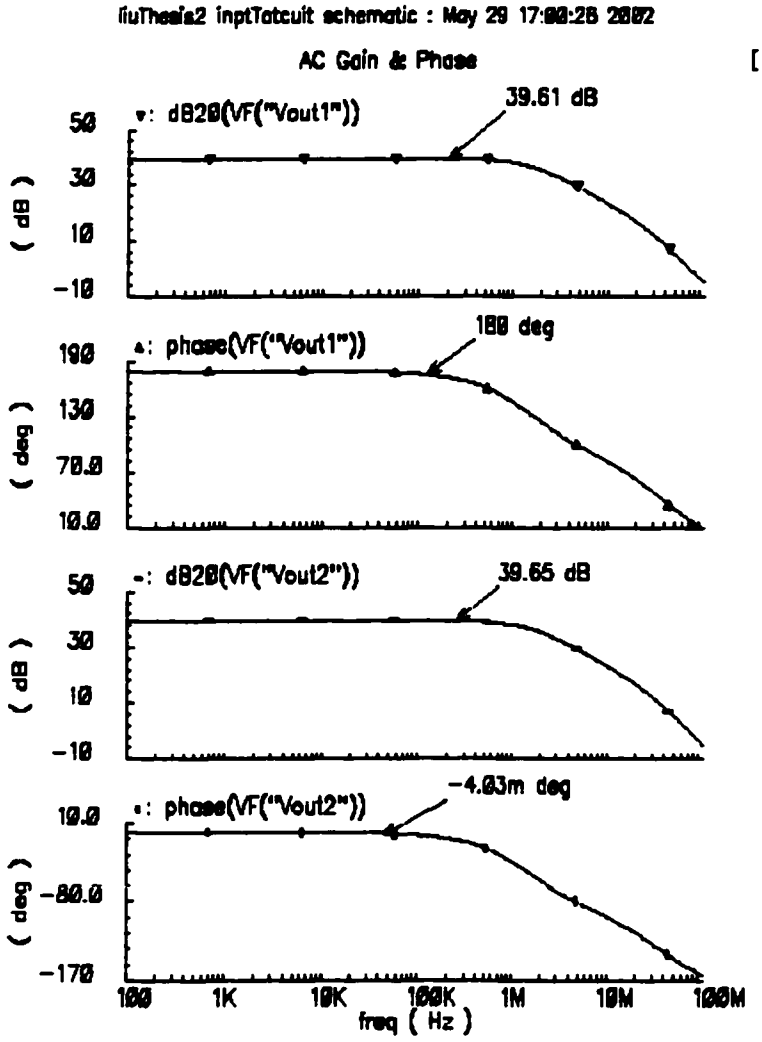
From the top curve in Figure 5.2 we can see that Vout1 and Vout2 are exactly reverse in phase, in which Vout2 has same phase as input signal and Vout1 has a totally reversed phase to input signal. In AC response (middle curve), output AC magnitude is 95.61, this

number is the ratio of Vout over Vin AC magnitude. It means the amplification of first stage is 95.61 times, or 39.61dB.

From the bottom curve of DC response, it can easily be identified that both Vout1 and Vout2 jumped their voltage level from 1.8V down to 0 or from 0 up to 1.8V respectively, around the dc input voltage of zero. This means that only very small dc input voltage variation will cause the output voltage level jump linearly from rail to rail. The amplification function of op-amp is just based on this linear region.

Figure 5.3 further supports above analysis, with phase(Vout1) = 180°, phase(Vout2) =0°,

Figure 5.3 Voltage Gain & Phase of First Stage



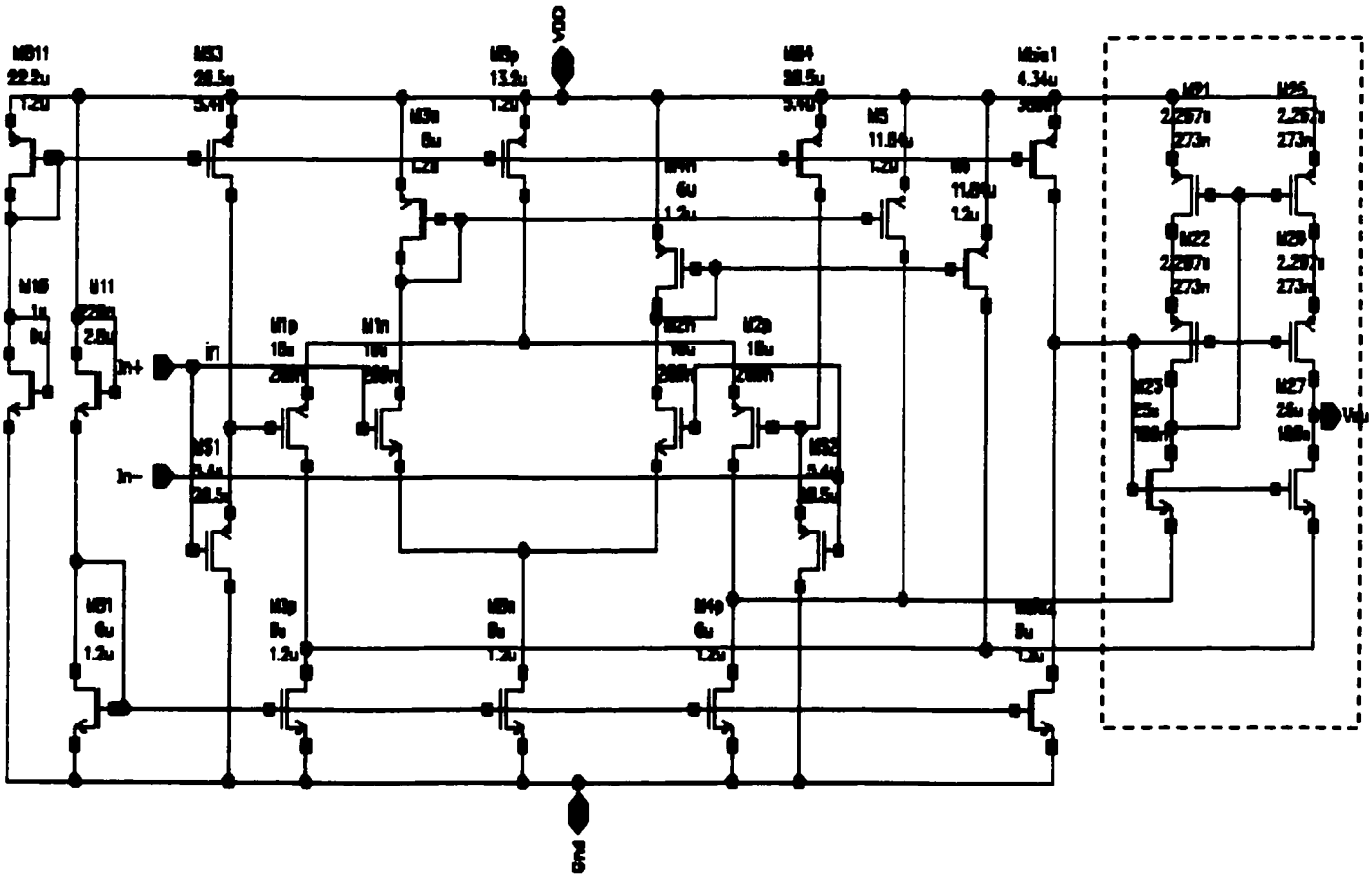
Gain (Vout1) = Gain (Vout2) = 39.6 dB. Figure 5.3 is also directly converted from Figure 5.2, using Cadence calculator function.

5.3 Folded Cascode Stage

For each stage, numerous simulation runs have been done in order to get optimal parameters. For example, we can set a rough range of one transistor's size, and then use sweep function to choose the optimal size with best simulation result. Fortunately, once the previous stage has been set, it will work steadily and any changes to the later stages will not affect its performance.

In Figure 5.4, folded cascode stage has been added to the first stage to provide high gain and keep the input and output swing high [17][18][19], see the transistors in dashed box.

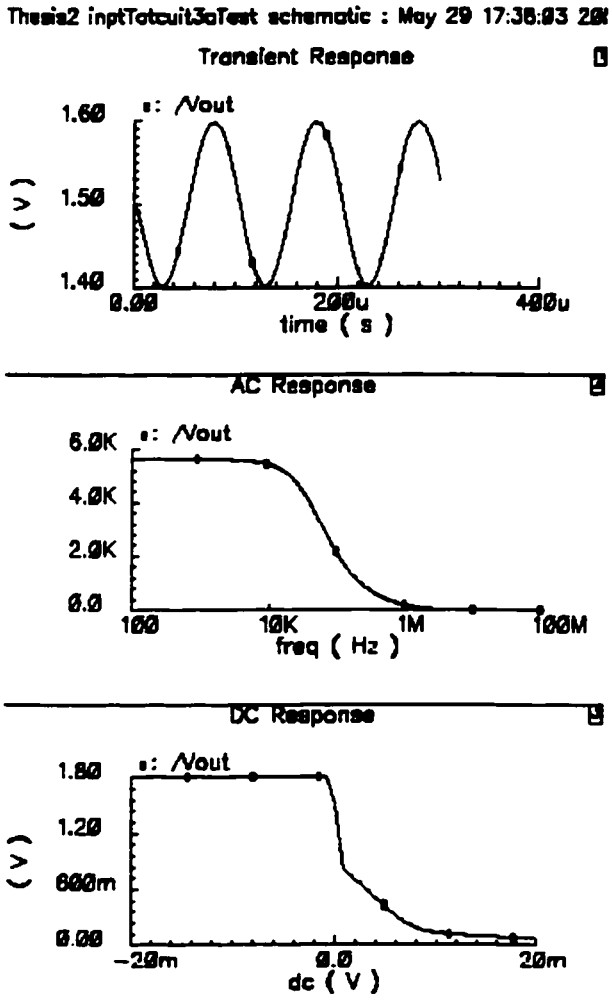
Figure 5.4 Folded Cascode Stage



Input signal remains the same as in first stage, output signal is combined to one instead of two.

Figure 5.5 shows the output response of cascode stage.

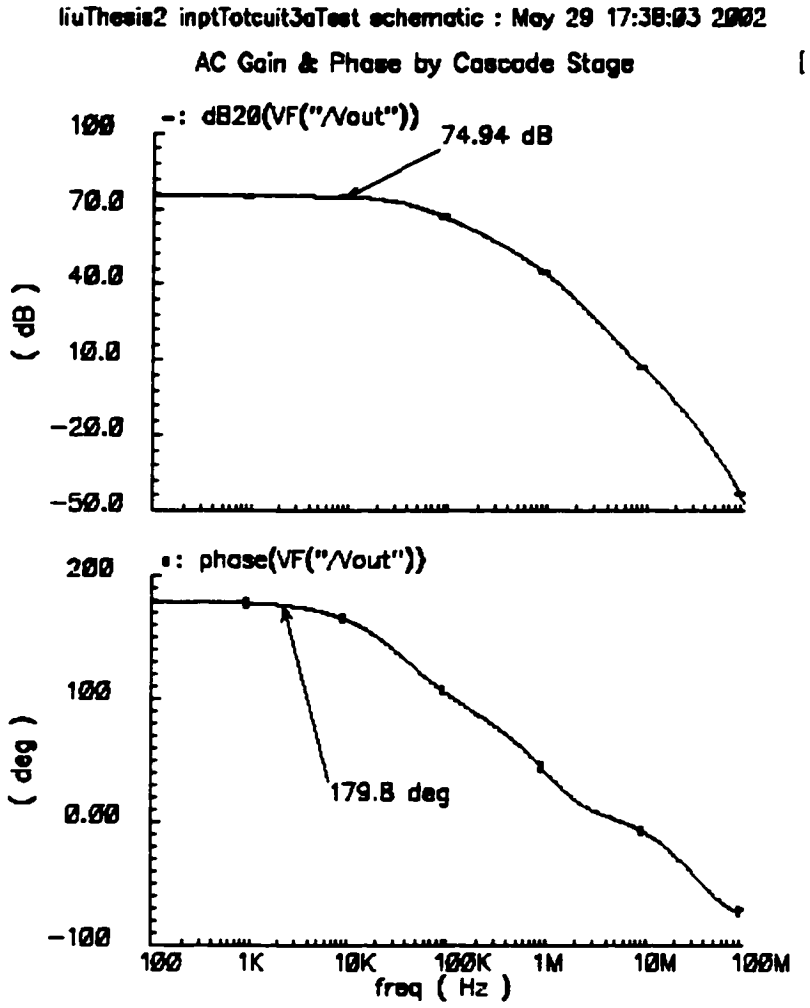
Figure 5.5 Output Response of Cascode Stage



In Transient response curve of Figure 5.5, the output swing has increased to 1.4V--1.6V, and it is still in reversed phase to input signal. The AC response curve shows the amplification has increased to 5.6k times (74.9dB); at last the DC response curve shows the rail-to-rail output variation against very small input changes.

Again, the voltage gain and phase response in Figure 5.6 are directly converted from Figure 5.5.

Figure 5.6 Voltage Gain & Phase Response of Cascode Stage



The voltage gain has increased to 74.94 dB while the phase is still in reverse, close to 180°.

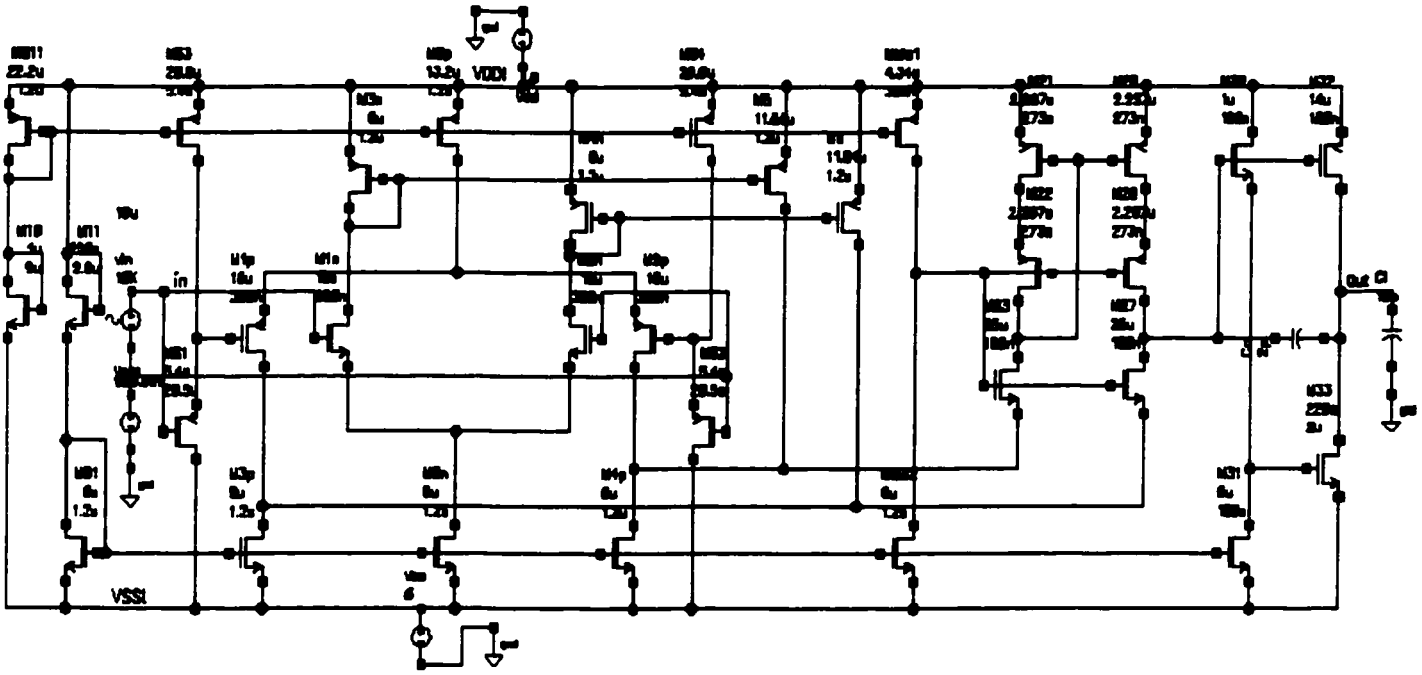
5.4 Complete Schematic (Including Class A-B Output Stage)

This schematic is fully differential therefore it can reject supply and substrate noise. This

type of structure also offers rail-to-rail input and output swing, higher common-mode rejection ratio, and lower clock feed-through noise [14] (since it appears as a common-mode signal).

Figure 5.7 shows the full op-amp with the DC level shifters in the complementary input stage.

Figure 5.7 Complete Op-Amp Schematic



Now we can review the whole components of the circuit. In above Figure 5.7 structure, differential input pairs consist of M1n, M1p, M2n and M2p. DC level shifter includes MS1--MS4. Folded Cascode stage includes M20--M23, M25--M27, M3p and M4p, MB01and MB02 are used to bias the cascode stage. This cascode stage increases gain without sacrificing output swing or speed. MB1 and MB11 are used to bias the overall circuit.

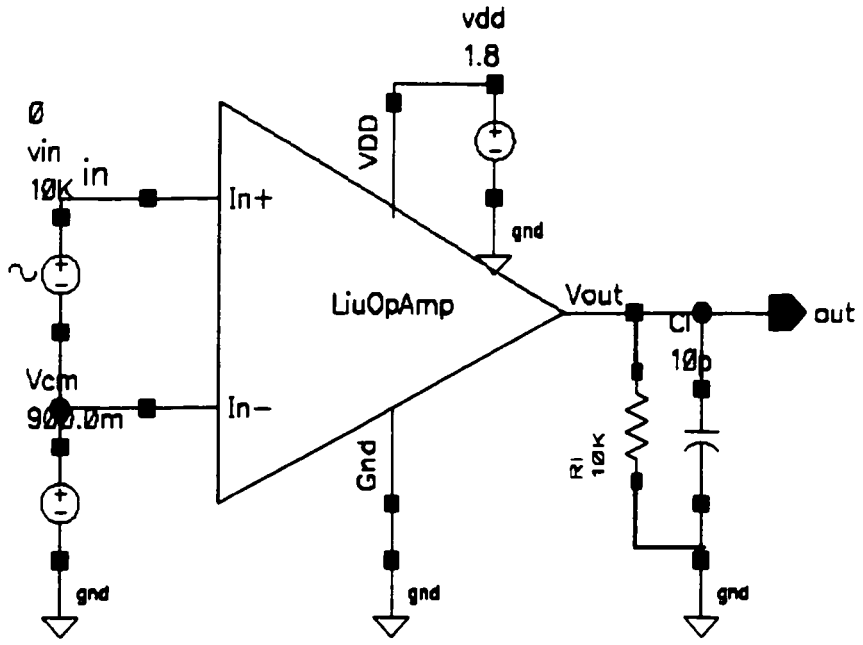
M10 and M11 are functioning as two resistors. Because the resistor can occupy large die area in 0.18μm CMOS technology, these two resistors are replaced by two N-MOS

transistors. Simulations proved that they just performed as good as resistors.

Class A-B output stage includes M30 – M33. Cc is the compensation capacitor. The trans conductance g_m of the input stage and Cc set the unity gain frequency of the amplifier, it equals to g_m/Cc [5]. At last R_L and C_L are the resistive and capacitive loads with the values of 10kΩ and 10pF, respectively.

For simplicity, circuit in Figure 5.7 is configured to Figure 5.8, all simulation results mentioned later on are from this configuration instead of above complex topology.

Figure 5.8 Op-Amp Configuration



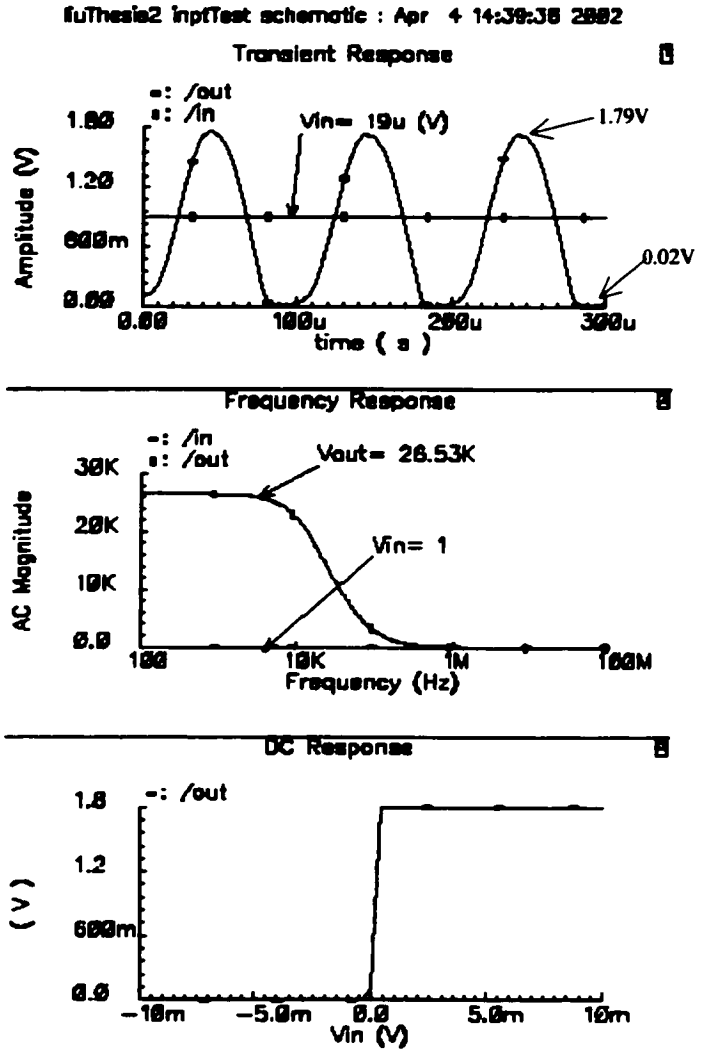
In following simulations, this op-amp symbol will be configured differently to meet different requirements.

5.5 Frequency Response of Complete Schematic

After class A-B output stage, transient response has reached 0.02 ~ 1.79V rail-to-rail

output swing, while AC magnitude has increased to 26.53k times (88.5 dB) comparing to input signal. The slope of DC response curve becomes bigger, representing a rail-to-rail output jump against a smaller input signal variation, see Figure 5.9

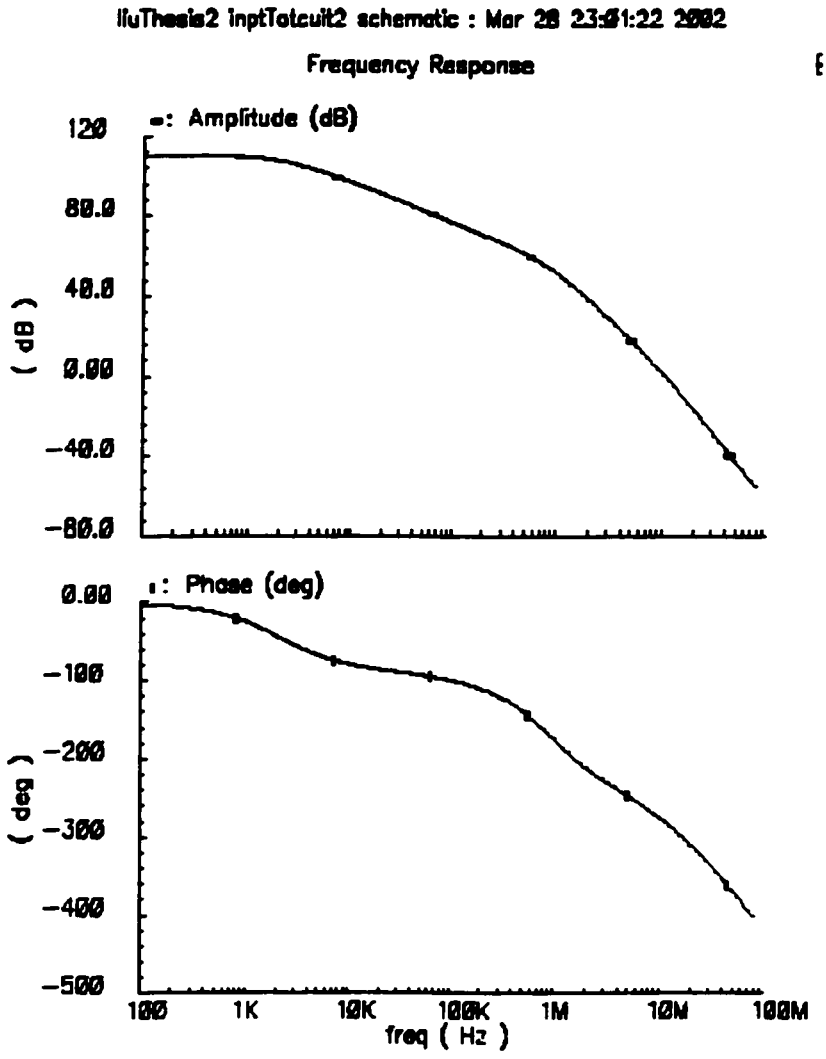
Figure 5.9 Output Response of Complete Schematic



5.5.1 Voltage Gain

As with previous simulations, the following frequency response is also directly from above Figure 5.9. The final voltage gain increases to 88.5 dB and the output signal becomes in phase with the input signal. See Figure 5.10

Figure 5.10 Frequency Response of Complete Circuit



5.5.2 Unity-Gain Frequency

The unity-gain frequency ω_c is defined as the frequency at which $|H(j\omega_c)| = 1$ [4]. From Figure 5.10 we can see the unity-gain frequency equals to 10MHz.

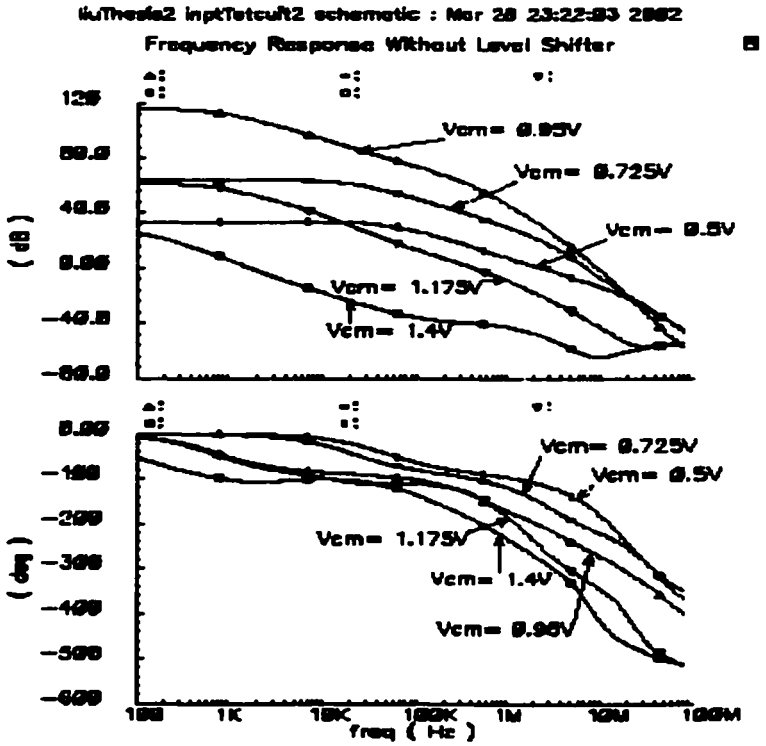
Chapter 6

Simulation of the Complete Op-Amp

6.1 Level Shifter Implementation

In Chapter 3 we have discussed the doubled transconductance g_m phenomenon for conventional complementary differential input stage without level shifter. Following simulation will further clarify what output response of total op-amp will look like if this conventional input stage is implemented, see Figure 6.1

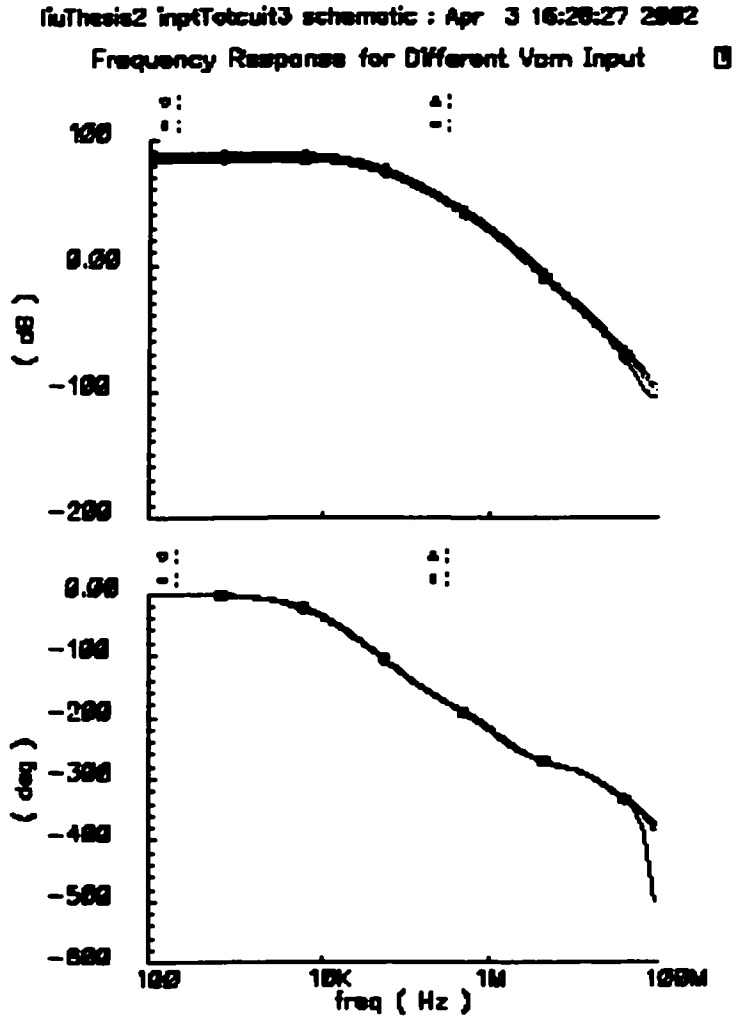
Figure 6.1 Frequency Response Without Level Shifter



In above figure the gains and phases of output signals depend heavily on the applied common-mode input voltage V_{cm}. The variation of V_{cm} has been marked on each curve, which varies from 0.5V ~ 1.4V, in 5 steps. As we have discussed before, this op-amp is unstable and cannot be compensated because of the inconstant-g_m.

However when DC level shifter is implemented, the gains and phases of the proposed op-amp are almost independent of the applied V_{cm}, see Figure 6.2

Figure 6.2 Frequency Response With Level Shifter



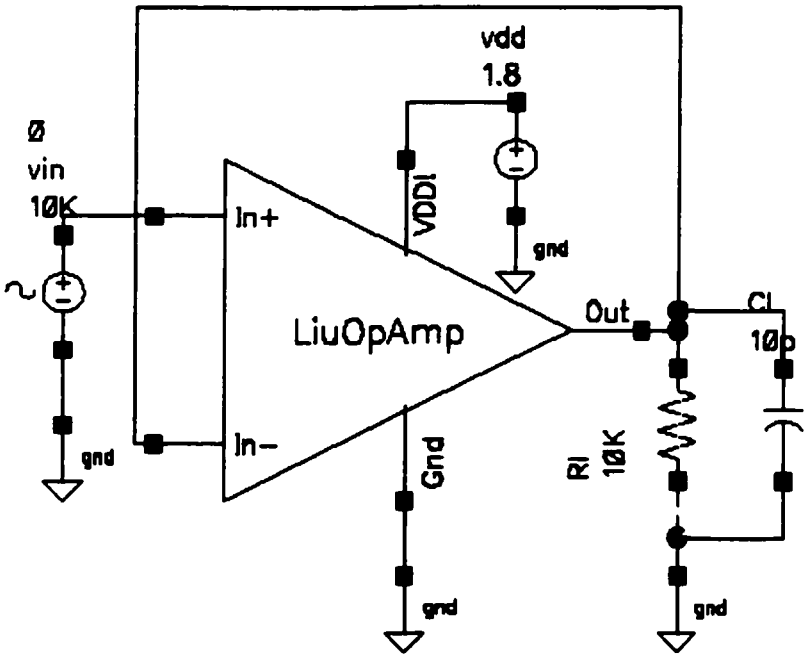
V_{cm} variation in figure 6.2 is the same as in Figure 6.1, but the frequency response of

this proposed op-amp is substantially improved over the op-amp without level-shifted input stage, as in Figure 3.2.

6.2 Input-Output Transfer Character

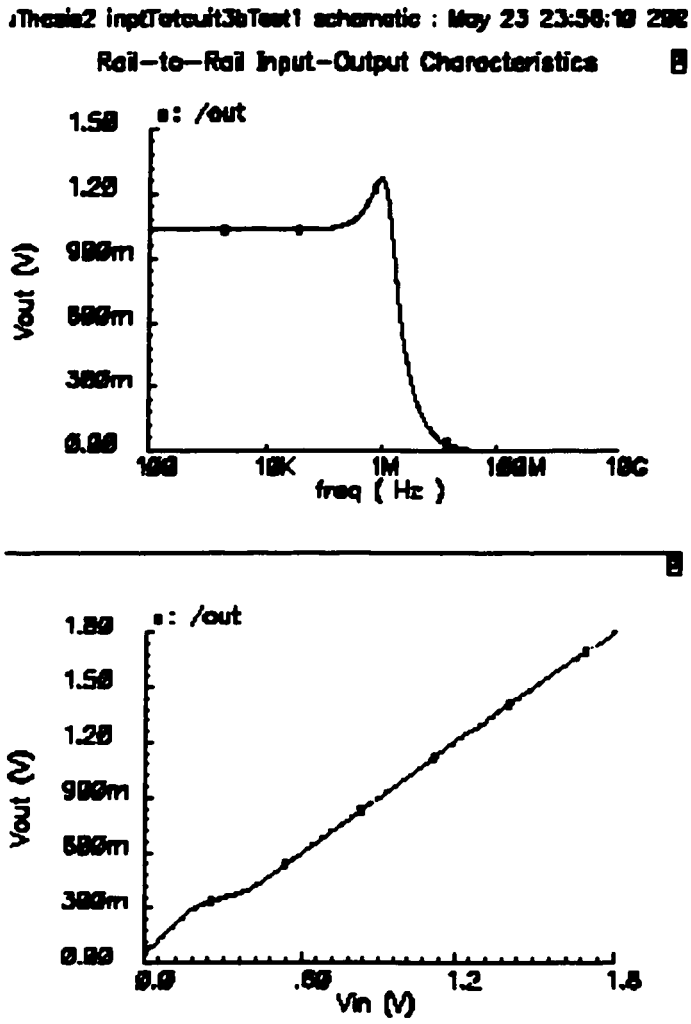
In Figure 6.3 the proposed op-amp is connected as unity-gain configuration in order to measure the input-output transfer character [10]. The load includes a 10kΩ resister R_L and a 10pF capacitor C_L. Input signal is 10kHz sine wave with AC magnitude equals to 1.

Figure 6.3 Unity-Gain Configuration



The following plot verifies that the op-amp has a rail-to-rail (0 ~ 1.8V) input range as well as a rail-to-rail output voltage swing (0.02 ~ 1.79V). Under unity-gain configuration, the input over output voltage ratio is satisfactorily linear, with $V_{in}/V_{out} = 1/1$.

Figure 6.4 Rail-to-Rail Input-Output Character



6.3 Trade-Offs and Optimization of the Op-Amp

The basic characteristics of an "ideal" op-amp should be [21]:

1) Input characteristics:

- Infinite input impedance, or zero input currents

  $Z_{IN} = \infty$, $I_{IN} = 0$

- Perfectly matched input stage, no dc (offset) voltage error

  $V_{IO} = 0$

- No noise sources

  $V_N = 0, I_N = 0$

2) Output characteristics

- Infinite output current, sourcing or sinking

  $I_{OUT\pm} = \infty$

- "Rail-to-Rail" output swing

  $V_{OM\pm} = V_{CC\pm}$

- Infinite step response (slew rate)

  $SR = \infty$

- No constraints on loads: resistive, capacitive or inductive

3) Power Supply characteristics

- No minimum supply voltage requirement; no maximum limit

  $V_{CC(MIN)} \geq 0, V_{CC(MAX)} \leq \infty$

- No power consumption (zero supply current); no power dissipation

  $I_{CC} = 0, P_D = 0$

- Single- or split-supply

4) Transfer characteristics

- Infinite open-loop gain

  $A_{VOL} = \infty$

- No frequency constraints

  $dc \leq f \leq \infty$

- No signal distortion introduced

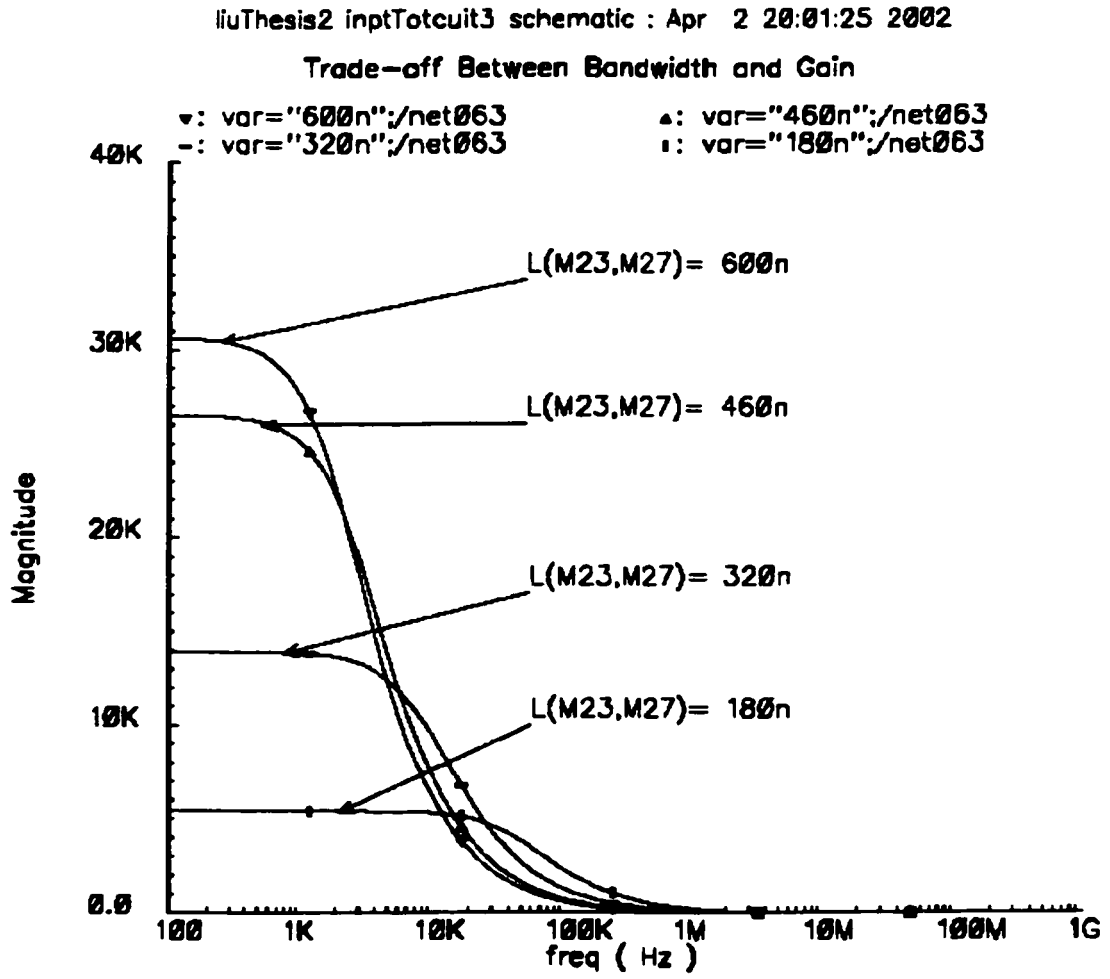
Naturally no op-amp exhibits any of above ideal characteristics. However, understanding these characters will enable us to quickly narrow our choices to a few parameters which can be more carefully evaluated. AC performance often comes with other tradeoffs, not

only with power consumption. In fact, power consumption frequently becomes the pivotal parameter in finalizing op-amp selection.

The final step in choosing a parameter is usually the matter of a more thorough comparison of key specifications and performance graphs to determine the best fit. Making some decisions based on sufficient literature search can lead us to a few parameters from which a more studied selection can be made.

Simulation in Figure 6.5 shows the trade-off between bandwidth and gain. Since the pro-

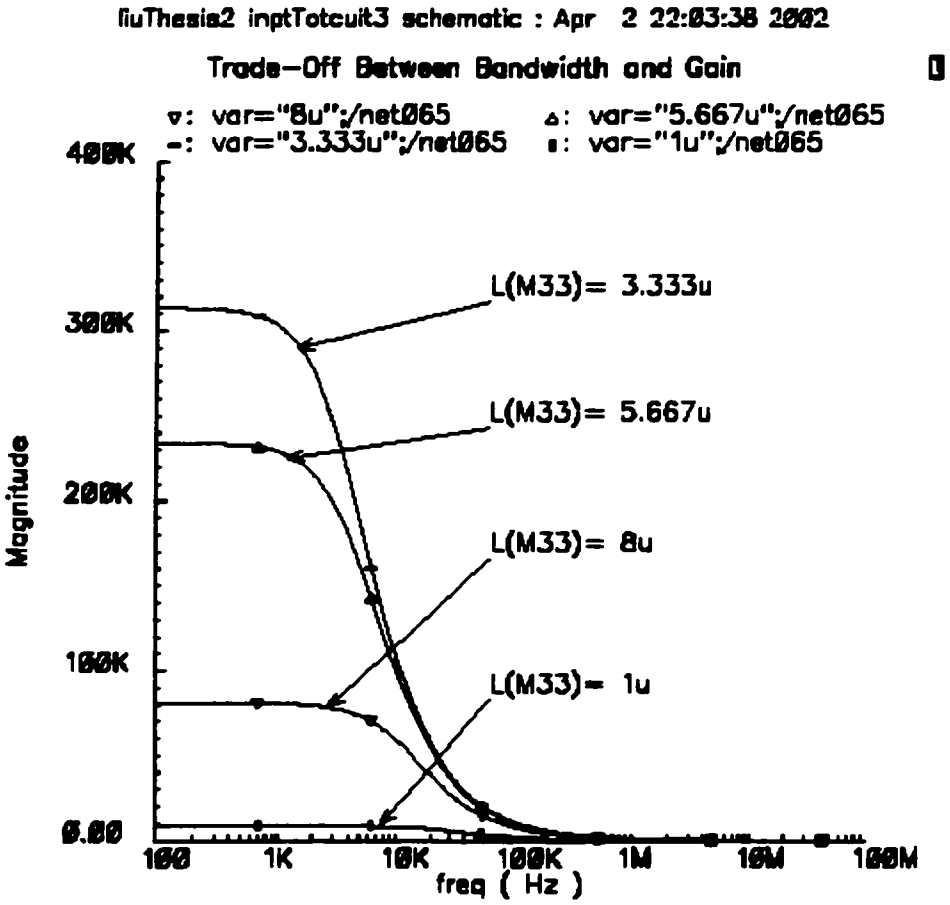
Figure 6.5 Trade-Off Between Bandwidth and Gain



posed op-amp is designed for acoustic signal conditioning, not very wide bandwidth is needed, therefore L= 180nm is chosen for M23 and M27 in complete circuit of Figure 5.7

For the same reason L= 2μm is the best choice for M33, see Figure 6.6

Figure 6.6 Another Trade-Off Between Bandwidth and Gain



Usually one character can tradeoff with several other parameters. This makes the op-amp design an optimization problem, as indicated in previous section 2.1

6.4 Common-Mode Rejection Ratio (CMRR)

CMRR is the ratio of common-mode interference voltage at the input of the circuit to the corresponding interference voltage at the output. Or, the ratio of the differential-mode gain to the common-mode gain is called CMRR:

$$CMRR = 20\log(A_{dm}/A_{cm}) \qquad (6)$$

where A_{dm} and A_{cm} are the differential and common-mode gain, respectively.

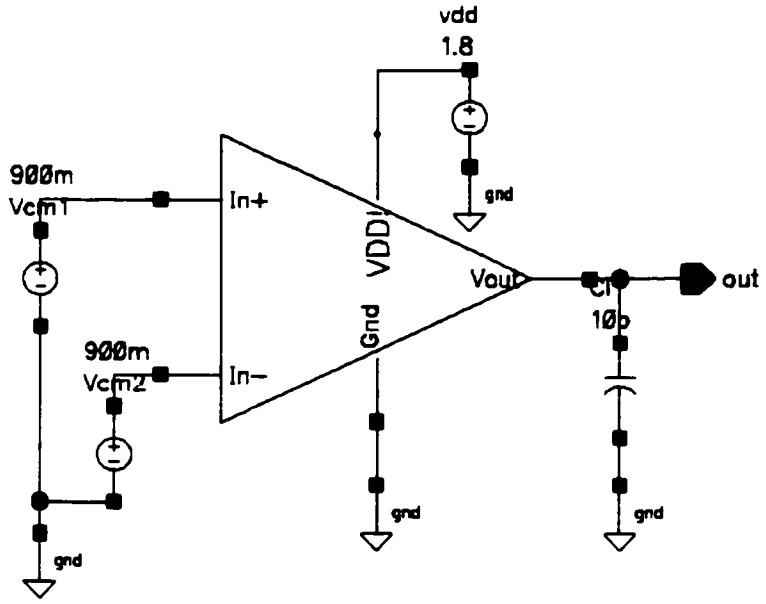
An ideal op-amp is a totally differential amplifier, meaning that it will not output any voltage if exactly the same value is applied to both $V_{in\pm}$ inputs, i.e. $A_{cm} = 0$. Therefore, a perfect op-amp has a CMRR of infinity. In reality if an op-amp has CMRR of 90 dB, meaning the ratio of gain is 31.6k, this number is very acceptable. However if our op-amp can reach a CMRR of 110 dB, this will be an extraordinary high value.

From equation (6) we know common-mode gain and differential-mode gain must be calculated in order to obtain CMRR.

6.4.1 Common-Mode Gain

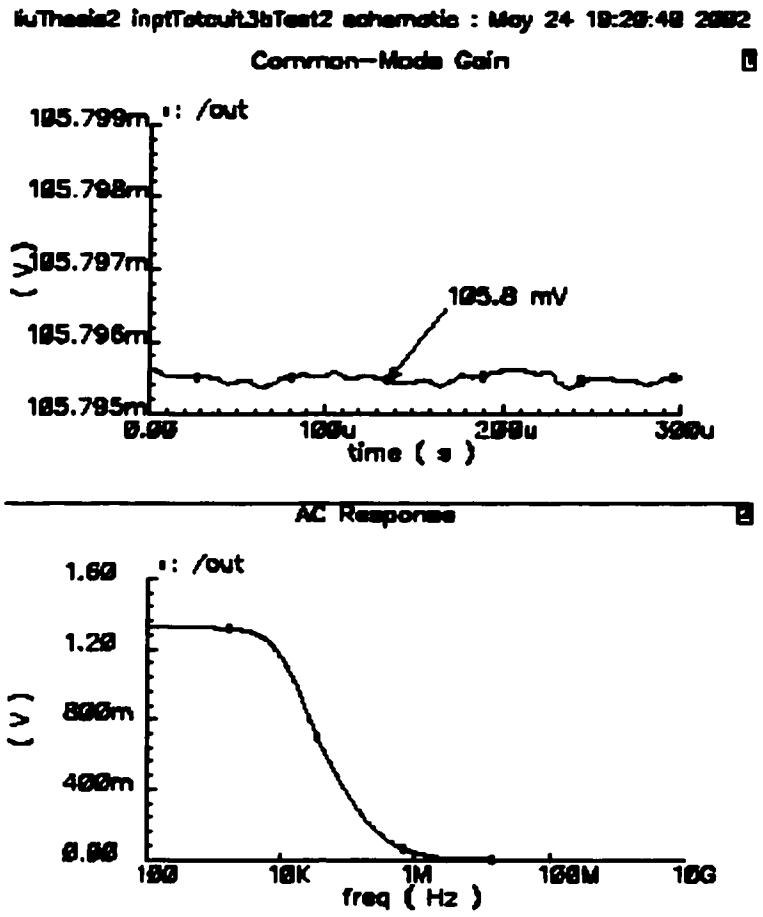
In Figure 6.7, two equal common-mode voltage V_{cm1}=V_{cm2} =0.9V are applied to In+ and In-. We have indicated that for an ideal op-amp the V_{out} should be "0".

Figure 6.7 Common-Mode Input Configuration



And from the proposed op-amp circuit, actually the V_{out} = 105.8 mV, see the simulation result in Figure 6.8

Figure 6.8 Common-Mode Gain



$V_{cm} = V_{cm1} = V_{cm2} = 0.9$ V

V_{out} = 105.8 mV = 0.1058V

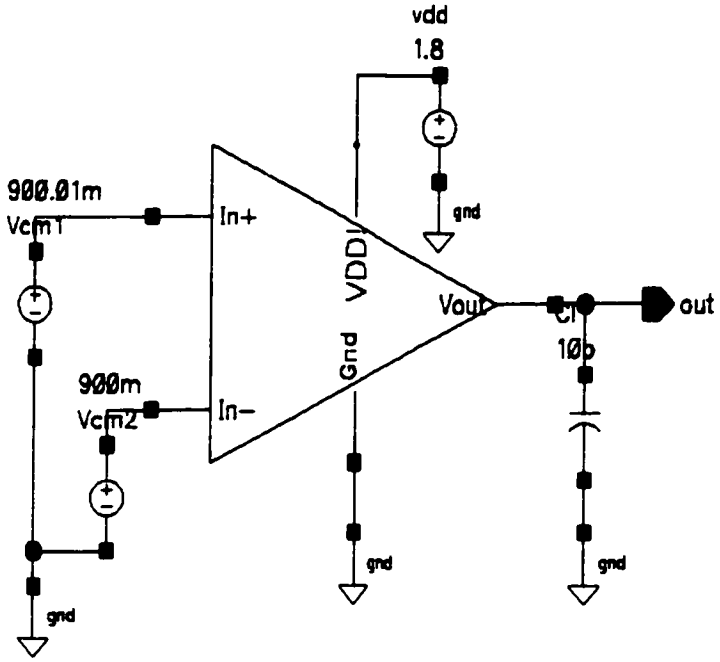
Common-Mode Gain: $A_{cm} = V_{out} / V_{cm} = 0.1176$

6.4.2 Differential-Mode Gain

Using the same method we can calculate the differential-mode gain, see differential-mode configuration in Figure 6.9. Common-mode voltage V_{cm1}=0.90001V is applied to In+

while V_{cm2} =0.9V is applied to In-.

Figure 6.9 Differential-Mode Input Configuration



Then, see simulation plot in Figure 6.10 for output response.

$V_{dm} = V_{cm1} - V_{cm2} = 0.90001-0.9 = 0.00001 = 10\ \mu V$

$V_{out} = 1.771$ V

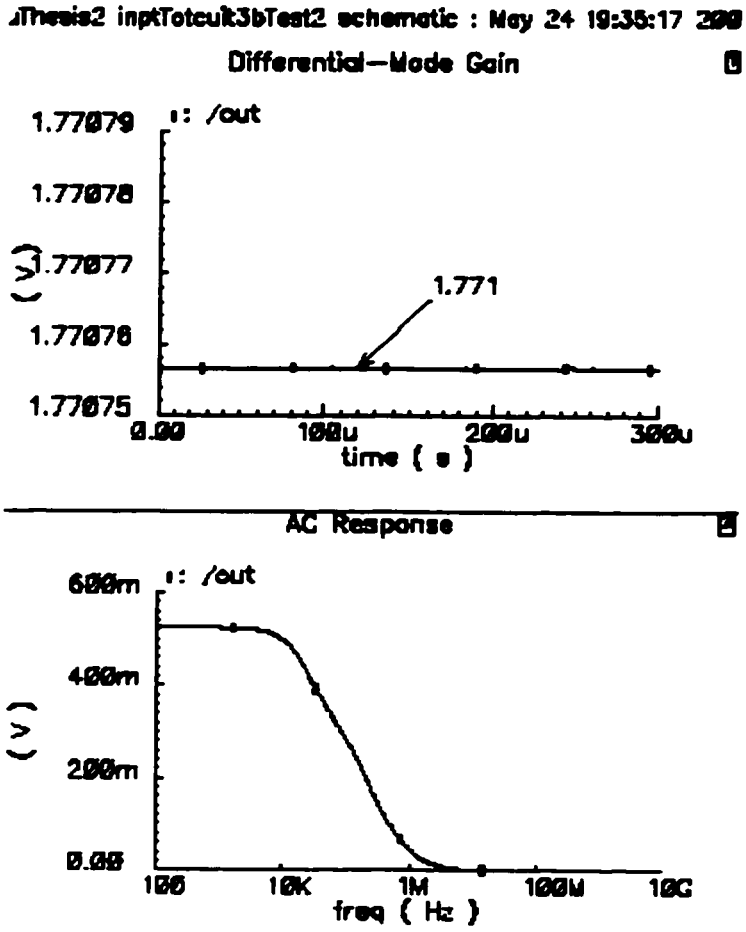
Differential-Mode Gain: $A_{dm} = V_{out} / V_{dm} = 1.771 \times 10^5$

6.4.3 CMRR Calculation

$CMRR = 20*\log(A_{dm}/A_{cm}) = 123.6$ dB

From above analysis we know this CMRR of the proposed op-amp is extraordinarily high, simply because the implementation of level shifter in complementary input stage has made the total transconductance g_m constant.

Figure 6.10 Differential-Mode Gain



6.5 Power Dissipation

In many systems, power dissipation is a critical parameter driving the selection of an op-amp. Sometimes we have to make difficult decisions trading power consumption for required performance. There are some first-order relationships that drive these decisions [21]:

• AC performance: slew rate, bandwidth, settling time – come at the expense of power consumption (increased supply current):

$SR \propto I_{CC}$ $BW \propto I_{CC}$ $t_s \propto I_{CC}$

- Noise figure varies inversely to first-stage current, hence lower noise op-amp requires higher current

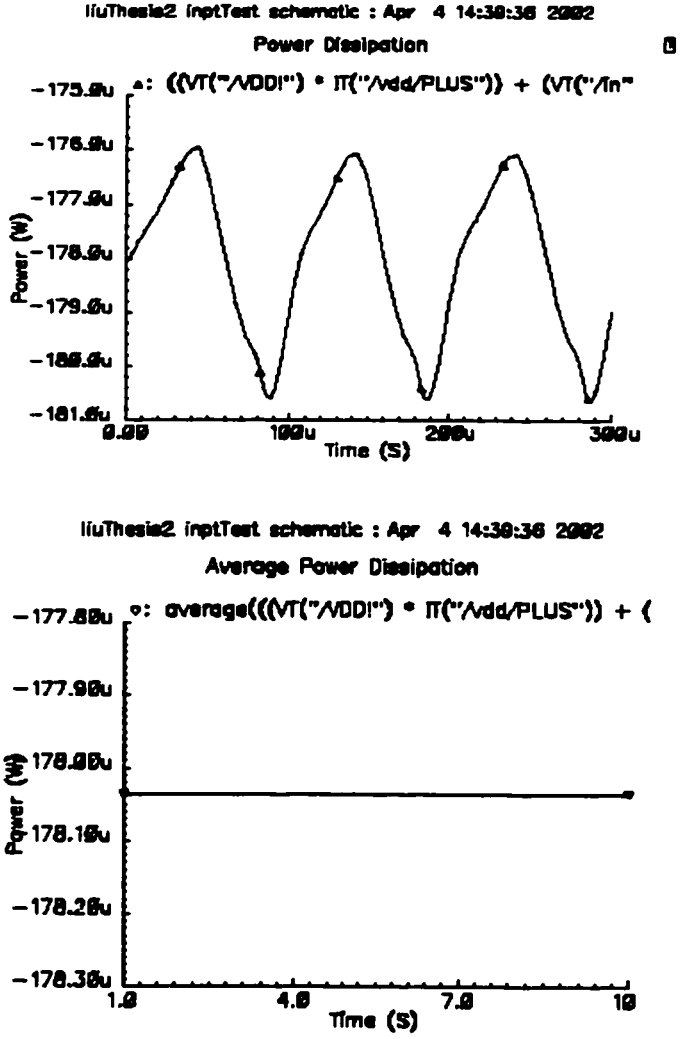
$$V_N \propto 1/I_{CC}$$

- In many op-amp families, output drive is proportional to supply current

$$I_o \propto I_{CC}$$

Making the judicious trade off between "lowest power" and required AC performance, noise or output drive is often among the first decisions a designer must take. Figure 6.11 shows the power dissipation as a function of time, and average power dissipation of the proposed op-amp, which is 178 μw.

Figure 6.11 Power Dissipation & Average Power Dissipation

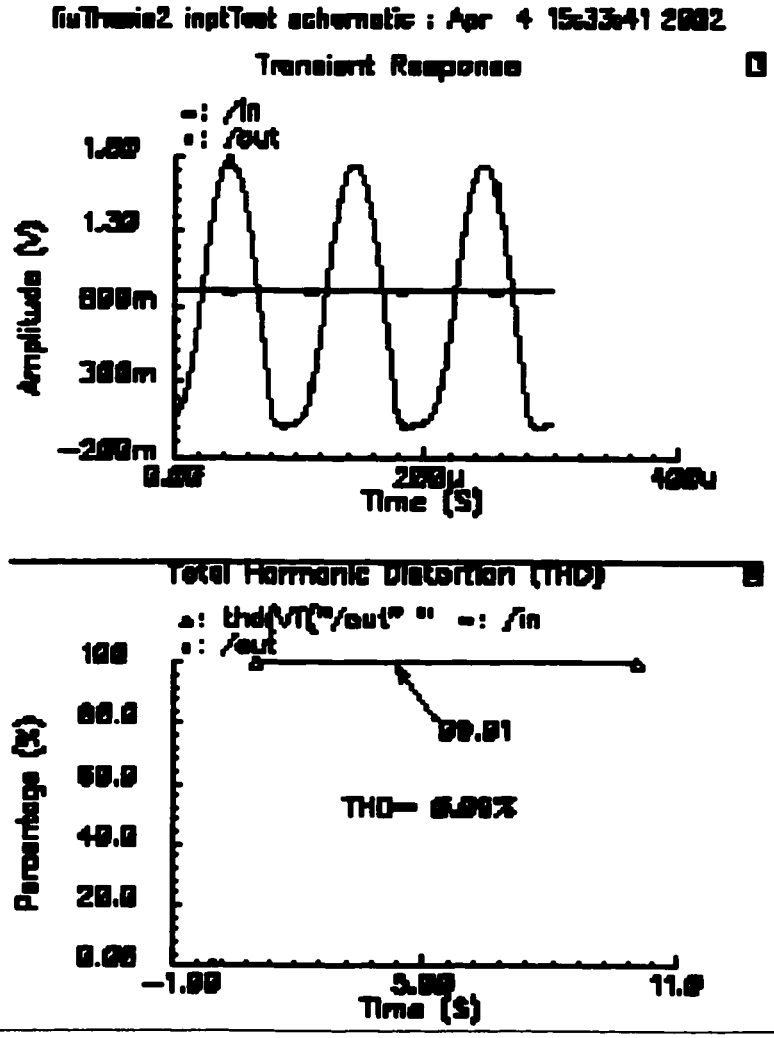


6.6 Total Harmonic Distortion (THD)

Total harmonic distortion (THD) is the ratio of the square root of the sum of the squares (RMS) of the values of the harmonics to the value of the fundamental input frequency. It is expressed in percent (%) or decibels (dB).

THD is a measure of the magnitude and distribution of integral linearity error and differential linearity error. The distribution of these errors may be different, depending on the amplitude of the output signal. Therefore, THD should be specified for both large and small signal amplitudes. Simulation result in Figure 6.12 shows that the THD of the proposed op-amp is 0.09%, which is a quite satisfied figure.

Figure 6.12 Total Harmonic Distortion

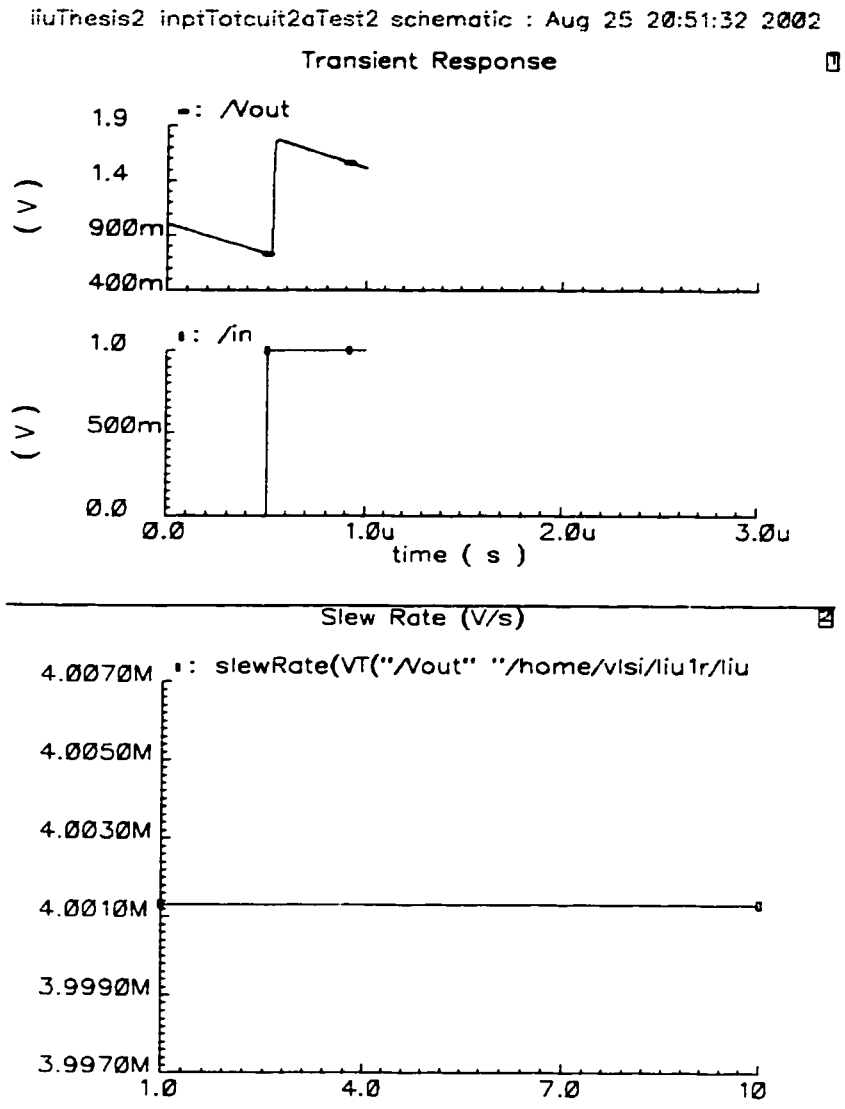


6.7 Slew Rate

The rate of voltage changes as a function of time is called the slew rate: it is used to describe the linearity of the output response of the op-amp over the input signal. The maximum slew rate of an amplifier is often a key specification to its performance. For most design applications, speed is almost always a critical factor, therefore, slew rate and bandwidth need to be maximized and settling time minimized. To do this the value of the compensation capacitor Cc is set as low as possible [5]. However, to provide for proper closed loop stability, the value of this capacitor needs to be increased until adequate phase margin is attained for the desired gain stability point. So this is another tradeoff problem.

Slew rate limitations are first seen as distortions at higher signal frequencies. This is because the output responses of the op-amp become non-linear at higher frequency input signals. This phenomenon can be explained more clearly by Figure 6.13. In this simulation, the square wave input is implemented while the output step response is used to measure the slew rate. The slew rate is calculated and plotted using the calculator function of Candence Virtuoso Schematic Editor, which equals to 4.001V/μs. This figure exceeds the design goal set in Table 2.1

Figure 6.13 Slew Rate Measurement

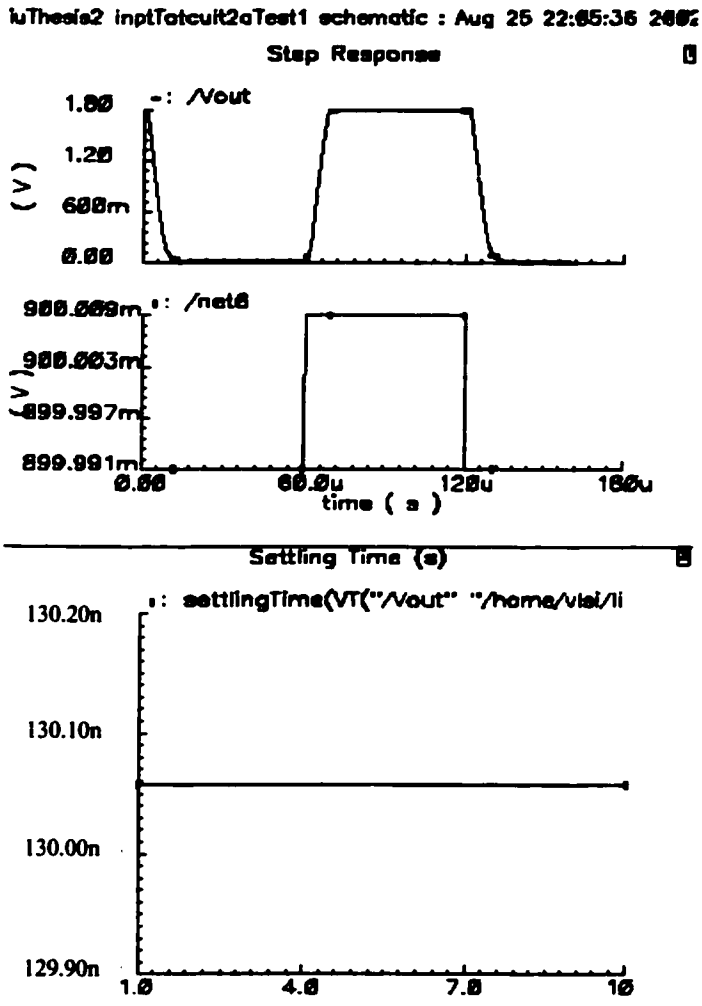


6.8 Settling Time

Settling Time is the time required for the output to reach and remain within a specified error band about its target value. Or more clearly, it is the time between the edge of the applied step function and the point where the amplifier output settles to within some selected percentage of the target voltage value. This percentage is usually 0.1% within the target value [4]. Settling time is the primary measure of dynamic performance of the op-amp.

Similar to the measurement of slew rate, the input signal is square wave and output step response is used to measure the settling time. The bottom plot of Figure 6.14 shows the calculated settling time, which equals to 130ns and meets design goals.

Figure 6.14 Settling Time Measurement

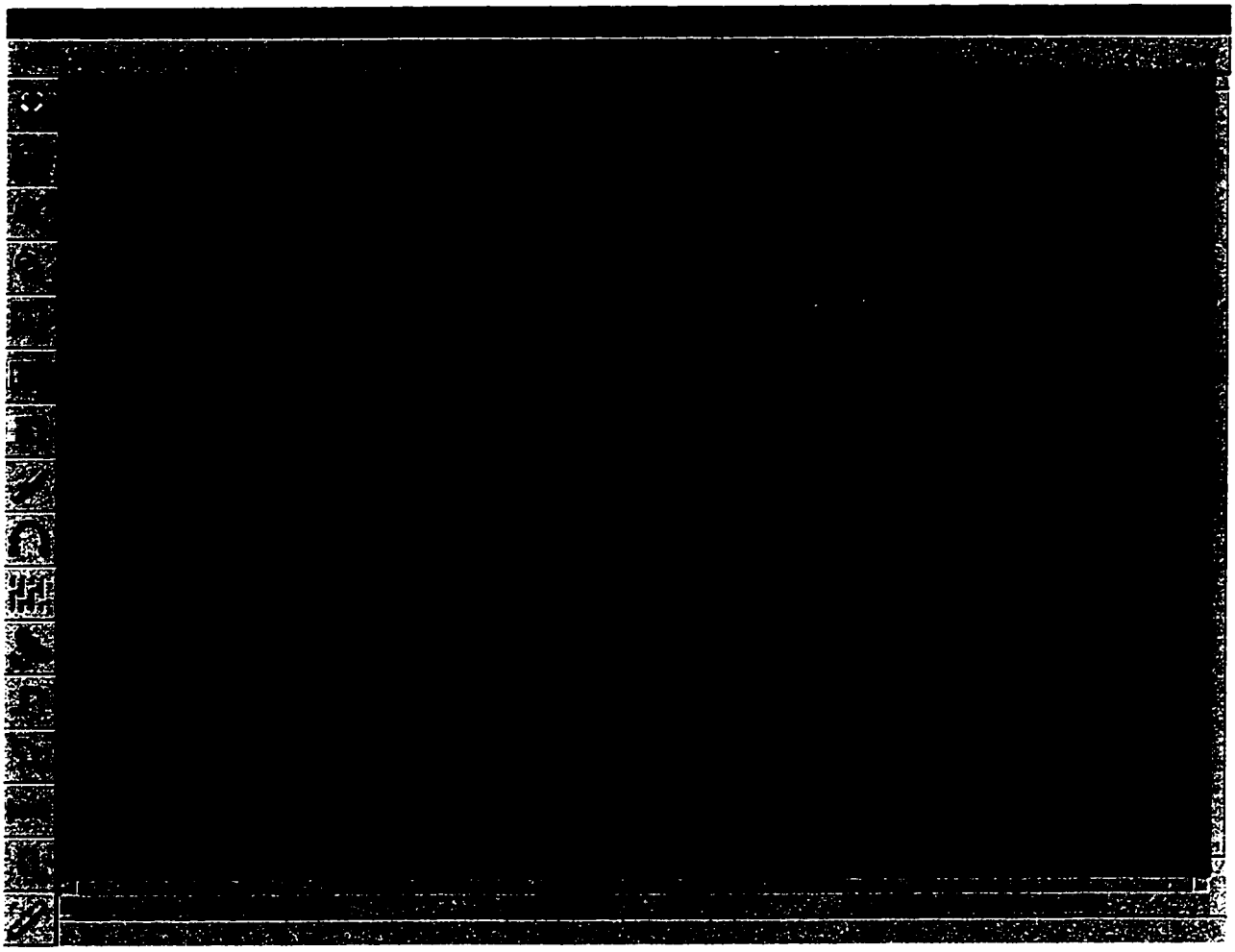


6.9 Final Layout of the Proposed Op-Amp

All previous simulation results, even by the different stages, were obtained based on the final layout shown in following Figure 6.15. This layout has passed the design rule check (DRC) and layout vs. schematic (LVS) check. The core area of this op-amp is 0.08mm^2,

while the total die area is 0.24mm², including pads, power ring and logo.

Figure 6.15 Final Layout of the Proposed Op-Amp



Different from many digital circuits where transistors are automatically generated in layout, in this analog design custom layout is crucial and is implemented throughout the layout in Figure 6.15. Improper layout will lead to significant mismatches and parasitic capacitances which would ruin the sensitive analog nodes, and degrade the circuit performance.

The resistors M10 and M11 (refer to Figure 5.7) were creatively implemented by NMOS with gate connected to drain. This has the advantage of avoid using resistors in CMOS technology which will occupy large die area.

6.10 Specifications of the Op-Amp

The figures in Table 6.1 show the simulation results of the proposed op-amp. Overall, this op-amp has very good results for operating under 1.8V power supply and consume only 178μW of power. The simulation specifications meet the preset design goals in nearly all the performance parameters. As design requirement, both input and output swing reaches rail-to-rail, this has been shown in the simulation results of Figure 6.4. The circuit also has pretty high gain and wide unity gain frequency. As Figure 5.10 depicts, the DC voltage gain attained is around 26.53k (85.5dB) with a gain bandwidth of 10kHz. In Figure 6.7 to Figure 6.10 we calculated the CMRR is 123.6dB, which is also extremely high. The slew rate is 4.001V/μs and 0.1% settling time for a step response is about 130ns, these figures are good enough for a voice signal conditioning. The simulation results prove that the proposed op-amp is well-suited for medium frequency voice signal processing.

Table 6.1 shows the summary of design goals vs. the specifications from simulation.

Table 6.1 Summary of Design Goals vs. Simulation Specifications

Technology: 0.18μm CMOS

Power Supply: 1.8V

Performance Parameters	Design Goals	Specifications from simulation
Output swing	rail to rail	**20mV ~ 1.79V** with a load of R=10k || C=10pF
Total internal power dissipation	<200μW	178μW
0.1% settling time	<150ns	130ns
Slew rate	>2V/μs	4.001V/μs
Voltage gain (DC)	>10K (80dB)	26.53K (88.5 dB)
Gain bandwidth	≥10 kHz	10 kHz
CMRR	>90 dB	123.6 dB
Total Harmonic Distortion (THD)	<0.1%	0.09%
Op-amp die area (Core area) **Op-amp die area (Including pads, etc.)**	**<0.1mm²** **<0.4mm²**	**0.08mm²** **0.24mm²**

Chapter 7

Conclusions and Contributions

7.1 Conclusions

7.1.1 The design of the proposed 0.18μm analog CMOS op-amp represents an advance in the state-of-the-art techniques by extending op-amp design to 0.18μm CMOS technology.

7.1.2 The proposed DC level shifter design methodology presented in this thesis improves the overlapping of the p-pair and n-pair tail currents and makes the variation of g_m as low as within 8%. This relatively constant-g_m makes the frequency response of the op- amp independent from the input common-mode voltage, so that the input range can be rail-to-rail, so as to increase the signal-to-noise ratio.

7.1.3 The proposed 0.18μm CMOS op-amp 32 transistors design has met most of the target design specifications: total internal power dissipation <180μw, slew rate = 4.001V/μs, CMRR= 123.6dB, etc. (See Table 6.1)

7.1.4 Short channel effects [25] and power requirements have lead to the utilization of analog transistors with the channel lengths

ranging from 0.18μm up to 20.5μm.

7.1.5 The op-amp was designed to provide analog signal conditioning appropriate to drive an analog-to-digital (A/D) converter. The A/D converter was represented by a load of 10kΩ resistor in parallel with a 10pF capacitor.

7.1.6 CMC's Design Rule Check (DRC) service checks the problems not flagged by previous local computer (Diva) DRC checking, and identify the nets with antenna rule violations. The proposed layout has been converted into a GDSII (Stream) format and submitted to CMC for DRC checking and has passed the CMC's Design Rule Check. This means the proposed op-amp is ready for fabrication. The application for a grant of fabrication area has been approved by CMC for a fabrication run in the TSMC 0.18-micron CMOS (CMOSP18) technology planned for November 20, 2002 (Run Code: 0206CF).

- The forecast date for shipping the chip is April 2, 2003
- The logo of the layout *ICFWRLIU* was assigned by CMC for fabrication identification

7.2 Contributions

7.2.1 The problems associated with a 0.18μm low-voltage CMOS analog operational amplifier design are:

- Short channel effects makes the design of a constant current source more difficult [22]
- To achieve the best possible signal to noise ratio the circuits must have a rail-to-rail dynamic input range
- Constant-g_m operation is difficult to maintain over the small dynamic range associated with the signal as a consequence of the non-linear properties of the transistor

- The architecture of an operational amplifier can vary radically as the technology feature size decrease

7.2.2 The contributions to solving the problems described in 7.2.1 in this thesis are:

- Current mirrors were used to scale the required bias currents. A relatively constant current source was achieved by using a transistor with a 9.0μm channel length [12].
- By using a rail-to-rail input stage of complementary differential pairs the signal-to-noise ratio was increased.
- The design methodology for the DC level-shifter was enhanced so as to optimize the sizes of all the required 4 transistors, resulting in increasing the ability of level shifting circuit to obtain a relatively constant-g_m (8% deviation minimum).

In previous DC level shifter design methodology [3] only 2 of the 4 transistors' sizes were varied to achieve DC level shifting, while the other 2 transistors' sizes were fixed. In the new DC level shifter design presented in this thesis all the 4 transistors' sizes of DC level shifter are optimized simultaneously to achieve double the ability of the previous DC level shifting circuits.

The simulation results for the proposed design are based on the parameters extracted from the layout in order to achieve maximum accuracy. The final layout is characterized by a fully custom-design to achieve specific functions that cannot be found in standard cells. Large die area has been saved by realizing resistors with NMOS transistors. Many parameters such as power dissipation, THD, slew rate and settling time were obtained using the calculator functions in the Cadence Virtuoso Schematic Editor.

7.3 Suggestions for Future Work

Future work would include the implementation and comparison of measured performance of the physical chip with the design specifications.

The 0.18μm CMOS analog operational amplifier design has been accepted for fabrication and physical testing is required when the hardware implementation is returned from the foundry in April 2003.

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