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Design and implementation of a high speed video digitizer.

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DESIGN AND IMPLEMENTATION OF A HIGH SPEED VIDEO DIGITIZER

by

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ABSTRACT

The Signals And Systems Laboratory in the Electrical Engineering Department at the University of Windsor has conducted research in the area of Digital Image Processing for the past several years. As a result of these research efforts, an Image Processing System has been developed for quality control problems. The first requirement for any Image Processing System is the capability to digitize and store the images in computer memory for further processing. At present, the Digitizer that is being used for this purpose is capable of digitizing a 256X256 image, in about 1 second. The slow speed of the Digitizer essentially limits the overall performance of the system.

This thesis covers the design and construction of a high speed Video Digitizer. The project goal, however, is to develop an electronically sophisticated hardware and software system around the existing hardware of the Image Processing System. The effort is to distribute the design emphasis over the analog, digital and software disciplines utilized in the system. The design is structured to meet the requirements of the image processing executive and also to enable easy operation of the Digitizer.

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Chapter I

INTRODUCTION

1.1 DIGITAL IMAGE PROCESSING

It is estimated that 75% of the information received by a human is visual. The process of receiving and using visual information is referred to as sight, perception or understanding. When a computer receives and uses visual information, this process is called Computer Image Processing And Recognition. Image rather than picture is used in the title because computers store numerical images of a picture or a scene. Processing and recognition refer to two broad classes of techniques that have evolved in this field. Many computer picture processing techniques have been developed and applied only in the last decade. The modern advancement in this field is mainly due to the recent availability of image scanning and display hardware at a reasonable cost and relatively free usage of computer.

Digital Image Processing has got applications in such diverse fields as astronomy, biology, nuclear medicine, law enforcement, industrial applications etc. All these fields share a common need for methods capable of enhancing pictorial information for human interpretation and analysis. In

medicine for instance, physicians are assisted by computer procedures that enhance the contrast or code the intensity levels into colour for easier interpretation of X-Rays and other Bio-medical images. Image enhancement and restoration procedures have been used to process degraded images depicting unrecoverable objects or experimental works too expensive to duplicate. Digital Image Processing is used for machine perception also. Machine perception refers to extraction of information from images in a form suitable for computer processing. Typical problems in machine perception employing image processing techniques can be found in automatic character recognition, industrial robots for product assembly and inspection and finger print identification etc.

1.2 AN IMAGE MODEL

A monochrome image (1) refers to a two dimensional light intensity function F(x,y) where x and y denote spatial coordinates and the value of F at any point (x,y) is proportional to the brightness(or grey level) of the image at that point.

The images that are perceived in everyday visual activity normally consist of light reflected from objects. The basic nature of F(x,y) is characterized by two components. One component is is the amount of source light incident on the scene being viewed, while the other is the amount of

light reflected by the objects in the scene.These components are called illumination and reflectance components and are denoted by $i(x,y)$ and $r(x,y)$ respectively.Thus

$$F(x,y) = i(x,y)\,r(x,y)$$

The nature of $i(x,y)$ is determined by the light source while $r(x,y)$ is determined by the characteristics of the objects in a scene.

The intensity of monochrome image F at Coordinates (x, y) is called the grey level 'l' of the image at that point.

'l' lies in the range

$$L_{min} < l < L_{max}$$

The interval $\{L_{min}, L_{max}\}$ is called the grey scale.It is common practice to shift this interval numerically to the interval {0,L} where l=0 is considered black and l=L is considered white in the scale.All intermediate values are shades of grey varying continuosly from black to white.

1.3 DIGITAL IMAGE

In the form in which they usually occur, images are not directly amenable to computer analysis. Since computers work with numerical rather than pictorial data, an image must be converted to numerical form before processing. A digital image is an image F(x,y) which has been discretized both in spatial coordinates and in brightness. A digital image can be considered as a matrix whose row and column indices identify a point in the image and the corresponding matrix value identifies the grey level at that point.

1.4 SAMPLING AND QUANTIZATION

For digitizing an image, the voltage waveform that is generated by the camera to represent (2) the brightness of a picture element is measured (or sampled) millions of times each second. Each sample is then quantized : it is assigned the number of the nearest step that the system can resolve. Digitization of the spatial coordinates is referred to as image sampling while amplitude digitization is called grey level quantization.

A continuous image F(x,y) can be approximated by equally spaced samples arranged in the form of a N * N array, where each element of the array is a discrete

$$F(x,y) = \begin{bmatrix} F(0,0) & F(0,1) & \cdots & F(0,N-1) \\ F(1,0) & F(1,1) & \cdots & F(1,N-1) \\ \vdots & \vdots & & \vdots \\ F(N-1,0) & F(N-1,1) & \cdots & F(N-1,N-1) \end{bmatrix}$$

grey levels allowed for each pixel. It is a common practice in digital image processing to let these quantities be integer powers of two ;

$$N = 2^{n}$$

$$G = 2^{m}$$

where G denotes the number of grey levels.

The number of bits required to store a digitized image is given by :

$$b = N * N * m$$

The resolution of the image is strongly dependent on both N and n. The more these parameters are increased, the closer the digitized array will approximate the orignal image

The number of samples and grey levels required to produce a faithful reproduction of an orignal image depends on the image itself. As a basis for comparision, the requirements to obtain a quality comparable to that of monochrome TV pictures over a wide range of image types are on the order of 512 * 512 pixels with 128 grey levels. As a rule, a minimum system for general image processing should be able to display 256 X 256 pixels with 64 grey levels.

1.5 ELEMENTS OF AN IMAGE DIGITIZER

A digitizer is a device which converts (3) an image into a numerical representation suitable for input into a digital computer. An image digitizer must be able to divide an image into picture elements and address each individually, measure the grey level of the image at each pixel, quantize that continuous measurement to produce an integer, and write out the set of integers on a data storage device.

To accomplish this, a digitizer must have five elements. The first is a sampling aperture which allows the digitizer to access the picture elements individually while ignoring the remainder of the image. The second element of an image is

a mechanism for scanning the image. This process consist of moving the sampling aperture over the image in a predetermined pattern. Scanning allows the sampling aperture to address pixels in order one at a time.

The third element is a sensor, which can measure the brightness of the image at each pixel through the sampling aperture. The sensor is commonly a transducer that converts light intensity into a electrical voltage or current. The fourth element, a quantizer converts the continuous output of the sensor into an integer value. Typically, the quantizer is an electronic circuit called an analog_to_digital converter. This produces a number that is proportional to the inout voltage or current.

The fifth element of an image digitizer is the output medium. The grey level values produced by the quantizer must be stored in an appropriate format for subsequent computer processing. Technically, the output medium could be omitted if the image were being processed "on line". Image digitizing is frequently done "off-line" from the main computer system, however, and the output medium is necessary. The medium can be magnetic tape or magnetic discs etc.

1.6 DIFFERENT TYPES OF DIGITIZERS

Among the most commonly used (3) digitizers are microdensitometers, flying spot scanners, image dissectors and TV camera digitizers. The first two devices require that the image to be digitized be in the form of a transperency or photograph. Image dissectors and TV cameras can accept images recorded in this manner, but they have the additional advantage of being able to digitize natural images that have sufficent light intensity to excite the detector.

1.6.1 Microdensitometers

In microdensitometers the transparency or the photograph is mounted on a flat bed or wrapped around a drum. Scanning is accomplished by focussing a beam of light on the image and translating the bed or rotating the drum in relation to the beam. In case of transparencies the beam passes through the film ;in photographs it is reflected from the surface of the image. In both cases the beam is focussed on a photodetector and grey level at any point in the image is recorded by the detector based on the intensity of the beam. A digital image is obtained by allowing only discrete values of intensity and position in the output. Although microdensitometers are slow devices, they are capable of high degree of position accuracy due the essentially continuous nature of mechanical translation used in the digitization process.

1.6.2

Flying Spot Scanner

Flying spot scanners also operate on the principle of focussing a transmitted or reflected source beam on a photodetector. In this case, however the image is stationary and the light source is a Cathode Ray Tube in which a beam of electrons, deflected by the electromagnets, impringes on a fluorescent phosphor surface. The beam thereby produces a spot of light that moves in a scanning pattern on the face of the tube. The fact that the beam is moved electronically allows high scanning speeds. Flying spot scanners are also ideally suited for applications in which it is desirable to control the beam scanning pattern externally. This flexibility is afforded by the fact that the position of the electron beam is quickly and easily established by external voltage signals applied to the electromagnets.

1.6.3 Image Dissectors and TV cameras

In image dissectors and TV cameras the image is focussed directly on the surface of a photosensitive tube whose response is proportional to the incident light pattern. Dissector operation is based on the principle of electronic emission, where the image incident on the photosensitive surface produces an electronic beam whose crossection is roughly the same as the geometry of the tube surface. Image pickup is accomplished by using electromagnets to deflect the entire beam past a pinhole located in the back of the

dissector tube. The pinhole lets through only a small cross section of the beam and thus looks at one point in the image at a time. Since photoemissive materials are very inefficent, the time that the pinhole has to look at the point source in order to collect enough electrons tends to make image digitizers rather slow digitizers. Most devices integrate the emission of each input point over a specified time interval before yielding a signal which is proportional to the brightness of the point. This integration capability is beneficial in terms of noise reductions, thus making image dissectors attractive in applications where high signal to noise ratios are required. As in flying spot scanners, control of the scanning pattern in image dissectors is easily varied by external voltagesignals applied to the electromagnets.

1.6.4

Vidicon Tube

Many general purpose TV image digitizers employ a vidicon tube, whose operation is based on the principle of photoconductivity. An image focused on the tube surface produces a pattern of varying coductivity which matches the distribution of brightness in the optical image. An independent, finely focussed electron beam scans the rear surface of the photoconductive target and by charge neutralization this beam creates a potential difference and produces on the collector a signal proportional to the input bright-

ness pattern. A digital image is obtained by sampling and quantizing this signal.

1.6.5 Evaluation

Although standard vidicon digitizers are in general less accurate than the systems discussed above, they have numerous advantages which in many applications outweigh their relative lack of precision. Vidicon systems are the most inexpensive systems in the market. They also have the distinct advantage that the image being digitized can be viewed in its entirety on a TV monitor. This capability not available in any of the systems discussed above is ideal for general purpose applications. Since vidicon systems employ electronic scanning and photoconductive tubes are reasonably efficient, these digitizers are much faster than microdensitometers and image dissectors. They are not as flexible in terms of beam control as flying spot scanners because of the scanning constraints required to produce a video image which can be viewed on a standard TV monitor.

1.7 PROBLEM STATEMENT

The Signals And Systems Laboratory in the Electrical Engineering department at the University of Windsor has developed an Image Processing System. The organization of the image processing system is shown in figure 1.1 It consists of the main computational element (SEL 32/27) a high speed convolution filter, a video camera and a digitizer, colour image display system with touch screen input, colour printer plotter, 32 M Byte hard disk and a 1.2 M Byte floppy diskette, EPROM programmer and system console.

The work was accomplished as a group effort. Each member of the group was assigned a unique job, such as the design of the video digitizer, interfacing the colour printer to SEL computer, interfacing the image display system, design of the convolution filter etc. Finally the individual units were integrated to form the total image processing system. More details about this image processing system are given in the next chapter.

This thesis deals with the design and implementation of the video digitizer. The Video digitizer is the front end of the system. A Hamamatsu C1000 camera is used as the input medium for supplying the analog image. The function of the proposed video digitizer is to digitize the signal supplied by the camera and store the digitized image into the SEL 32/27 memory.

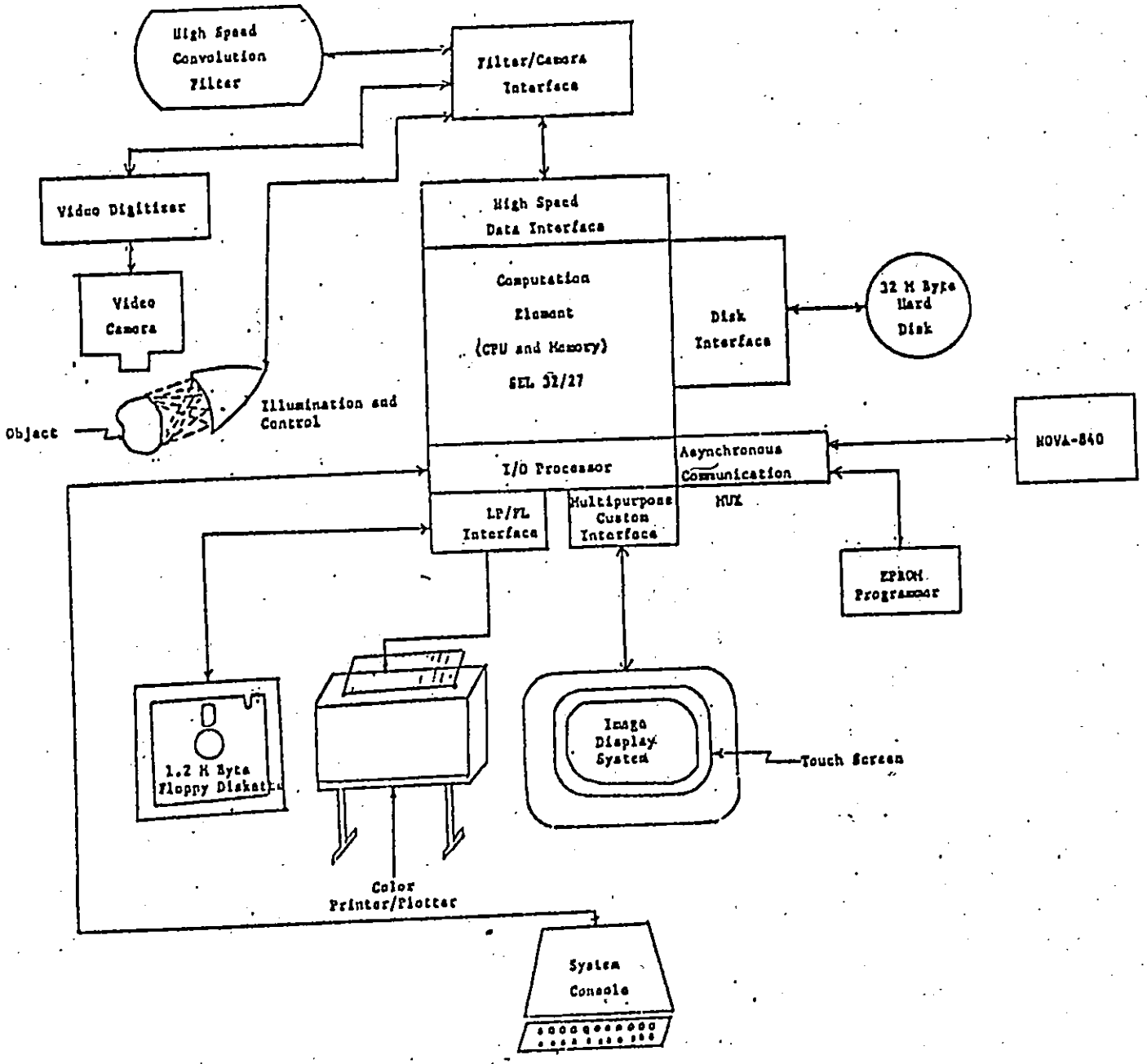


Fig 1.1 IMAGE PROCESSING SYSTEM

The block diagram of the Digitizer system is given in the figure 1.2 .

From the block diagram it is clear that the design of the video Digitizer can be divided into three parts:

(a) Interface between the TV camera and the analog to digital converter.

(b) Interface between the analog to digital converter and SEL 32/27 computer.

(c) Software drivers for controlling the operation of the digitizer.

The interface between TV camera and A/D converter contains hardware which controls the sampling process. It selects the instants of time when sampling should start and when it should stop. Various clock pulses are also generated which control the A/D converter.

The interface between A/D converter and the SEL 32/27 computer has got hardware which helps in storing the digitized image into the SEL 32/27 computer memory. Digitized data is transferred to the host computer through the High Speed Data Interface.

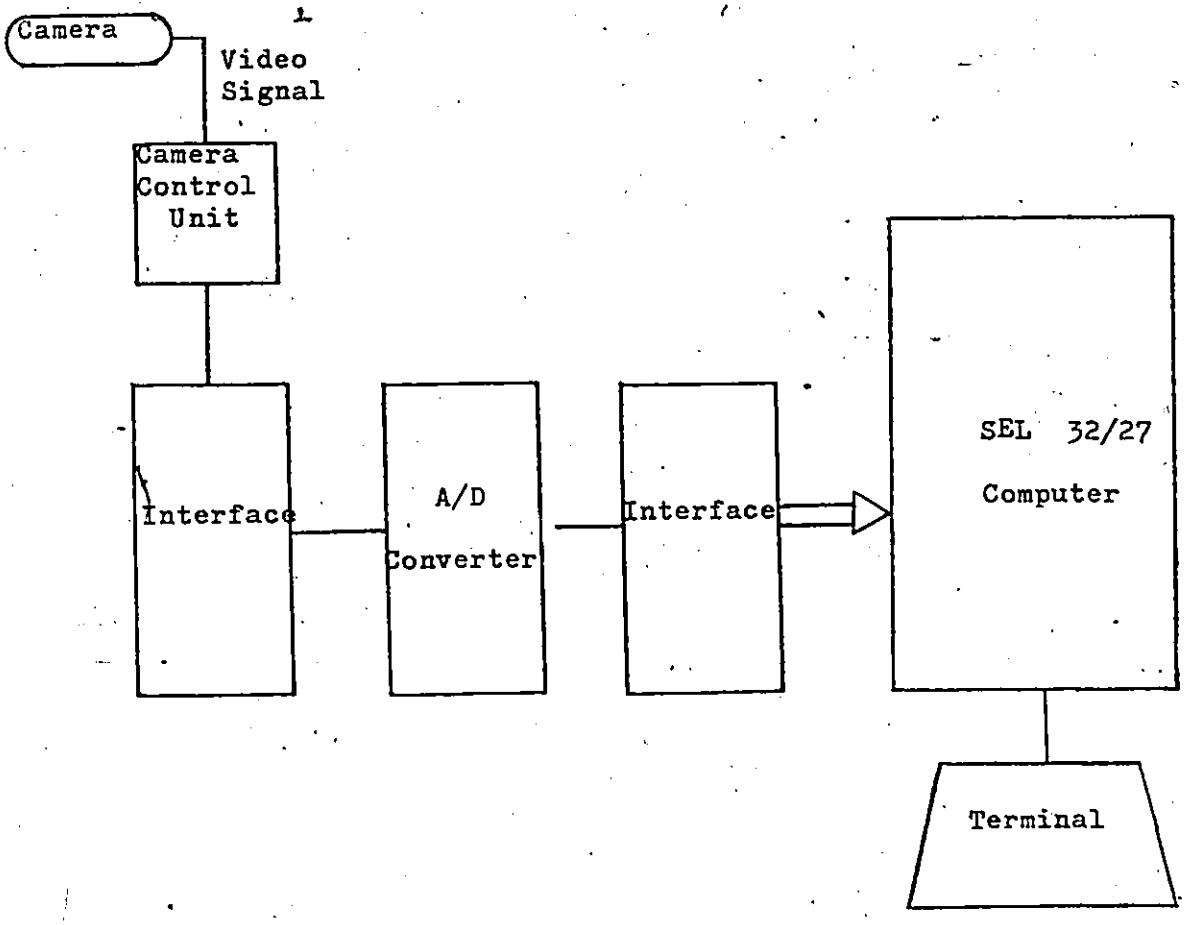


Fig. 1.2 Digitizer Block Diagram

1.8 THESIS ORGANIZATION

Chapter II, describes the working of the Image Processing System. A brief description is given about the various peripheral devices interfaced to the host computer.

Chapter III, gives the description about the Hamamatsu camera. The special features associated with the camera, the working and the controls of the camera are discussed.

Chapter IV, deals with the Video rate A/D converter. The Flash Conversion Technique used for conversion purpose is described in detail.

Chapter V, contains the details about the Camera / A to D converter interface. Important design considerations are discussed. The working of the interface is described with the help of block diagram and the timing diagram of the interface.

Chapter VI, describes the transfer of digitized data from the digitizer to the SEL Computer. A brief description of the HSD interface is included in this chapter.

Chapter VII, gives the summary and conclusions of this work.

Chapter II

IMAGE PROCESSING SYSTEM

2.1 INTRODUCTION

In this chapter, the details of the image processing system developed by the Signals And Systems laboratory at The University Of Windsor, are outlined. The aim of this system is to develop the solutions to quality control image processing problems. The central element of the system is a SEL 32/27 processor, which was chosen because of its large direct memory access, high speed processing power and in particular its high input/output through put rate.

2.2 SYSTEM ORGANIZATION

Figure 1.1 shows the organization of the intelligent image processing system. It consists of the main computational element (SEL 32/27), high speed convolution filter, a video camera and illumination control, colour image display system with touch screen input, colour printer/plotter etc. The SEL 32/27 is the primary computational element of the image processing system and the high speed convolution filter is used for pre-processing the images.

The operation of the image processing system is controlled through system console. The touch screen input can also be used for specifying various functions like digitizing, filtering, display etc. By activating the digitize function from the touch screen or the system console, the image of the part under inspecion is digitized. The convolution filter is used to pre -process the image and is also used for template matching during flaw detection process. The purpose of the image display system is to convert an image stored in a section of the SEL 32/27 memory into either a black and white composite video for a grey level display or to generate R, G and B signals for a pseudo colour display. The display of the processed images of the parts under inspection is of great importance for the developement and verification of various image processing algorithms. An AYDIN 5216 Image display computer has been acquired for this purpose. It has got the capability of displaying a 512*512 image. The display system also has a touch screen input device which allows even a untrained personal to use the image processing system.

The plotter is used to generate hard copies of the images of different parts. A TRILOG 100 colour plotter/printer has been acquired for this purpose. The plotter/printer system can plot images in colour on ordinary paper and also can be used for general purpose printing.

The interface between the Data General NOVA 840 and the image processing system was built to transfer different image procesing algorithms that were developed on NOVA to the mage processing system. The EPROM Programmer is used to program the EPROM's required for implementation of residue arithmetic operations within the convution filter.

2.2.1 SEL 32/27 Mini-Computer

The SEL 32/27 is the basic computational element of the Image Processing System. It consists of a 32-bit processor, 512 K Bytes of MOS Memory, an input/output Processor, 32 M Bytes hard disc drive, 1.2 m Bytes floppy diskette drive, a high speed data interface, interfaces for the Line Printer/ Floppy Disc, Image Display System and a general purpose communication mutiplexer. To facilitate the development of different image processing algorithms a Multitasking Executive (MPX-32), Fortran 77 compiler and an Assembler have also been incorporated into the image processing system.

The SEL 32/27 components are interconnected via two buses, the SEL Bus and the MP Bus as shown in figure 2.1. The SEL bus is a high speed 32-bit synchronous bus that can transfer data at the rate of 26.67 M Bytes per sec. and each module connected to the SEL bus is assigned a unique

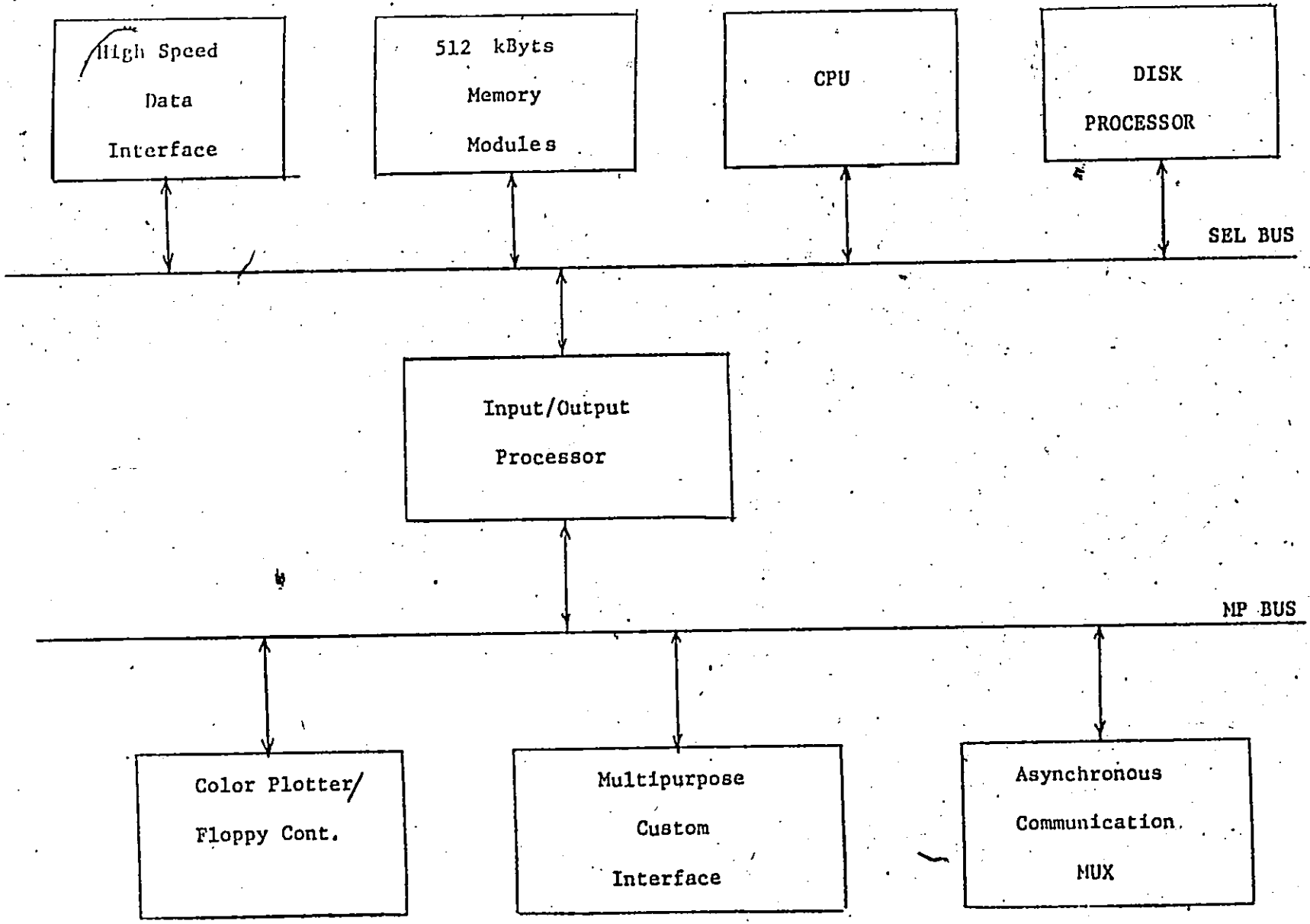


FIG. 2-1 Architecture of SEL 32/27

priority. The Multipurpose (MP) bus is a medium speed 16-bit asynchronous bus that can transfer I/O dta at the rate of 1.5 M Bytes per sec.

2.2.2 High-Speed Convolution Filter

The high speed convolution filter (4) is the 2nd computational element of the image processing system. It is used to pre-process the image of the part under inspection and is is also used for template matching during the flaw detection procedures. The design of the convolution filter is based on the signal and system's group researches into Number Theoretic hardware techniques and is implemented via a 2-D, radix-2 NTT computational element. The entire filter has been constructed with EPROM's, adders, registers, two 128 x 128 word memory buffers and a 128 x 128 word coefficent memory. The filtering operation is performed by taking the NTT of the image, multiplying this by the NTT of the filter impulse response and then taking the inverse NTT of the product.

The Convolution Filter Hardware is organized to compute the circular convolution of an 128 x 128 image with 128 x 128 spatial filter kernel. The linear convolution of the different sizes of the images and the filter kernels have been implemented via software by using the overlap-save technique of sectioned convolutions.

The convolution filter has been interfaced to the SEL 32/27 via the High Speed Data Interface (HSD). Taking into account the I/O rates of the HSD (3.2 M Bytes per sec.) the filter can process an image section of 128 x 128 Bytes in 83.5 ms. This time does not include the overhead of the HSD software handler. Taking this overhead into account and the software overhead of the overlap save algorithm a filtering time of 0.8 sec is required to filter a 256 x 256 image by a 17 x 17 spacial filter kernel.

2.3 VIDEO DIGITIZER

The basic function of the video digitizer is to digitize the image of the part under inspection. A Hamamatsu C1000 special purpose camera is used for gathering the analog image. The camera is specially designed for use with digital computers and image processing hardware. The number of scanning lines in a field is in powers of two i.e. 256, 512 or 1024. The incoming signal from the camera which represents the brightness of the picture at different points, is sampled and quantized. The operation of sampling and quantizing is performed by the A/D converter within the video digitizer. The output of the A/D converter is 8 bit digitized data.

The design of the video digitizer is based on the basic principle that sampling is done only during the periods

when the actual video signal is present, and it is stopped during the blanking periods. The circuitry consists of counters, comparaters, decoders and memory buffers etc. Digitized data is transferred to the SEL 32/27 computer through the HSD interface. Convolution filter and the digitizer share the same HSD interface. This is of little concern since the filtering and the image gathering operations can be mutiplexed without any loss in the computational speed of the SEL 32/27.

The conversion rate of the A/D converter depends on the maximum rate at which digitized data can be transferred to SEL 32/27 computer memory. This rate is 3.3 Mhz. To keep the output digitized data rate below this value, the sampling period has been set to 300 ns. At this sampling frequency, a 256 X 256 image can be digitized in two vidicon scans of the camera or about 33 ms.

2.4 COLOUR PRINTER

The TRILOG COLORPLOT is a unique colour printer (5) capable of plotting in multicolour or Black & White on a plain paper without any toners.It uses a colour ribbon made up of three colour zones Magenta,Cyan and Yellow.The various colours are achieved by interspersing the colour dots and controlling the dot density by software.A typical example

would be the the interspering of the yellow and blue dots to produce a Green tone.The shade of Green(light or dark) that can be produced depends on the dot density of the two primary colours.

The TRILOG COLORPLOT is programmed to plot all the yellow dots first followed by red and blue.The form is reversed after plotting all the yellow dots and again after plotting all the red dots.This arrangement is quite practical and it avoids contamination of colours especially yellow.

Printing is done by a bank of hammers mounted on a moving shuttle. As the shuttle sweeps across the hammers are activated electromagnetically at each position at which a dot is to be printed. The shuttle slows down towards the end of the line and accelerates in the reverse direction,the paper feed moves the paper by one vertical dot row.

2.4.1 Character Printing

The upper case characters are printed by the COLORPLOT as a 7X9 dot matrix.It is possible to plot upto 132 characters per inch. A standard set of 96 character ASCII is stored in a PROM,and is accessed by the received character codes.

2.4.2 Plotting-

The plot mode is selected by the PLOT command and by omitting this the printer will continue to be in PRINT mode. In the Plot mode bits 1 through 6 of each data byte are interpreted as six contiguous dot positions in a dot row. The 7th bit is always programmed as '1' to identify the byte as printable data and it is possible to print upto 100 lots/ inch. It should be noted here that it is not possible to mix character and plot data, except by reversing the form to perform the second operation.

2.4.3 Colour Plotting

The COLORPLOT is capable of producing attractive plots in colour. The colours can be programmed by the user. Before beginning to plot in colour the ribbon drive system initializes by moving the ribbon through a colour boundary crossing. The drive then reverses the direction and during the second pass of the ribbon boundary, the colour code is 'read' and the colour zone in front of the print station is determined. The drive then searches for the colour to be printed as specified by the user's program.

When the required colour zone is in front of the print station, printing proceeds according to the programmed

dot density.In case of multi colour plotting the form is reversed to Top of Form after completely plotting one colour.The three colours (yellow,magenta or cyan) can be specified by the program by their Hex codes.

YELLOW 10H

RED 11H

BLUE 12H

The colour selection is programmed as a single byte line immediately preceeding the plot data for the first line to be printed in that colour.Since the colours printed are opaque the various colours can only be generated by interspersing the dots of the three primary colours.The shades that can be obtained can be controlled by the dot density.

2.5 AYDIN 5216 DISPLAY

The AYDIN 5216 Display unit is a sophisticated computer with its processing ability built around the powerful INTEL 8086 16-bit microprocessor.The standard Firmware provided with the display has an instruction set of (6) largely alphanumeric and graphic instructions which accepts and processes instruction for display. The standard firmware is a powerful display instruction set,but it does not provide its own operating system.The 5216 display computer can be

provided with a second processor card,with an AYDIN supplied or user supplied operating system.One processor card contains the operating system and the other has the standard firmware alphanumeric and graphic display instruction set.In this configuration,the 5216 is a stand alone computer.

Alternatively the operating system may be supplied by a host computer which communicates with the 5216 as if it were a peripheral device of the host.The AYDIN 5216 display computer we are using is interfaced to the SEL 32/27 computer.The standard firmware instruction accepts codes from the host computer and then executes all the necessary code to generate alphanemeric or graphic data on the display monitor.This monitor has a picture resolution of 512 by 512 pixels.Depending on the display hardware configuration upto 256 colours may be displayed on the colour monitor simultaneously.In addition to computer control through coded instructions,another way the 5216 interface with the real world is through its key board inputs.

2.5.1 DISPLAY COMPUTER SPECIFICATIONS

INTERFACING :Two serial interfaces permitting 9600bps data transfer for keyboard or low-speed modems.One 16 bit parallel interface for graph tablets or other devices operating in the programmed I/O mode.

PICTURE STORAGE :Pixel loading into refresh memory via the processor upto 8 bits per pixel in a 512 by 512 format.Less than one microsecond access time to any pixel or 16 bit raster word.

ALPHANUMERIC FEATURES :5 by 7 or 10 by 14 character fronts, special chracters programmed in RAM.

GRAPHICS GENERATION :Special graphic symbols and patterns generated via the processor under software control.

COLOUR OUTPUT :Individual red,green and blue composite outputs having 8 level intensity providing a total of 256 unique colour combinations.The pseudo colour capability and grey level translation is made possible by a RAM lookup table.

SCROLL / ROLL : Simultaneous rolling or scrolling of all selected memory channels by page or within rectangular limits (Destructively or Non-Destructively)

2.6 TOUCH SCREEN

The touch screen digitizer is a new concept in Man / Machine interface that enables untrained personnel to gain access to computer data simply by touching the screen of the

display system with a finger[10]. This eliminates the need to have keyboards, lightpens or joysticks, and permits almost untrained person to work on the system.

The principle of a Touch Screen working (7) is relatively simple to explain. The digitizer measures the touch position by measuring the voltage distribution across a transparent conductive film. Two thin transparent films are mounted in front of a CRT but are kept seperated by an insulating seperator at the edges. When this sandwich is touched one conductive layer is forced in the other yielding an output voltage proportional to the touch position. The voltage is converted to a binary number, combined with similar data from the other axis, filtered, formatted into ASCII characters and transmitted as a serial RS232C message or made available as two 8 bit binary words for paralled interfacing.

There are 5 operating modes of the Touch screen

1. Mode 0 : Inactive

   The touch screen does not do output any information when touched.

2. Mode 1 : Continious output

   The screen outputs position data continuously as long as the screen is touched. The output is updated approximately 60 times per second.

3. Mode 2 : Output on initial touch

The screen outputs data only on the initial touch. The screen touch must be released before any other output is produced. This feature is very useful in the MENU selection where continuous output would overload the host computer with useless data.

4. Mode 3 : ADS regent 40 alignment

This mode is used to align the touch film to an ADDS regent 40 terminal.

5. Mode 4 : Fixed array of 80 touch pads

This mode is not of much significance to us because it uses up the full screen. In this mode the screen is divided in 80 fixed touch pads and only a single ASCII character is transmitted for each pad.

In modes 1, 2 and 3 the touch system produces ASCII characters at the speed set by baud rate.

The message format of the data sent to the host is dependent on the mode selected by the user.

Chapter III

VIDICON CAMERA

3.1 INTRODUCTION

The TV camera has found wide application fields such as in the scietific studies, industrial measurements, on line controls and others because of its orignality in features as an image information inputting eqipment. In ordinary TV cameras, however there has been problems including stability of synchronization, image distortion, drift, shading, interfacing with other devices etc., due to the fact that they have been developed for the purpose of image observation and not for precision image analysis. The HAMAMATSU C1000 vidicon camera system is designed specifically for use with digital and analog computers, high precision and externally stabilized.

For these reasons a Hamamatsu C1000 camera was selected as an input medium for digitizing the pictures. Some important features of this camera are discussed next.

3.2 FEATURES

3.2.1 Timing Control With Clock

All control signals as well as deflection frequencies are controlled by clock frequency of the crystal oscillator, which allows stability in synchronization for high precision and stable measurements.

3.2.2 Image Stability

Within 0.2%. Temperature stability +10 C to +40 C is within 0.2%, which includes the effect of image shift and drift.

3.2.3 Selection Of Scanning Line Number

Selectable from 256, 512, and 1024 depending on the amount of information and processing speed.

3.2.4 Tube Protection Circuit

When the horizontal and/or vertical synchronization fails the circuit provides positive protection to the vidicon.

3.2.5 Level Indicator

A video level indicator is incorporated so that the operator may monitor the quality of the signal.

3.2.6 Frame Blanking

This is to improve the quality of the image in case the intensity of the image is not enough. This is done by controlling the storage time on the photocathode of the image pickup tube.

3.3 CONSTITUTION

The Hamamatsu C1000 vidicon camera system has got two main parts:

(a) Camera Head

(b) Camera Control Unit

3.3.1 Camera Head

The function of the camera head is to produce the video signal. It uses a vidicon type of image sensing tube.

The vidicon is a cylindrical (8) glass envelope containing an electron gun at one end and a target and faceplate at the other. The tube is surrounded by a yoke containing electromagnetic focus and deflection coil. The faceplate is coated on the inside with a thin layer of photoconductor over a thin transparent metal film that forms the target. Behind the target is a positively charged fine wire mesh.

When the light strikes a small area of photoconductor it allows the electrons to flow through, locally depleting the electron charge layer. Thus, if an optical image is formed on the target, the photoconductor will form an identical electron image on the back of the target. As the electron beam scans the target, it replaces the lost electrons, restoring the uniform surface charge. As the electrons are replaced, a current flows in the external target circuit. This current is proportional to the number of electrons required to restore the charge and therefore to the light intensity at that point. It is also proportional to the beam velocity, which in turn determines the time available for the charge to flow. Current variations in the target circuit produce the video signal of the vidicon.

The block diagram of the camera head is given in ref. (8). Apart from the image sensing tube it contains some other circuits such as video pre amplifier, cathode blanking and tube protection circuits, focus and alignement circuits etc. The function of these circuits is to control the position of the electronic beam. A More complete description of these circuits is given in ref. (8).

3.3.2 Camera Control Unit

The function of the camera control unit is to generate the composite TV signal from the video signal generated by the camera head. Also, the CCU controls the operation of the camera head. The block diagram of the camera control unit is given in ref.(3). It contains clock circuits, blanking and sync mixing circuits, shading and landing circuits, power supply etc. More complete description of these circuits is given in (8).

3.4 OPERATION

The cable connection for the camera head, camera control unit, and the monitor is given in the figure 3.1. The important points in the operation of the camera are given below :

3.4.1 Power On-Off Switch

A switch powers the unit. The neon lamp will indicate that the unit is powered.

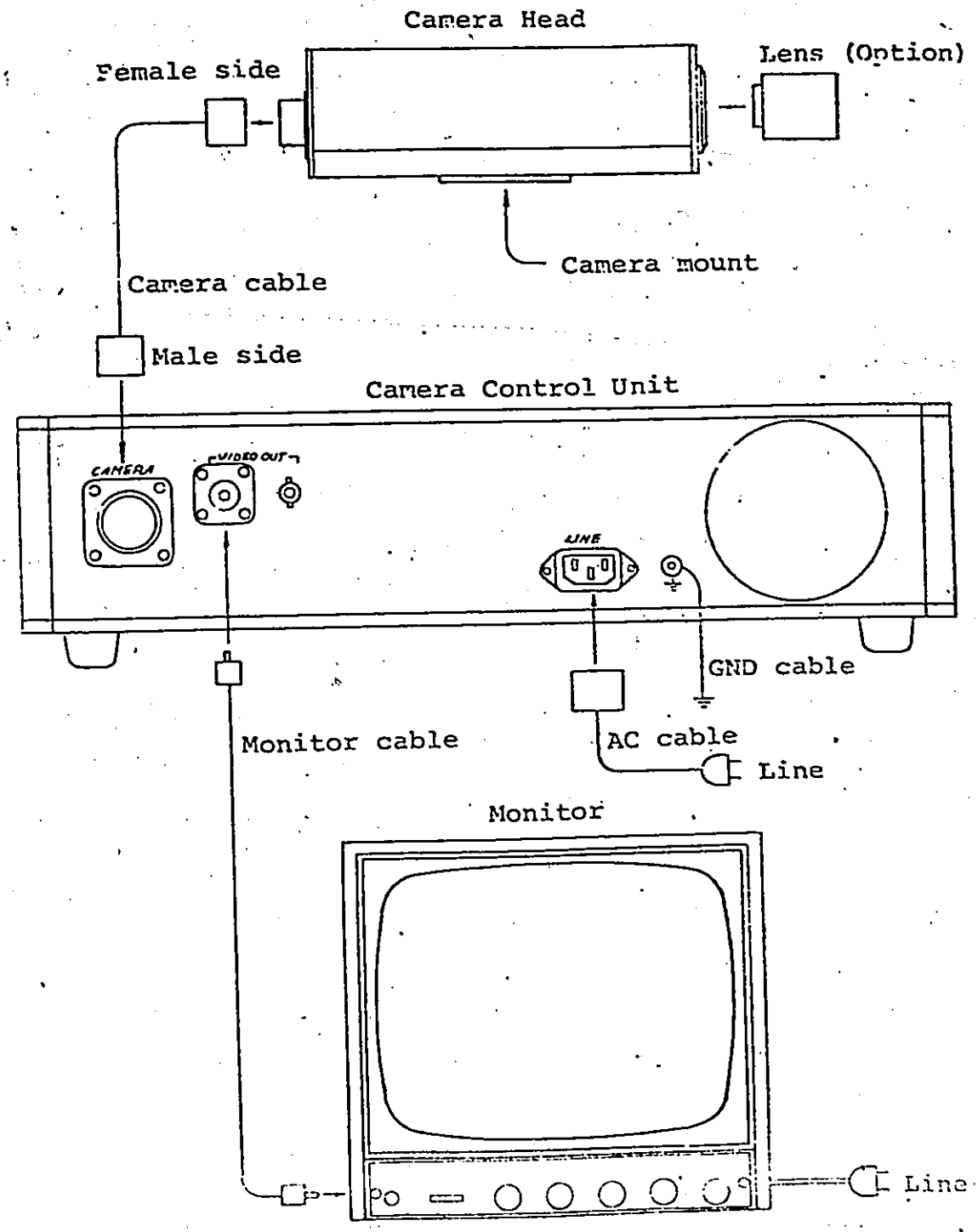


Fig. 3.1 Cable Connection for Camera.

3.4.2 RESO CONTROL switch

Selects number of effective scanning lines.

256 : The scanning line will be adjusted to 256.
Interlace is 1:1

512 : The scanning lines will be adjusted to 512.
Interlace is 2:1

1024 : The scanning line will be adjsted to 1024.
Interlace is 4:1

M999 : This range is used when the unit is equipped with M999 I/O interface to control the unit externally.

M998 : This range is used when the unit is equipped with M998 I/O buffer to control the unit externally.

3.4.3 Beam

Adjusts the beam current of the image pickup tube. In adjustment, this should be set to the point just a little after the negative image on the monitor changes to positive.

3.4.4 Target

By turning this clockwise, the sensitivity of the image pickup tube is increased. The camera should not be used with much too sensitivity otherwise it will result in making burn-in in the tube due to the increase of dark current.

3.4.5 Video Level Indicator

The green side of the LED will light when the amount of input signal to the camera is optimum, while the red side will light when the amount is too much. Both will not light when the amount is too small. The camera should be adjusted within the range where only the green LED is lighting.

Other controls such as target manu-auto switch, picture nor -slice switch, threshold knob, slice post-nega switch, S. position Int-Ext switch etc. are only used if the camera is equipped with some optional modules.

For digitization purpose the most important control is the resolution control switch which sets the number of resoluton lines. Since the desired digitized image should have a dimension 256 X 256, this switch is set to 256.

Chapter IV

VIDEO A/D CONVERTER

4.1 INTRODUCTION

Accurately digitizing analog signals containing high frequencies, demands ultrahigh speed or video A/D converters. Such a converter is essential to diverse uses such as video digitizing, radar signal processing, and high speed data communications. Most video A/D converters work in the 1-to-20 MHz range. But at these speeds, resolution can be a problem. Fortunately, 8 bits and fewer most often suffice in ultrafast A/D applications.

There are many approaches to digitizing a analog waveform. That new devices are being designed using a variety of these techniques (9) is evidence that each offers advantages under certain circumstances. The three methods most often employed at conversion rates exceeding 3MSPS are: the successive parallel approach (also known as the feed forward design), the stage by stage or gray encoder, and the fully parallel or "Flash" converter.

For the design of the video digitizer, a TDC1007J chip was used for A/D conversion. In this chapter, the flash

conversion technique, the configuration of the TDC1007J chip, conversion errors associated with the chip, and a few other video rate A/D converters are described.

4.2 THE CONVERSION TECHNIQUE

The flash encoder is a direct implementation (10) of the analog to digital conversion function. An N bit representation of the analog signal requires division of the allowable input range into 2**N discrete, predetermined levels and development of an N bit digital word indicating to which level the input signal is the closest. This is generally accomplished by determining (2**N)-1 thresholds or cutpoints and determining between which pairs of adjacent thresholds the input signal falls. The flash encoder provides a separate comparator circuit and reference for each threshold and (2**N)-1 digital outputs are combined to produce the desired N bit code. This technique is extremly fast and inherently monotonic, and a number of successful parallel converters have been built in discrete, hybrid, and monolithic form. However, the approach suffers from an exponential growth in complexity with each extra bit added.

Development of alternate conversion methods has been a successful effort to reduce the component count of the converter by performing encoding in stages, adjusting the analog input based on the results obtained in the present

stage such that it can be accepted by a succeeding stage. Dramatic reductions in circuit complexity are realized, but at the expense of considerably more analog circuitry and a reduction in the conversion throughput rate.

A sample of the time varying signal contains information in the measured amplitude and in the time of sampling. Timing errors can be translated into amplitude errors by examining the worst case condition of sampling a full scale sine wave of maximum input frequency at zero crossing, where the slew rate is the highest. The error in percent of full scale, E, due to an error in timing, T, is $E=\pi T \times 100\%$.

Timing errors are called aperture time, and aperture uncertainity or jitter. With an input signal of 5 MHz, total aperture errors of only 64 picoseconds will result in an midscale level error of 1/2 least significant bit (LSB) at 8-bit resolution in addition to static linearity errors. As encoding techniques other than the flash method often require tens of nanoseonds for completion (aperture time), these conversion systems generally include a sample-and-hold circuit which has sufficently small aperture effects and maintains a stable output during the encoding process.

Production of a video sample and hold circuit that does not excessively degrade the input signal is difficult

and its inclusion adds another error source to the conversion system. A flash converter with strobed comparators is in effect a type of digital sample and hold, where the input level is maintained in the digital comparator outputs rather than as a voltage on the holding capacitor. The difficulty in implementing the strobed flash converters is in providing a picosecond matching between (2**N)-1 differential comparators. The small geometries and close component matching of integrated circiutry make such a design practical.

4.3 THE CHIP

The TDC1007J organization is illustrated in figure 4.1. The analog voltage input is applied simultaneously to all comparators, while a separate reference voltage is developed for each in the resistor string between Vrt and Vrb (Reference top and Reference bottom). Vrm, the resistor midpoint tap is provided with a 15-K ohm series resistor Rt to allow a slight adjustment of the midscale point. The 255 comparator outputs are translated into a binary code within the three stage encoder circuitry. The resulting 8 bits are applied to a set of exclusive OR gates controlled by input pins NMINV and NLINV. These signals permit true or inverted binary or two's complement output coding. the output latch holds the data until another conversion is complete.

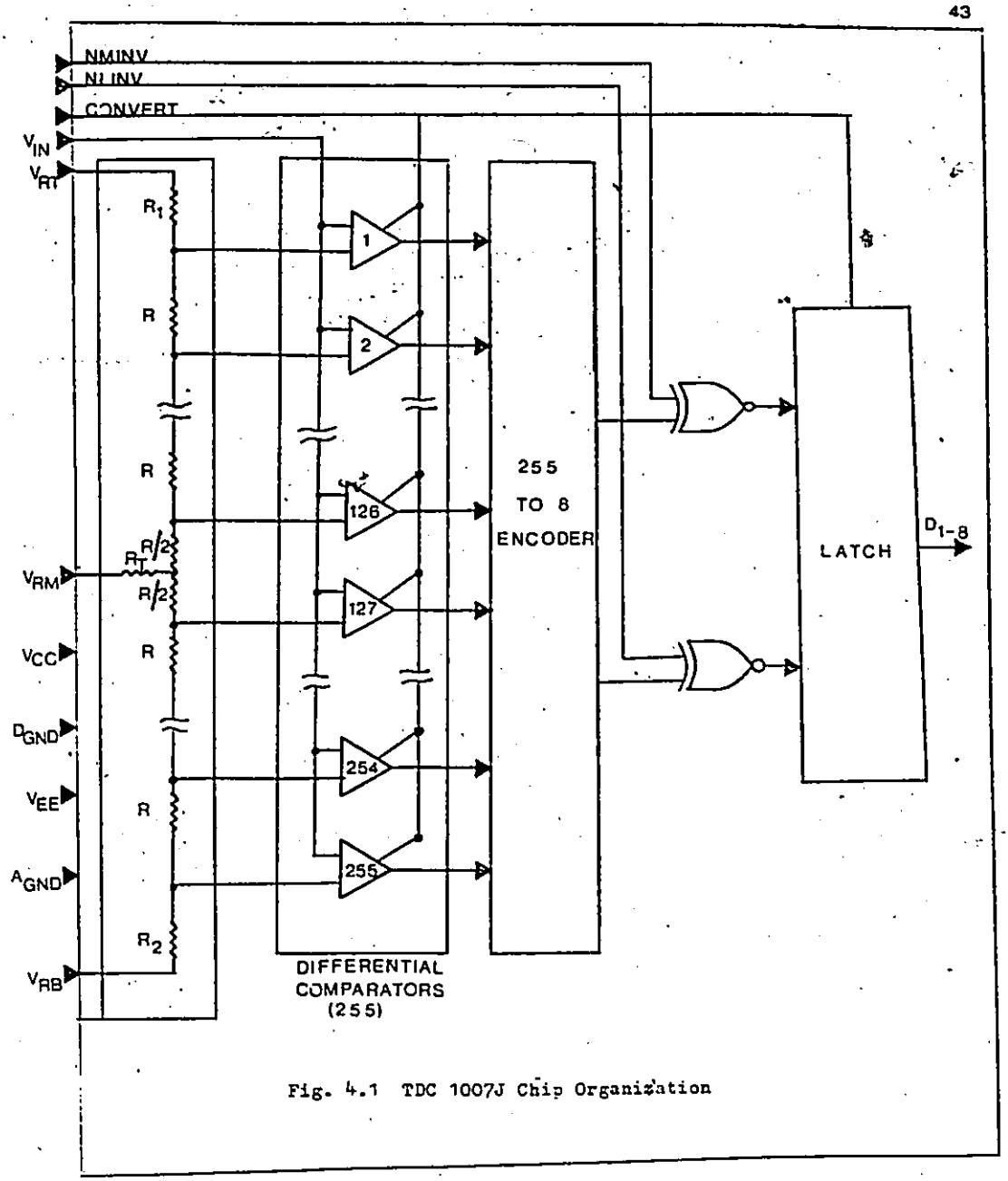


Fig. 4.1 TDC 1007J Chip Organization

The comparators are latched a short time (T delay) after the rising edge of the convert signals shown in the figure 4.2. The 255 to 8 encoding is performed at the falling edge, and the results are transferred to the output pins on the next rising edge, as the next analog sample is latched into the comparators. This pipelining permits the highest possible conversion throughput.

The comparators generate an N-in-255 code, frequently referred to as a "thermometer" code. It presents all ones below the threshold and all zeros above. The desired output code is the total number of ones generated, but such a 255 bit input adder circuit is not efficent from a layout standpoint and would require several pipelined stages. The alternate approach is to locate the unique point where the 1-to-0 transition occurs and mark this with a 1-in-255 signal which is readily encoded to 8 bits in an array of OR gates. The first encoding stage is actually performed by three input

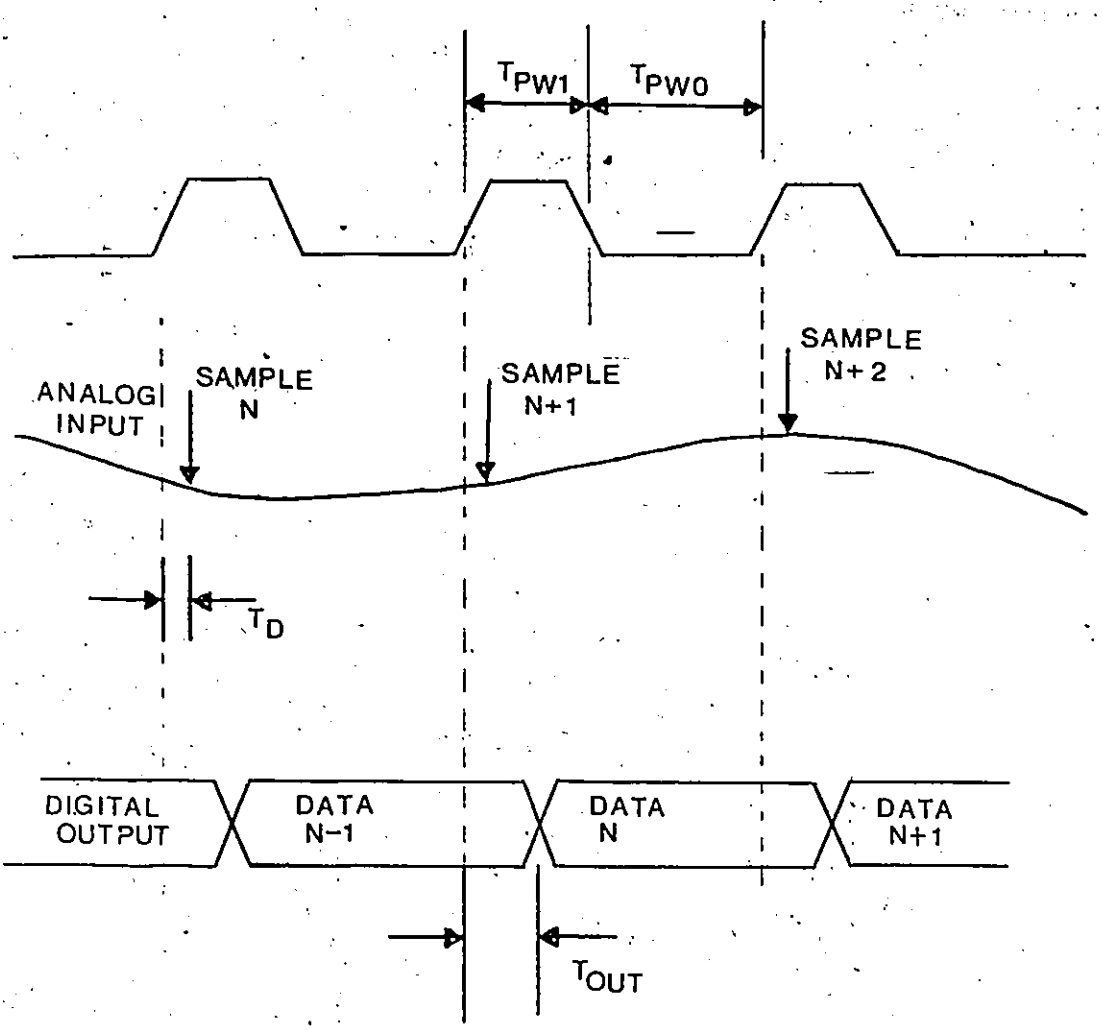


Fig. 4.2 Timing Diagram of the A/D Converter.

AND gates which detect a 1-1-0 sequence to protect against random comparator misfirings within the range of zeros. These gate outputs are latched and held on the falling edge of the convert signal, while comparators are released to acquire the next sample.

OR encoding is performed in two stages: (1) Four 6 bit words are generated and latched on the convert signal rising edge. One of these represents the 6 least significant bits of the eight bit output while the other three are zero. (2) The OR function of these four words plus the two most significant bits indicating which word is non zero appear at the output and are held when the convert signal again falls.

4.4 SUPPORT CIRCUITRY

Two support circuits necessary for the operation of the A/D converter are a voltage reference and a buffer amplifier. The reference is readily generated from a standard fixed or adjustable reference IC buffered with an operational amplifier and emitter follower transistor to sink 35 mA from Vrb at -2 V. This voltage can be adjusted over the range of -1.9 to -2.1 V for full scale calibration or gain adjustment. The symmetrical comparator design provides wide reference bandwidth if dynamic range is required.

An input buffer is required because, though the input capacitance of the comparator circuit is only 1 pF, the total chip input load including other parasites approaches 300 pF. As this value is largely a nonlinear junction capacitance and varies as a function of analog signal level and convert signal state, it must be driven by an impedance of less than 10 ohm, and cannot be employed as a component of an input filter. The buffering requirement is similar to that of driving a 75 ohm cable. The LH0033 hybrid amplifier performs quite well in this application.

4.5 TDC 1019J A/D CONVERTER

The TDC 1019J chip (11) is a 9 bit flash analog to digital converter that contains 511 differential comparators and ECL control circuits. This A/D converter can operate at rates from dc to 25 megasamples per second, sampling large signal components upto 7 MHz without sample and hold circuit. The main reason for seeking higher resolution in an A/D converter is to reduce the quantization error, the error that occurs during the digitization process because each digital output code corresponds to a finite input voltage range.

In a flash converter, one bit of additional resolution requires two times as many comparators. Extra resolution also means that comparator must have more accurate a.c.

and d.c. parameters. In addition noise rejection must be at least double each time the resolution is upgraded by one bit. The TDC 1019J contains 511 comparators and 511:9 encoder. The encoder provides a 9 bit input to a latch that in turn provides a complementary final output of 9 bits. A convert signal controls A/D conversion by strobing all 511 comparators, the 511:9 encoder, and the output latch. For noise reduction and speed, ECL interfaces are used for all digital signals.

Chapter V

TV CAMERA/ A TO D CONVERTER INTERFACE

5.1 INTRODUCTION

In this chapter, the design of the interface between T.V. camera and the A/D converter is discussed. As we know, the voltage waveform generated by the camera represents the brightness of the picture. This voltage waveform is sampled at a very high rate and the samples are then quantized. The operation of sampling and quantizing is performed by the A/D converter. The output of the A/D converter is the digitized image.

The operation of digitizing the image is not as simple as it appears to be. There are several design criteria which have to be satisfied. The voltage waveform generated by the camera not only contains the actual video signal, but it contains horizontal blanking and vertical blanking intervals also. These intervals do not contain any video information. Horizontal blanking and vertical blanking pulses are needed to display the picture on the video monitor. But the aim is to store a digitized image in the computer memory which represents the actual grey levels of the picture. Since the blanking pulses do not represent the grey levels

of the picture, the operation of digitization should be stopped during the blanking intervals.

There are several other such criterion which are discussed in next few pages.

5.2 T.V. CAMERA WAVEFORM

Before explaining the operation of the Digitizer, a few important features of the voltage waveform generated by the T.V. camera are discussed. The shape of the Hamamatsu camera video signal waveform is similar that of the standard NTSC signal. But there are a few differences also. The first major difference is that the number of active lines in a field is 256 as compared to 262.5 in the NTSC signal. The second major difference is that the horizontal line frequency is 16.530 Khz. whereas in NTSC signal this value is 15.750 Khz. The time in which each line must complete its trace and retrace is about 60 usec, whereas in the standard T.V. signal this duration is 63.5 usec.

The active scanning line duration is about 40 usec. During this duration the actual video signal is present. The horizontal blanking interval is about 20 usec. During this interval no scanning is done. This part of the waveform does not represent the actual video signal. On top of the horizontal blanking pulses are superimposed the horizontal

sync pulses. The function of the horizontal sync pulses is to synchronize the scanning lines at the picture tube of the receiver, with that of the camera tube at the transmitter.

At the end of each field occurs the vertical blanking pulses. The frequency of these pulses is 60 Hz. The duration of this pulse is about 1340 usec. The vertical blanking pulse is composed of equalizing pulses, vertical synchronization pulse etc.

The amplitude of the video signal is 1.0 V p-p. Upto 70% of this amplitude is used for transmitting picture information and the rest 30% is used for blanking and synchronization signals. Blanking level occurs at about 0.3 V. From 0.3 V to 1.0 V, actual picture information is present.

If the resolution control of the camera control unit is set at 256, then each frame of the picture contains 256 lines. In this mode the frame frequency and the field frequency are both equal, because each frame is composed of only one field. There is no interlacing. After the camera has scanned 256 lines, a new frame begins.

5.3 IMPORTANT FACTORS IN DIGITIZATION PROCESS

The digital image which is used for image processing, represents the grey levels of the picture. This digital image is obtained from the camera voltage waveform by sampling and quantizing. As discussed in the previous section the camera voltage waveform has got video signal as well as horizontal blanking and vertical blanking intervals. If this waveform is sampled continuosly then the portions which correspond to blanking intervals are also digitized. But this part of the digitized image contains no information about the image and hence it is not useful for image processing.

Thus the first major requirement when the image is to be digitized from the camera voltage waveform, is that the horizontal and vertical blanking pulses should be seperated from the camera signal. When the sampling process begins, sampling is only allowed during the periods when the actual video signal is present. During the blanking intervals which have been seperated from the video signal, sampling process is disallowed.

Figure 5.1 (a) gives the horizontal line scanning diagram and the figure 5.1 (b) shows the vertical retrace scanning. In figure 5.1 (a) starting at point 'a', the electron beam moves to the right until point a' is reached and it has completed one active line. The interval

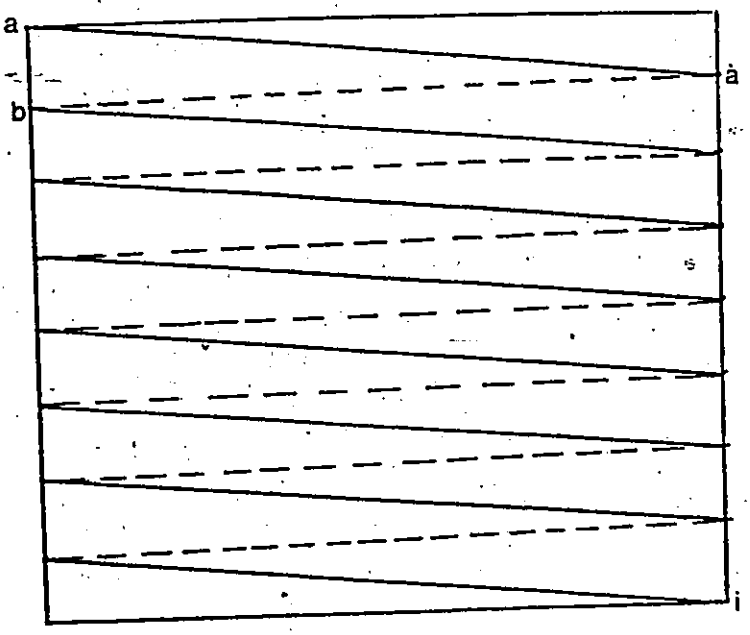


FIG. 5.1(a) HORIZONTAL SCANNING

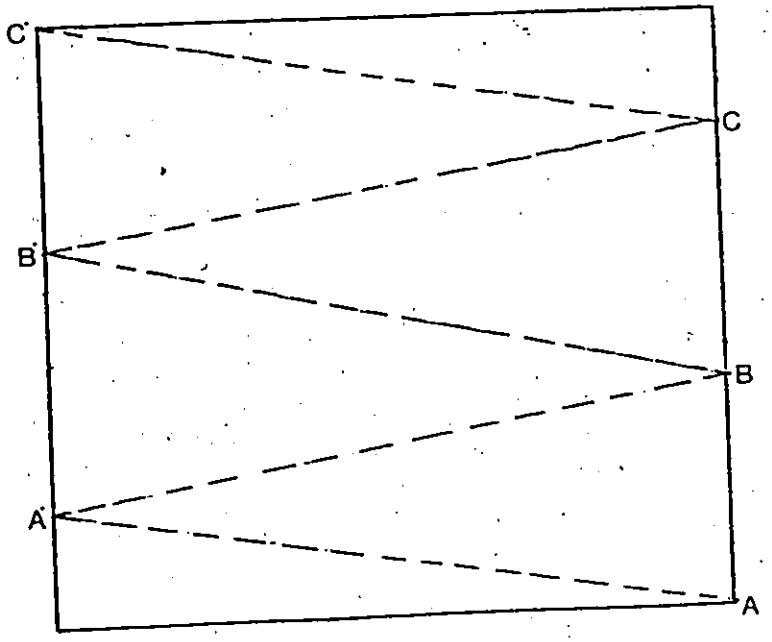


FIG. 5.1(b) VERTICAL RETRACE

from a' to b is called the retrace, or horizontal blanking. In this fashion 256 lines are scanned till the point i is reached. At this point the spot is again blanked out and both vertical and horizontal retrace takes place as shown in the figure 5.1 (b). Upon returning to point c', which is same as point a, all the scanning lines have been traversed and one frame has been completed.

In the figure 5.1 (a), the process of sampling is represented by the symbol 'X'.As shown in the fig, sampling takes place only during the active trace of the line, during the flyback time the sampling process is stopped. Thus the digitized image corresponds to active scanning lines only. During the vertical blanking period also the sampling is stopped and it again begins when the beam reaches the point a.

The number of sampling points on a line depends on the degree of resolution required. For example, in the case of a (256 X 256) image, 256 sampling points are selected on an active line.

The other important factor that has to be considered is the sampling rate or the conversion rate. The aim is to digitize the image as fast as possible. The maximum conversion rate depends on the following two factors :

1) Maximum conversion rate of the A/D converter.

2) The maximum rate at which the digitized data can be stored into the computer memory.

In this scheme of digitization, the conversion rate of the A/D converter is not a limiting factor. The maximum conversion rate of the TRW A/D converter being used for this purpose is 10MHz. Thus we can use sampling frequencies as high as 10MHz which is very fast. But the second factor, namely the maximum rate at which the digitized data can be stored into the computer memory, proves to be the limiting factor. The maximum rate at which digital data can be transferred to the SEL 32/27 host computer is only 3.33 mega samples per second. So the sampling rate at the most can be equal to 3.33 MHz.

When a (256 X 256) image is to be digitized, the resolution control switch of the Hamamatsu Camera is kept at range 256. In this case, each field consists of 256 scanning lines. To digitize a 256 X 256 image, it is required that on each scanning line 256 sampling points be taken. Since each field is scanned in 1/60 th of a second, and each field contains 256 lines and if 256 sampling points are selected on a line, then the whole 256 X 256 image can be digitized in 16.66 ms.

In the case of the Hamamatsu special purpose camera, the time duration of the active scan of a line is about 40 μs. If 256 sampling points are selected on the line during this duration, this corresponds to a samling frequency of about 6.4 MHz. Thus, digitized data from the A/D converter is available at this rate. But the maximum rate at which the digitized data can be transferred to the SEL 32/27 computer is only 3.3 MHz. To avoid this problem a different scheme for selecting the sampling points was developed.

In this scheme the image is digitized in two scans of the camera instead of one scan. During the first scan 128 points are selected on a line. In the second scan, the remaining 128 point are selected on each line. Thus, in two scans all the 256 points are sampled on the line. The obvious disadvantage of this scheme is that total time to digitize the image is doubled.

In figure 5.2, this sampling scheme is illustrated. During the first scan 128 points are selected on each line. These points are denoted by 'X' in figure 5.3. During the next scan, on the same line different 128 points are again selected. These points are denoted by 0. Thus in two scans all the 256 points are selected on the line. It is to be emphasized that the sampling points selected during the second scan should fall exactly in the middle of the points

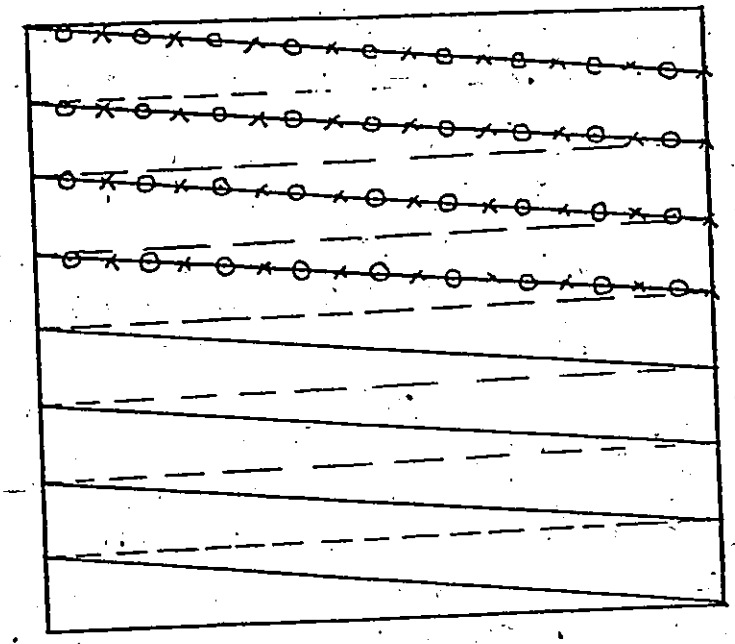


Fig. 5.2 Sampling Diagram.

⊗ Points selected in first scan
O Points selected in second scan

selected during the first scan so that in the final digitized image there are 256 equidistant sampled points on a line. This type of sampling is accomplished through the use of a delay circuit. This delay circuit is operative during the second scan. The delay circuit provides a delay exactly equal to the half of the sampling frequency period, so that the sampling points in the second scan fall exactly in between the sampling points taken in the first scan.

As mentioned earlier the disadvantage of this scheme is that the total time to digitize the image is increased from 16.66 ms to 33.33 ms. Another assumption is that the image would remain stationary during this period. If the picture content changes between the first and the second scan, this type of scheme would give unsatisfactory results.

The third important point which deserves attention during the digitization process is that when digitization should start and when it should stop. Digitization process is controlled through software commands from the computer terminal.

It is to be preffered that sampling should always commence from the beginning of the first line. In this case it is much easier to store the digitized values in proper order and sequence. The process of digitization is initiated

counter. After the second field has been scanned and the digitization process is complete, the next vertical blanking pulse resets the counter and the sampling process stops. Thus, by using the vertical blanking pulses as the reference pulses, the sampling process can be controlled.

5.4 SYSTEM BLOCK DIAGRAM

Based on these design criterion, an interface between the Hamamatsu camera and the the A/D converter was designed. The block diagram of the proposed interface is given in the figure 5.3. All components used in this interface are TTL compatible.

5.4.1 DESCRIPTION

The video signal from the hamamatsu T.V. camera is fed to the blanking pulse separator. The function of this circuit is to separate the horizontal blanking pulses and the vertical blanking pulses from the composite video signal. This circuit was specially designed for the hamamatsu camera, but with slight modifications it can be used with other T.V. cameras also. The circuit consists of Comparators (12), Integrators etc. The outputs of this unit are the horizontal and vertical blanking pulses available at seperate outputs.

The horizontal and the vertical blanking pulses are passed through an inverter. By inverting the vertical blanking pulse, the active field duration is at logic 1 and the

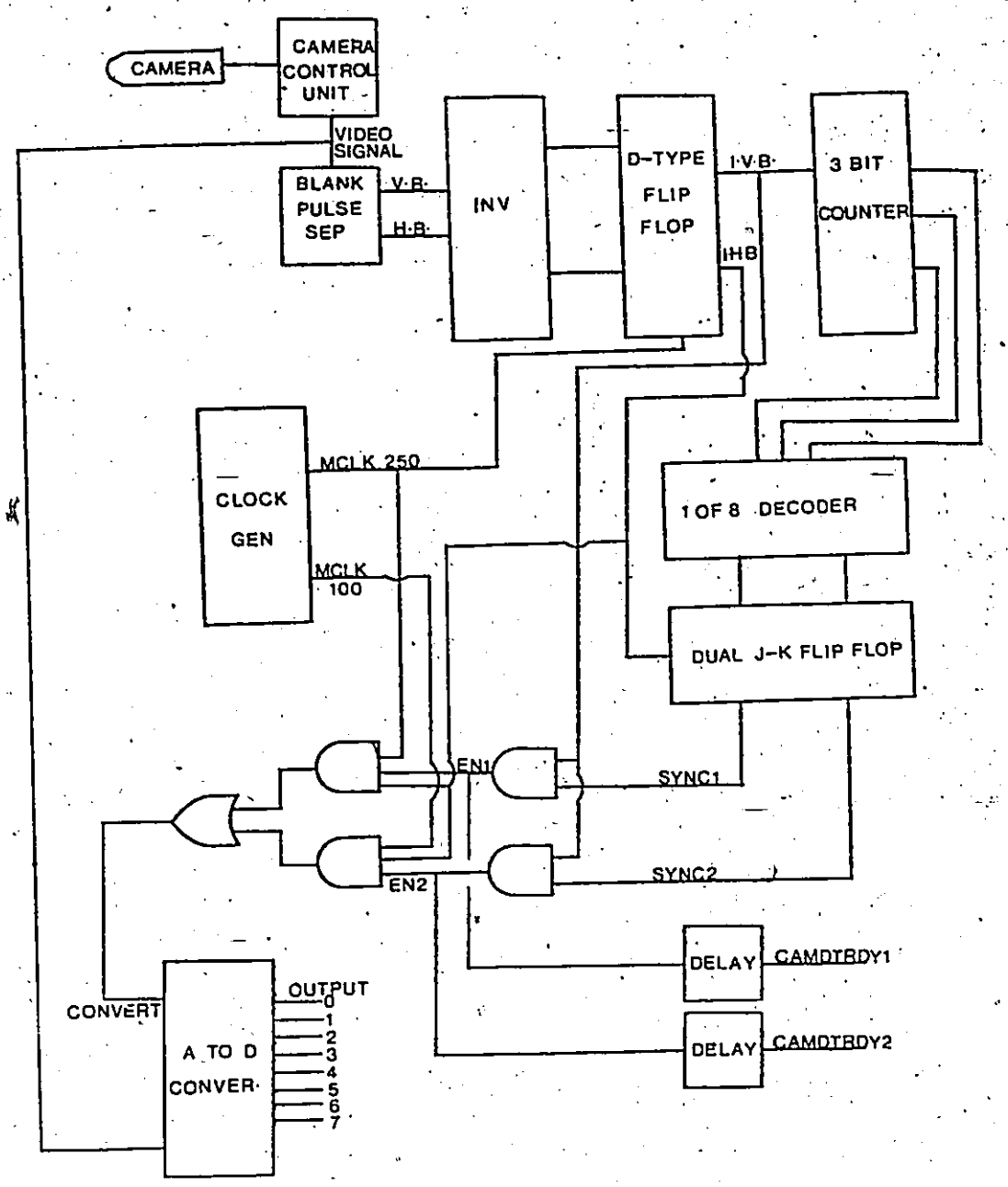


Fig. 5.3 TV Camera A/D Converter Interface.

vertical blanking duration is at logic 0. Thus the rising edge of the inverted vertic1 blanking pulse signifies the beginning of a new field and the falling edge coincides with the vertical blanking duration. Similarly by inverting the horizontal blanking pulse, the active duration of a scanning line is at logic 1 and the horizontal blanking interval is at logic 0. Thus, the rising edge of the inverted horizontal blanking pulse signifies the beginning of a new line and the falling edge coincides with the horizontal blanking period. Let us denote the inverted vertical blanking pulses and the inverted horizontal blancing as I.V.B. and I.H.B. respectively.

A LS74124 chip (13) is used to generate the system clocks. In total six clock pulses are generated. The time period of the clock pulses is 300nS and each clock pulse is delayed by 50nS from the preceding clock pulse. The rising edges of the I.V.B. and I.H.B. are synchronized with the rising edge of MCLK 250 in a synchronizing circuit. A dual D type flip flop is used for this purpose.

The process of digitization is controlled through a counter and decoder logic. The synchronized I.V.B. is fed to a 3 bit counter. This counter is triggered by the rising edge of the input pulse. After the command for digitization is issued by the systen the counter is reset and and it

starts counting the I.V.B. pulses. The output of the counter is connected to a 1 of 8 decoder. Because the counter is triggered by the rising edge of the I.V.B., therefore the count is advanced by one with the starting of every new field. After receiving the digitization command the counter is reset and the output of the counter remains zero until it encounters a rising edge. This takes care of the condition that digitization should not start in the middle of the field but only at the beginning of a new field. When the counter counts one the corresponding output of the 1 of 8 decoder is active. This active signal is used to initiate the digitization process. To ensure that sampling should start from the starting of the first line, the output of the decoder and the rising edge of the I.H.B. are synchronized. This is done by using a J K flip flop. Output of the 1 of 8 decoder is fed to the J input of the flip flop and inverted J signal is fed to the K input. I.H.B. is connected to the clock input. The output of the J K flip flop goes high when the output of of the decoder goes high and at the rising edge of the I.H.B. i.e. at the beginning of the first line. Because the image is to be digitized in two vidicon scans or two active fields, therefore two consecutive outputs of the 1 of 8 decoder are used. When the second field begins the 1 of 8 decoder output corresponding to the previous field goes inactive and the next output line corresponding to the second field goes active. This is also synchronized to the

I.V.B. These two signals are denoted by SYNC1 and SYNC2 respectively. SYNC1 and SYNC2 signals are connected to an AND gate. The other input of the AND gate is the I.V.B. signal. The outputs of the AND gate are called the ENABLE1 and ENABLE2.

To store the digitized image data in the computer memory through the HSD interface, two signals are needed which inform the HSD at appropriate times that the digitized data is ready. These two signals are called CAMDTRDY1 and CAMDTRDY2. CAMDTRDY1 is active low while the digitized data from the first scan is being transferred and CAMDTRDY2 is active when the digitized data from the second scan is being transferred. These two signals are derived from the ENABLE1 and ENABLE2 signals. ENABLE1 and ENABLE2 signals go high at the starting of the first line and these remain high during the entire duration of the field. Thus the sampling process starts when the ENABLE signals go high. But the A/D conversion process involves some delay therefore the digitized data is not available immediately after the ENABLE signal goes high. Thus CAMDTRDY1 and CAMDTRDY2 signals are obtained from the ENABLE signals by providing appropriate delays.

ENABLE signal goes high at the starting of a new field and it remains high during the entire duration of the

field. But the A/D conversion should only take place during the active duration of the line and it should stop during the horizontal blanking interval. Thus, the convert signal for the A/D converter should be present only during the active duration of the line. The convert signal is obtained by connecting the ENABLE signal, I.H.B. and the sampling clock to a triple input AND gate. Two AND gates are needed to derive the two separate convert signals for the two scans. In the first scan MCLK250 is used as the sampling clock. In the second scan because it is required that the sampling points should fall exactly in the middle of the sampling points selected during the first scan, therefore MCLK100 is used as the sampling clock. MCLK100 is delayed by 150 nS from the MCLK250. The convert signal for the A/D converter is obtained by connecting the CONVERT1 and CONVERT2 signals to an OR gate and then the output of the OR gate is the CONVERT signal.

The CONVERT signal is connected to the convert input of the A/D converter. The composite video signal from the camera is connected to the analog input of the A/D converter. The digitized image data is available on the output lines of the A/D converter.

The circuit diagrams for the interface are given in the Appendix.

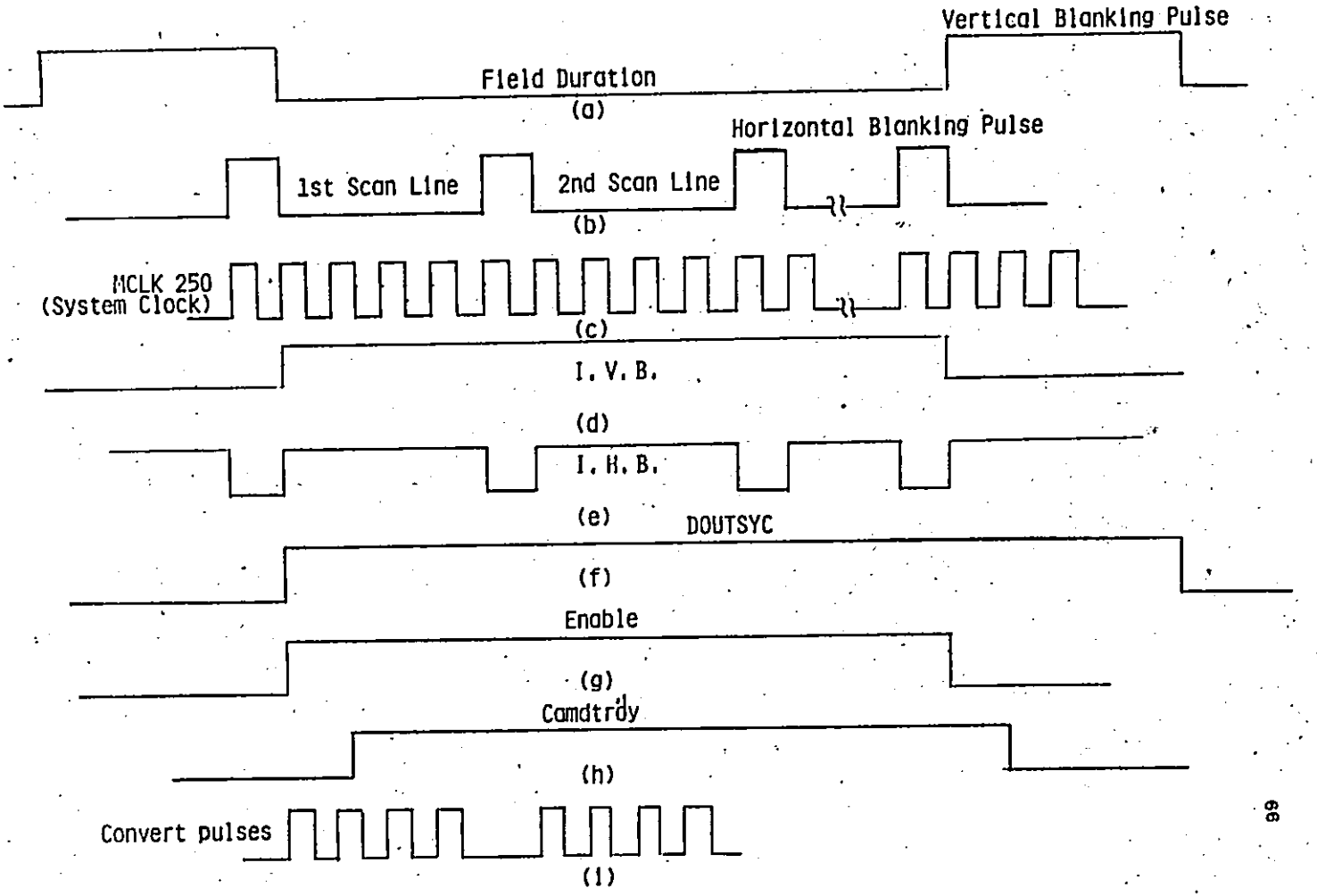


Fig. 5.4 Timing Diagram

5.5 TIMING DIAGRAM

The timing diagram for the interface between the Camera and the A/D converter is given in figure 5.4. The vertical blanking pulses and the horizontal blanking pulses are seperated from the video signal. In this diagram the vertical blanking pulses and the active duration of the field are given in (a). The horizontal blanking pulses and the active scanning line are swown in (b). MCLK 250 is used as the system clock. Inverted vertical blanking pulses and the inverted horizontal blanking pulses are synchronized to MCLK 250. The decoder output goes high at the beginning of a new field and it remains high until a new field begins. The decoder output is synchronized to I.H.B. This signal is denoted by DOUTSYC in the figure.

ENABLE signal is derived from the DOUTSYC. This signal remains active during the entire duration of the field in which sampling has to be done. CAMDTRDY is derived from the ENABLE signal by delaying the ENABLE signal. The delay period is equal to one clock period. This delay is needed because the digital output from the A/D converter is available only after about one clock period from the start of sampling process. CONVERT signal for the A/D converter is generated from ENABLE signal by disallowing the sampling pulses during the horizontal blanking intervals. In the first scan MCLK 250 is used as the sampling clock and in the second scan MCLK 100 is used for this purpose.

Chapter VI

DATA TRANSFER FROM DIGITIZER TO SEL COMPUTER

6.1 INTRODUCTION

The digitized video data from the digitizer is transferred to the computer through a High Speed Data (HSD) interface. HSD interface allows data transfers at a much higher rate than the RS 232 interface. This chapter gives a brief description of the HSD interface and also the complete details of the interface between the HSD and the Video Digitizer.

6.2 HSD OVERVIEW

The high speed data interface (HSD) (14) is an optional feature for the SYSTEMS 32 SERIES computer. It provides a full 32-bit parallel interface to a customer designed device at rates upto 834 K transfers per second.

The handler design is based on the notion that the HSD hardware acts as a controller : it performs the handshaking with the CPU and performs all SELBUS operations needed to fetch and store either the data or status relating to the required operations. Therefore, references to the HSD simply imply controller functions which are generic to I/O operations in general. The device attached to the HSD is

user addition. The general assusmption about the device is that it can source and/or synchronize data with the possibility of presenting device specific status on request.

Some important points about HSD :

1. High speed data transfers upto 834 words per second. Each word is 32 bits. So effective data transfer rates of 834 * 4 bytes/sec.
2. Upto 64 K transfers per block.
3. Simple handshake protocol between HSD and customer designed equipment
4. External mode capability which allows the customer device to provide both memory address and data for each trasfer.
5. Automatic status posting.
6. Intercomputer link capability.

6.2.1 Functional Description

The HSD is essentially divided into three functional parts. The first part consists ofaspecial SELBUS interface which allows overlapped CPU and memory communications to and from the HSD. The second part consists of a simple 32-bit bidirectional data bus and the appropriate handshake control signals to interface the HSD to a customer designed device interface. The third part consists of appropriate internal storage registers and sequential control logic for controll-

ing the data flow internal to the HSD, to and from the SELBUS, and to and from the customer handshake interface.

Typical block transfers are initiated by setting up an input / output command list (IOCL) which consists of one or more input /output command blocks (IOCB), and then issuing a command device (CD) start I/O (SIO) instruction. The above functions cause the HSD to fetch the contents of the first (IOCB) by using a pointer in the transfer interrupt TI dedicated location. Each (IOCB) contains the operation code (which is also sent to the device), the transfer count, the memory buffer address, and space to post error or device status when required.

The HSD controls all the data transfers until the transfer count reaches zero, or an error has occured. The service interrupt (SI) status is then automatically posted in the TI dedicated location, and an SI is generated. An error will cause the error status to be automatically posted in the current IOCB before normal SI status posting.

Automatic status posting eliminates the need for test device (TD) instruction except to determine whether the HSD is present in the system. When the HSD is placed in the external mode, each data transfer must be preceded by the transfer to the appropriate memory address from the customer

device to the HSD. The customer device has got complete control of HSD operations while the HSD is in the external mode.

The following discussion provides a brief description of the macro level instructions used to control and obtain status from the HSD.

6.2.2 Command Device (CD) Instruction

The command device (CD) instruction is the basic macrolevel instruction used to initiate and terminate the HSD operations.

All combinations of the command device instruction require status to be returned to the CPU by an advanced read status (ARSTX) read status (RSTX) bus sequence. The HSD will always return an all zero status word and will essentially ignore all illegal command combinations

6.2.2.1 Transfer Address Word (TAW)

The transfer address word is a 32 bit word used with the command device initialize data transfer instruction. The TAW provides the memory address of the first input / output command block. The TAW is provided in a dedicated memory location for the HSD interface.

6.2.2.2 Test Device (TD) Instruction

The test device (TD) instruction is used only to determine whether the HSD is connected to the system. If HSD is off-line or is not plugged into the system, execution of a TD 8000 will set all four condition code bits to one. If the HSD is plugged in and on-line, the execution of any TD will result in condition code bits of all zeros . Therefore the TD should only be used to determine whether HSD is present in the system .

6.2.3 Input / Output Command Block (IOCB)

The input /output command block (IOCB) consists of four 32 bit words generated by the software system . The four words of the IOCB contain the operation code, transfer count, memory buffer address or device dependent command, and the error/device status . Figure 6.2 illustrates the format of the IOCB .

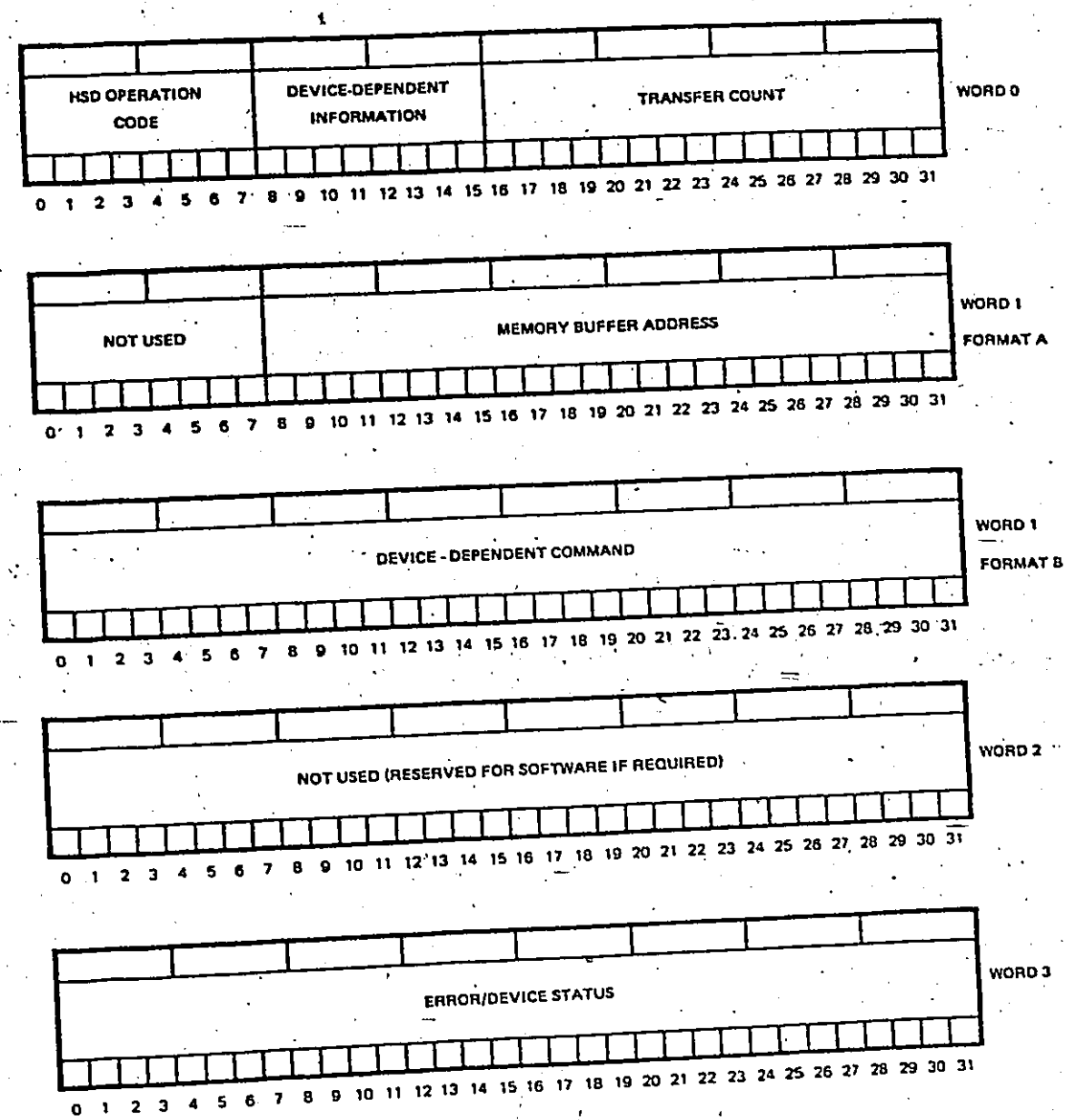


Fig 6-1 Input/Output Command Block (IOCB) Format

6.2.3.1 HSD Operation Code

HSD OPERATION CODE

BIT	
0	When set indicates input transfer, reset for output
1	Command transfer, word 1 of the IOCB is sent to the device
2	Device status request, store into word 3 of the IOCB
3	Continue on error
4	Interrupt, when completed processing IOCB
5	Transfer in channel ; that is, branch to specified IOCB
6	Command chain, that is, execute next IOCB
7	Data chain, continue transfer with address and count specified in the next IOCB

6.3 DATA TRANSFER FROM VIDEO DIGITIZER

The 8 bit video data from the A/D converter is transferred to the SEL computer through the HSD interface. The Digitizer and the convolution filter share the same HSD interface. The filtering and the image gathering operations can be multiplexed without any loss in the computational speed of the SEL computer.

6.3.1 HSD/FILTER INTERFACE

Figure 6.3 shows the block diagram of the interface between the HSD and the filter. The interface part consists of Line Drivers/Receivers, Input And Output Buffers, Mutiplexers/Accumulators, an 18 bit NTT stage and butterfly counter, logic for control of all input/output operations and generation of the system clock and the timing signals. The logic for the control and accumulation of the digitized image from the video digitizer has been built in this interface.

The interface logic is controlled by signals from the HSD. The Filter Function Register within the interface can be loaded from the HSD to specify the next filter function (Load Image Data, Load Coeff. Memory, Send Camera Data, etc.). Once a filter function has been specified the data between the HSD and the filter is transferred asynchrously at a rate of 834K, 32 bit words per second. The 8 bit data from the Video Digitizer is accumulated to form a 32 bit word and this accumulated data is transferred to the HSD in a pipeline.

The NTT Stage/Butterfly Counter has been designed to serve a dual purpose. During the transfer of data between the filter and the HSD it is used to count the number of Pixels and during the convolution operation it serves as a stage and butterfly counter.

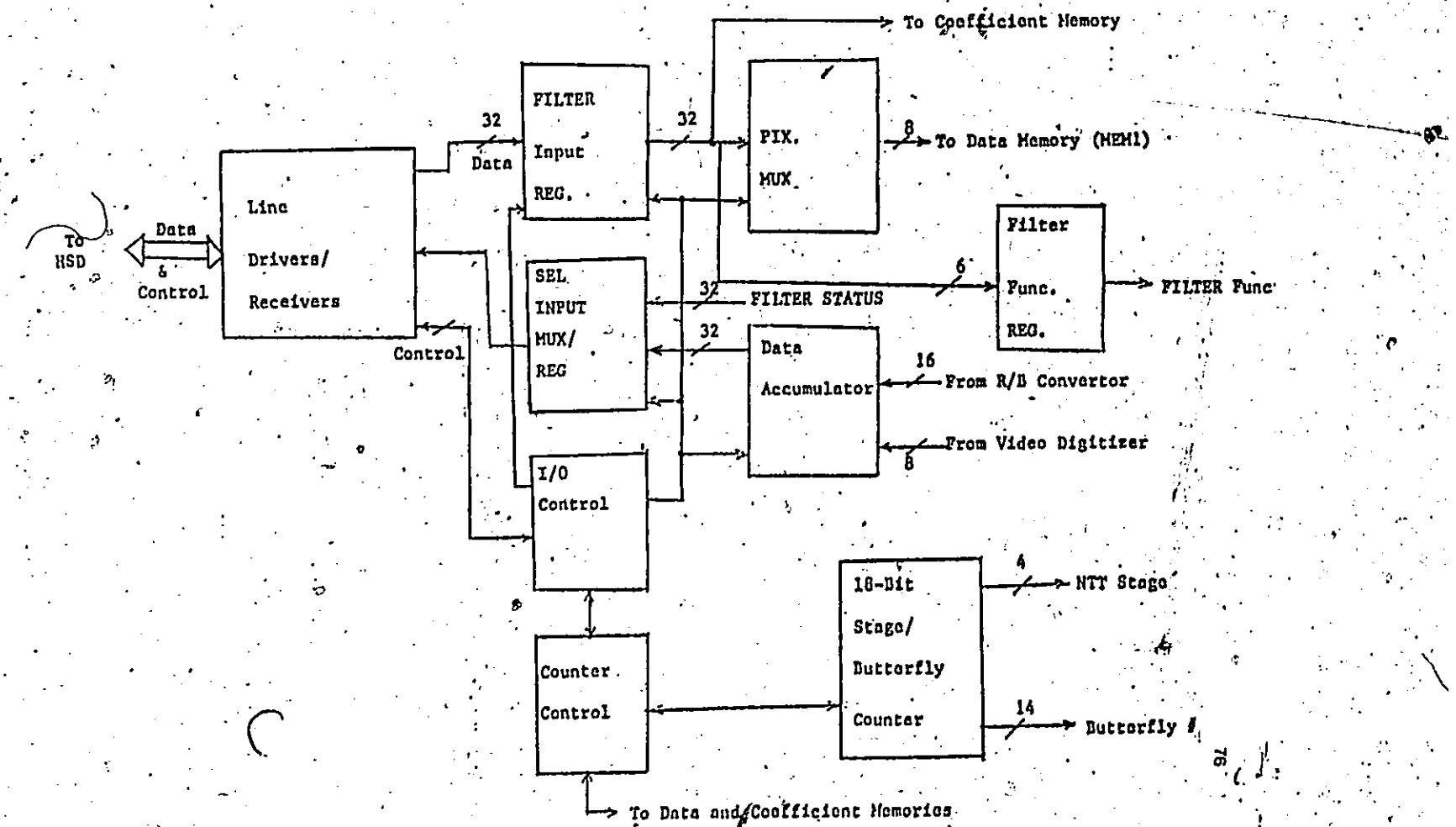


Fig. 6-2 Filter/HSD Interface Block Diagram

6.3.2 Interface Control Logic

The main interface signals that control the data transfer between the HSD and the filter are FILFUNCRDY, FILFUNCACK, FILINRDY, FILINACK, FILOUTRDY, FILOUTACK, FILSTATRDY and the FILSTATACK. Some of these signals are used to control the data transfer between the HSD and the Filter whereas others are used to control the data transfer between the Filter and the HSD. A brief description of these signals is given below.

FILFUNCRDY----Whenever a new filter function is specified, this line from the HSD goes high. This informs the filter that a new operation is desired

FILFUNCACK----This signal is generated by the filter interface to acknowledge the FILFUNCRDY function.

FILINRDY----From HSD. It indicates that data is ready to be transferred to the filter.

FILINACK----From Filter. Acknowledges the transfer of data from HSD to Filter.

FILOUTRDY----From Filter. Filter output is ready to go to HSD.

FILOUTACK----From HSD. Acknowledges the transfer of data from Filter to HSD.

FILSTATRDY----From Filter. Transfers the status of the Filter to the HSD. It informs the computer whether the Filter is on or off.

FILSTATACK----From HSD. Acknowledges the filter status.

6.3.3 Different Types Of Data Transfers Between Filter/HSD

Whenever a new filter function is specified, the FILFUNCRDY signal from the HSD goes high and if the filter is not in the process of accepting a previous function, the 32 bit data on the SELOUT31-SELOUT0 is loaded into the FILINREG. Since only 6 bits out of the 32-bits of the filter function data may specify a function, these 6 function bits are transferred to the Filter Function Register. Out of these 6 filter function bits only 3 bits specify a mutually exclusive operation and these 3 bits are decoded by the FILFUNCDECODER. The meanings of the function specified by the 3 function bits is as follows.

NOP-------- No Operation

LDIMG------ The bit pattern for this operation is 001. This function is used to load the image data into the filter buffers.

LDCOF------ The bit pattern for this operation is 010. This function is used to load filter coefficents into the coefficent memory.

SDFILDT--- The bit pattern for this operation is 101. This operation is used to send the filtered image to the memory.

SDCAMDT--- The bit pattern for this operation is 011. This operation is used to send the digitized data from the camera to the HSD interface.

CLRMCNT--- The bit pattern for this operation is 111. This operation is used to clear the butterfly counter and send Filter status to HSD.

6.3.4 Transfer Of Data From Digitizer To HSD

During the transfer of data between the HSD and the camera interface, SDCAMDT is true. Two additional signals CAMDTRDY and ENCAMDTRD are available to control the digitizer interface. CAMDTRDY signal comes from the digitizer and and the ENCAMDTRD signal is generated by the Filter/HSD interface. CAMDTRDY is active low whenever the digitized data from the A/D converter is available for transfer. ENCAMDTRD is high true whenever the filter interface is ready to accept more data to be sent to the HSD, otherwise this signal is false.

When SDCAMDT is true, this forces the Data Accumulator to accept data from the digitizer. The data accumulator consists of Multiplexers and Registers. The circuit diagrams are given in the appendix. Video digitizer output is connected to the RBCAMMUX 1/4. These Quad 2-Input Multiplexers can select data from 2 sources. One of the sources is the Video Digitizer and the other source is the filtered image data from the memory buffers. If SDCAMDT is true, then the data from the Video digitizer is selected and if SDFILDT is true then the filtered image data is selected for transfer to the HSD.

RBCAMMUX 5 is set up to store the digitized data into the FILOUT Registers. There are four registers FILOUTREG1/4

and data is stored into these registers a Byte at a time. When four bytes of data are accumulated in these registers, ENCAMDTRD goes low and the data in the FILOUTREG1/4 is loaded into the SEL Input Registers, SELINREG1/8. At this stage the FILOUTRDY line from the interface goes high to indicate to the HSDthat data is available in SELINREG1/8. The true state of the FILOUTRDY, brings ENCAMDTRD to a high state and next four bytes of data are accumulated in FILOUTREG1/4.

6.3.5 Timing Diagram

Figure 6.4 shows the timing diagram of CAMDTRDY, ENCAMDTRD and the digitized data to be transferred to the compiter. Digitized video data from the Digitizer is transferred to the HSD whenever SDCAMDT is true and CAMDTRDY is active low. ENCAMDTRD is high true whenever the filter interface is ready to accept more data to be sent to the HSD, otherwise this signal is false.

The digitized data is transferred to the HSD on the rising edge of MCLK50. Digitized data from the Digitizer must be available at least 50nS before the rising edge of MCLK50. Digitized data is transferred in blocks of 4 bytes. After 4 bytes of data have been transferred the signal ENCAMDTRD goes low on the falling edge of MCLK50. If the HSD is ready to accept more data at this time, the ENCAMDTRD signal becomes high within 50nS otherwise it will stay low.

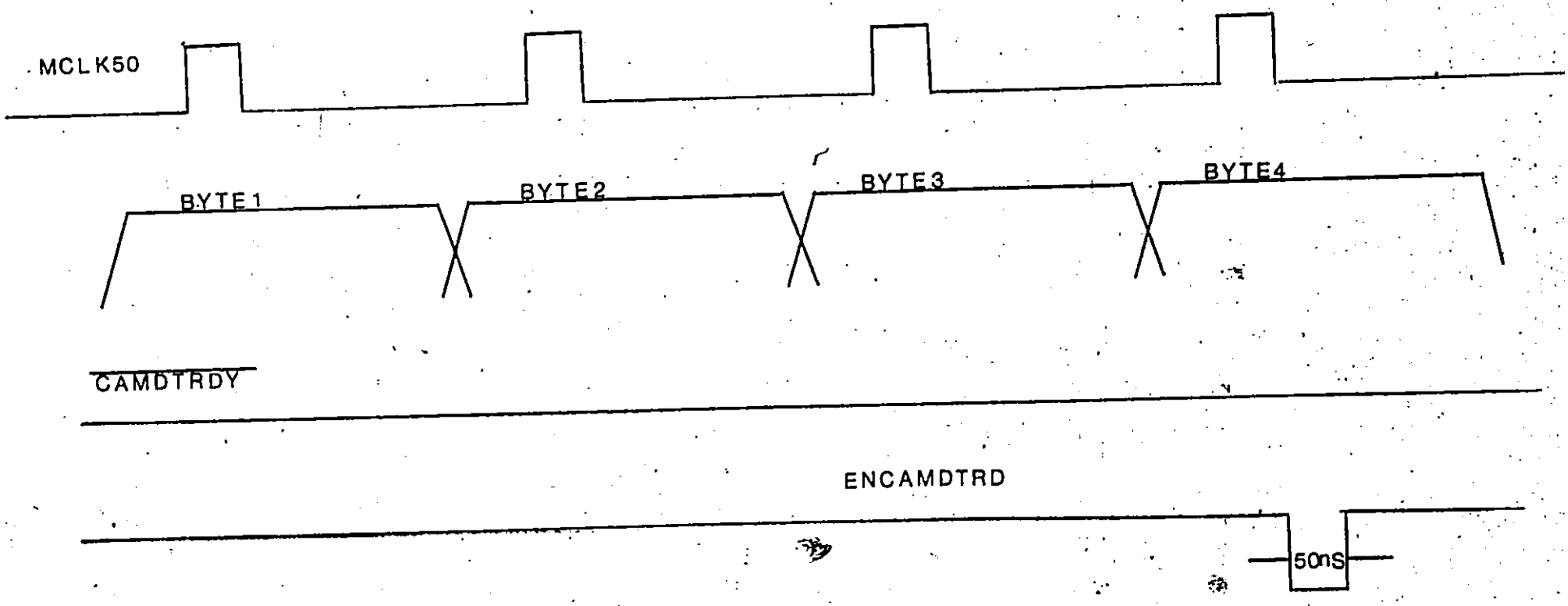


Fig 6 3 Timing Diagram For Data Transfer

Thus, the next byte of data from the digitizer must be available on the output lines as long as ENCAMDTRD is low.

6.4 SUBROUTINE SDIMG

The assembly language subroutine used for the purpose of sending a Digitized image from the Digitizer to the SEL computer is SDIMG. The subroutine is written in assembly language to improve the computational time.

The image is digitized in two Vidicon scans. The digitized data from each of these scans should be stored in a seperate array. Since, in each scan a (256X128) resolution digitized image is generated, thus 32K Bytes of data are transferred in each scan. Data is transferred through HSD as a 32 bit word. Thus, in total, 8K 32 bit words are transferred in each scan. From the two (256X128) data arrays a composite (256X256) image is generated through software.

The subroutine can be called from the main FORTRAN program as

CALL SDIMG(IDAT,IER1,IER2,IOCM)
where

IDAT-------DATA ARRAY CONTAINING THE DIGITIZED IMAGE DATA TO BE SENT FROM DIGITIZER TO THE COMPUTER.

IER1-------STATUS OF HANDLER POSTED IN THE FCB.

IER2-------STATUS OF THE DEVICE AS POSTED BY THE HANDLER IN IOCL.

IOCM-------PARAMETER TO INDICATE THAT THE I/O OPERATION IS COMPLETE.

The IOCL used for this purpose is given below.

```
EXECUTE ASSEMBLE

IOCL  GEN 8/X'A2',8/X'30',16/0
      GEN 32/W(DATA)
      DATAD 0
      GEN 8/X'82',8/X'60',16/X'2000'
      GEN 32/0
      DATAD 0
      GEN 8/X'A8',8/X'00',16/0
      GEN 32/W(DATA)
      DATAD 0
```

where

HSD command X'A2' means INPUT TRANSFER, DEVICE STATUS REQUEST AND COMMAND CHAIN

UDD command X'30' means CLEAR MAIN COUNTER OF FILTER

GEN 32/W(DATA) is to GENERATE DUMMY DATA ADDRESS

HSD command X'82' means READ DATA AND COMMAND CHAIN

UDD command X'60' means SEND CAMERA DATA TO COMPUTER

16/X'2000' means TRANSFER COUNT IS 8 K WORDS

HSD command X'A8' means INPUT TRANSFER, DEVICE STATUS REQUEST AND INTERRUPT AFTER COMPLETED PROCESSING IOCB.

UDD command X'00' means NO OPERATION.

6.5 OPERATION AND TESTING

The digitizer hardware was assembled using standard TTL components. The operation of the digitizer was checked with the help of a DGLCH LAM 3250 Logic Analyzer. The important outputs of the digitizer that were checked are the CAMDTRDY signal which goes active low whenever digitized data is ready for transfer, the CONVERT signal and the 8 bit A/D converter output.

The A/D converter output depends on the nature of the image. The operating range of the A/D converter has been so adjusted that the output values above 220 represent the different shades of white and values below 40 represent various shades of black. The operation of the digitizer was checked by digitizing images of different picture contents.

Fig. (6.4) shows the digitizer output for a white image. In this figure B7 and B6 represent the CAMDTRDY and CONVERT signal respectively and A7 through A0 represent the 8 bit A/D converter output. In the case of a white image, it can be observed that the A/D converter output value is greater than 220.

Fig. (6.5) depicts the digitizer output for a black image. As can be observed from this figure the A/D output value is less than 40.

Fig. (6.6) shows the digitizer output for an image which is half black and half white. It can be observed from this figure that for black portions of the image the A/D output value is less than 40 and for white parts of the image the value is greater than 220

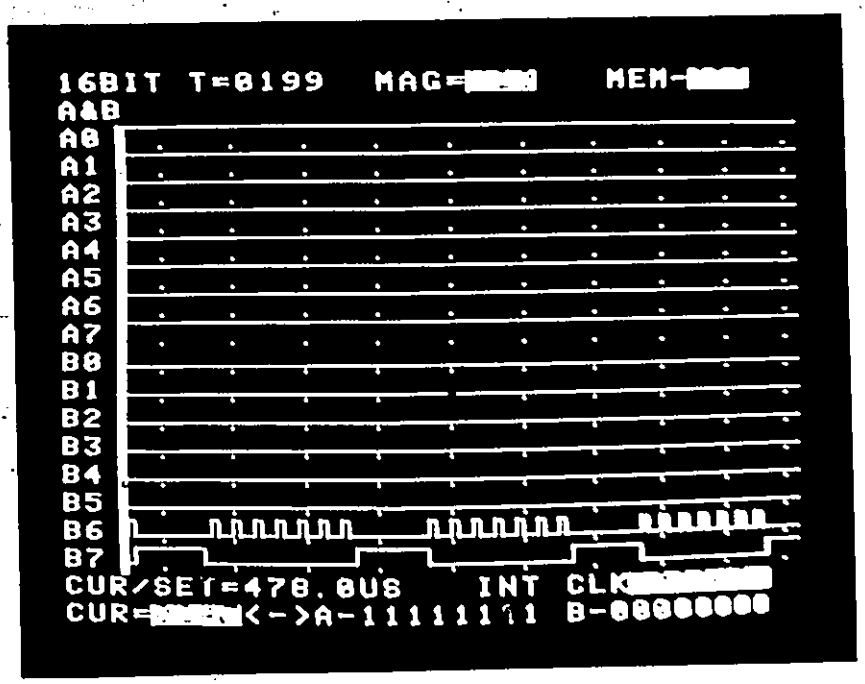


Fig. 6.4 Digitizer Output(White Image)

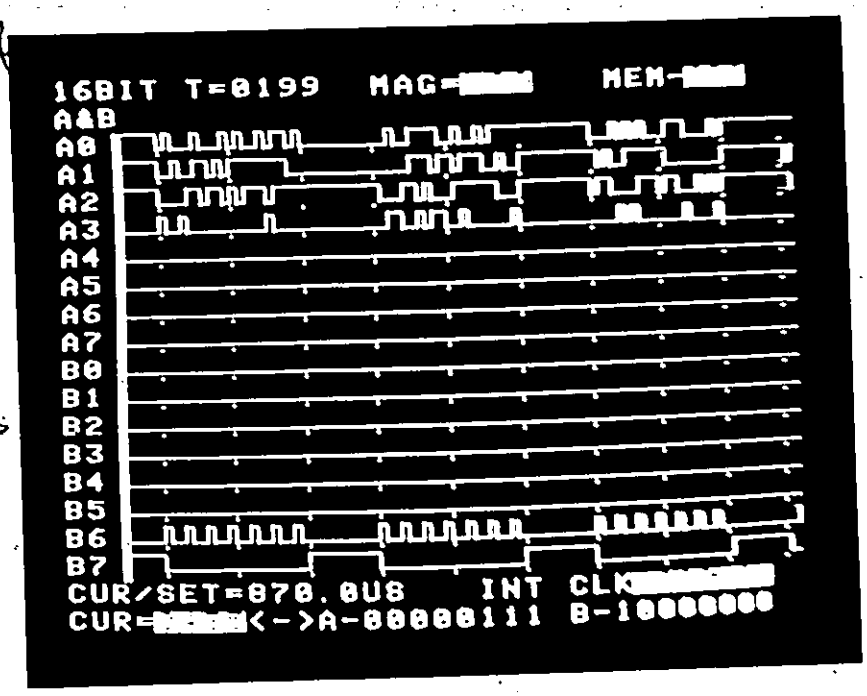


Fig. 6.5 Digitizer Output(Black Image)

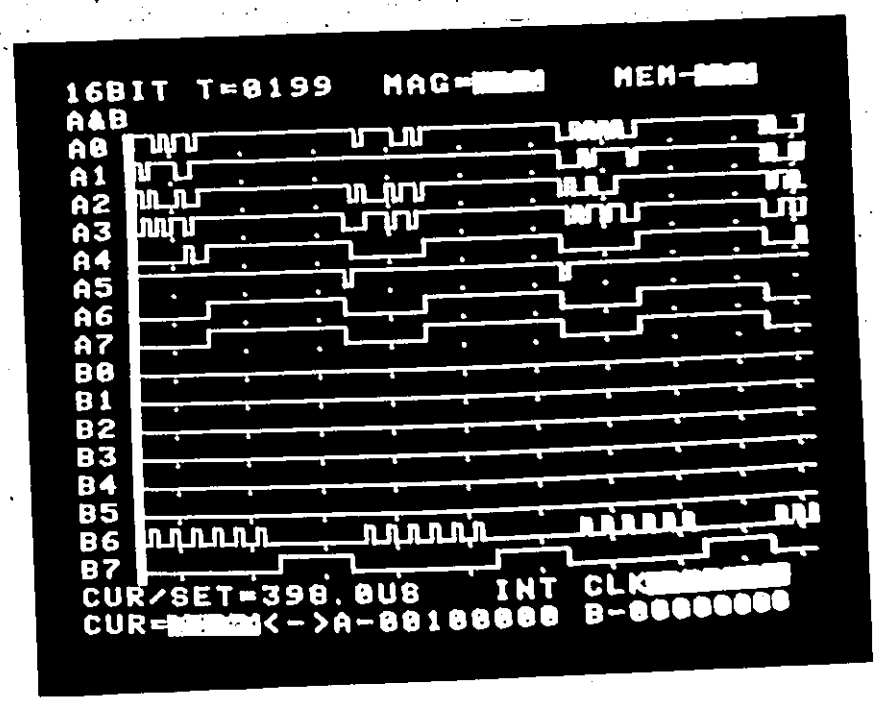


Fig. 6.6 Digitizer Output(Half Black And Half White Image)

Chapter VII

SUMMARY AND CONCLUSIONS

This research was undertaken to design and implement a Video Digitizer for the Image Processing System developed by this department. The main aim of the project was to design a system which meets all the requirements of the Image Processing Executive and at the same time fits into the existing hardware without any major modifications and additions to that hardware.

The work was accomplished in three stages. First of all, an interface was built between the Vidicon camera and A/D converter. The function of this interface is to allow the A/D conversion of the video signal at appropriate timings and at desired conversion frequencies. The major objective was to digitize the image at very high rates. To accomplish this, a new technique was developed to select the sampling points on a scanning line. Through this method, a 256X256 image can be digitized in two scans of the vidicon camera or about 33ms.

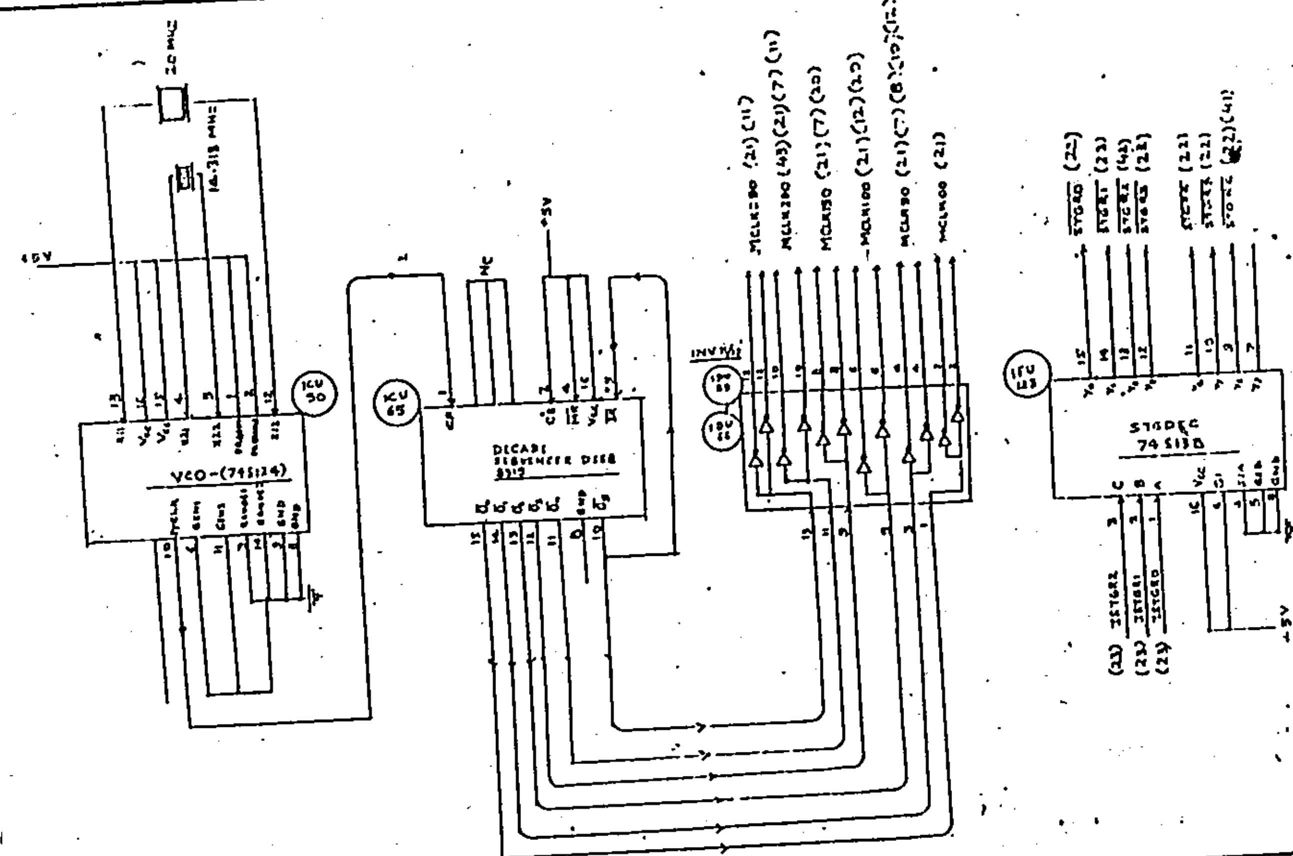
In second stage of the project, an interface was designed between the Digitizer and the SEL computer. To ac-

complish this task, the HSD interface for the SEL computer was studied in detail. The existing hardware assembled around the HSD was also studied and an effort was made to utilize this hardware to fullest extent for data transfer purposes. In the final stage of the work, software drivers were written to control the operation of the digitizer. The programs were written in assembly language to speed up the operation.

The hardware was assembled using standard TTL components. The Digitizer is very easy to operate and the digitization process can be initiated through computer console. Although, the Digitizer was designed for use with a particular system, still the various design requirements considered in the implementation are general in nature. Thus, with slight modifications, the digitizer can be used for other systems also.

Appendix A

SCHEMATIC DIAGRAMS



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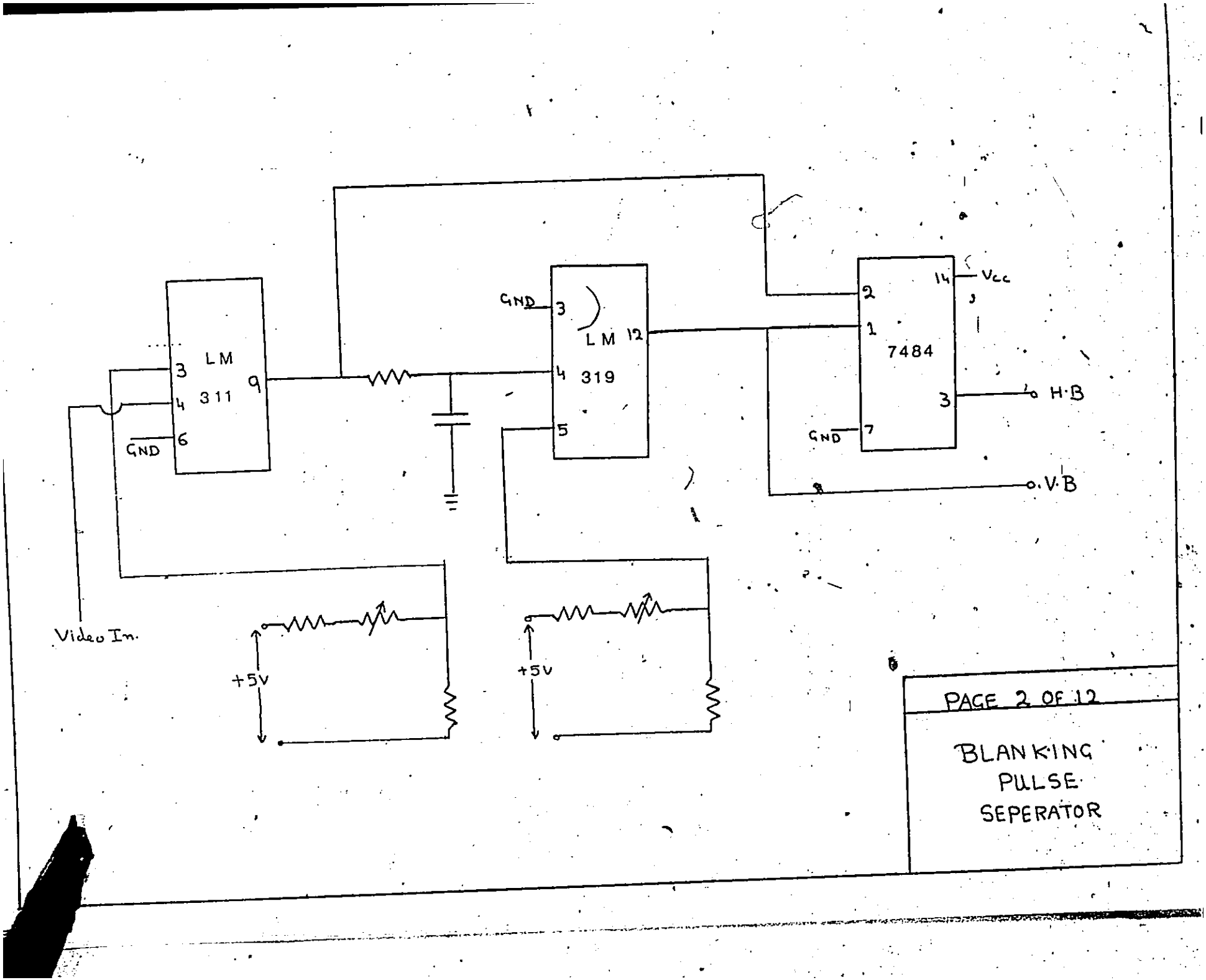
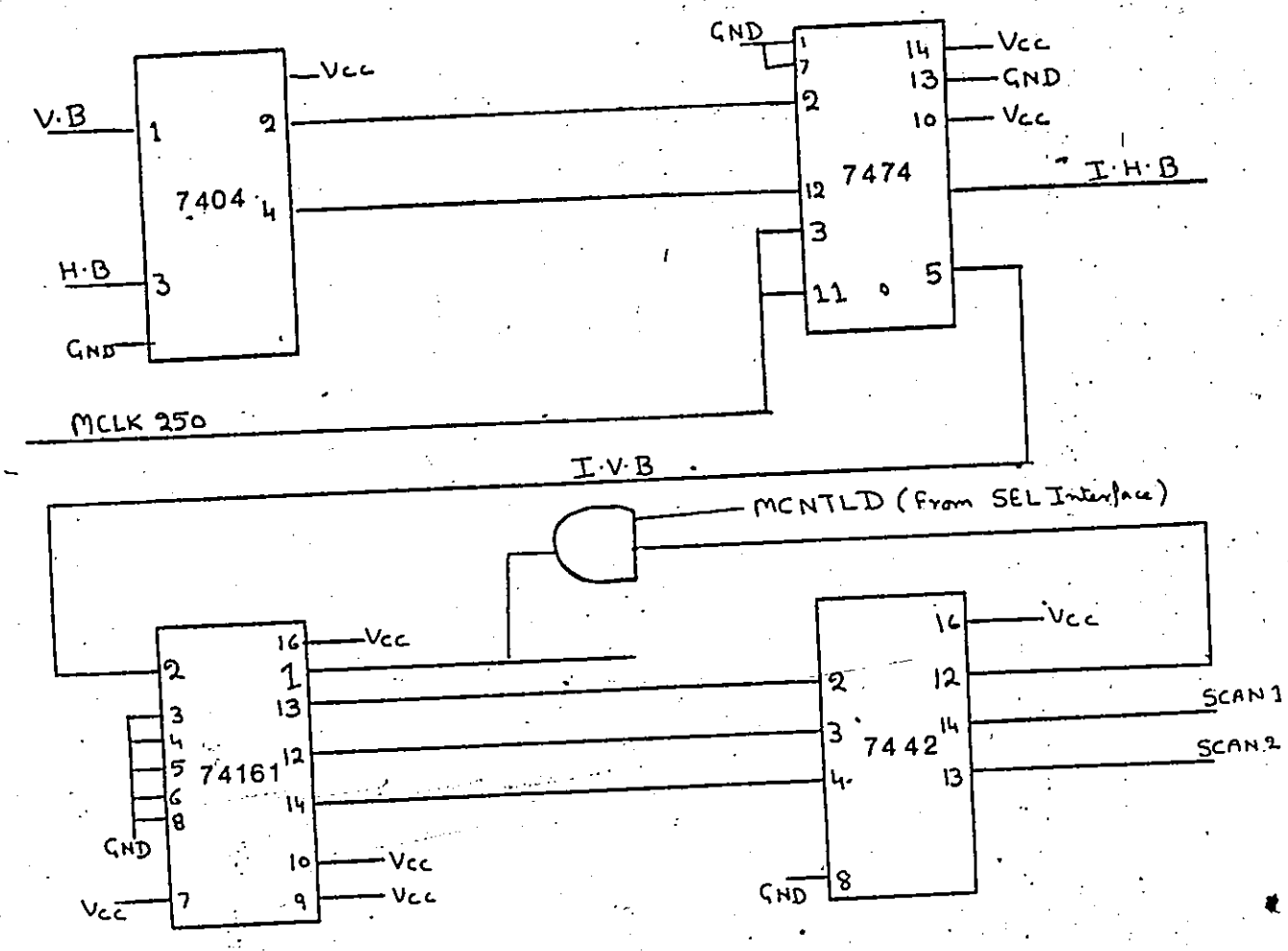
CLOCK GENERATOR


LM
311
3
4
6
9
GND
LM
319
GND
3
4
5
12
7484
2
1
14
Vcc
3
H·B
GND
7
V·B
Video In.
+5V
+5V
PAGE 2 OF 12
BLANKING
PULSE
SEPERATOR



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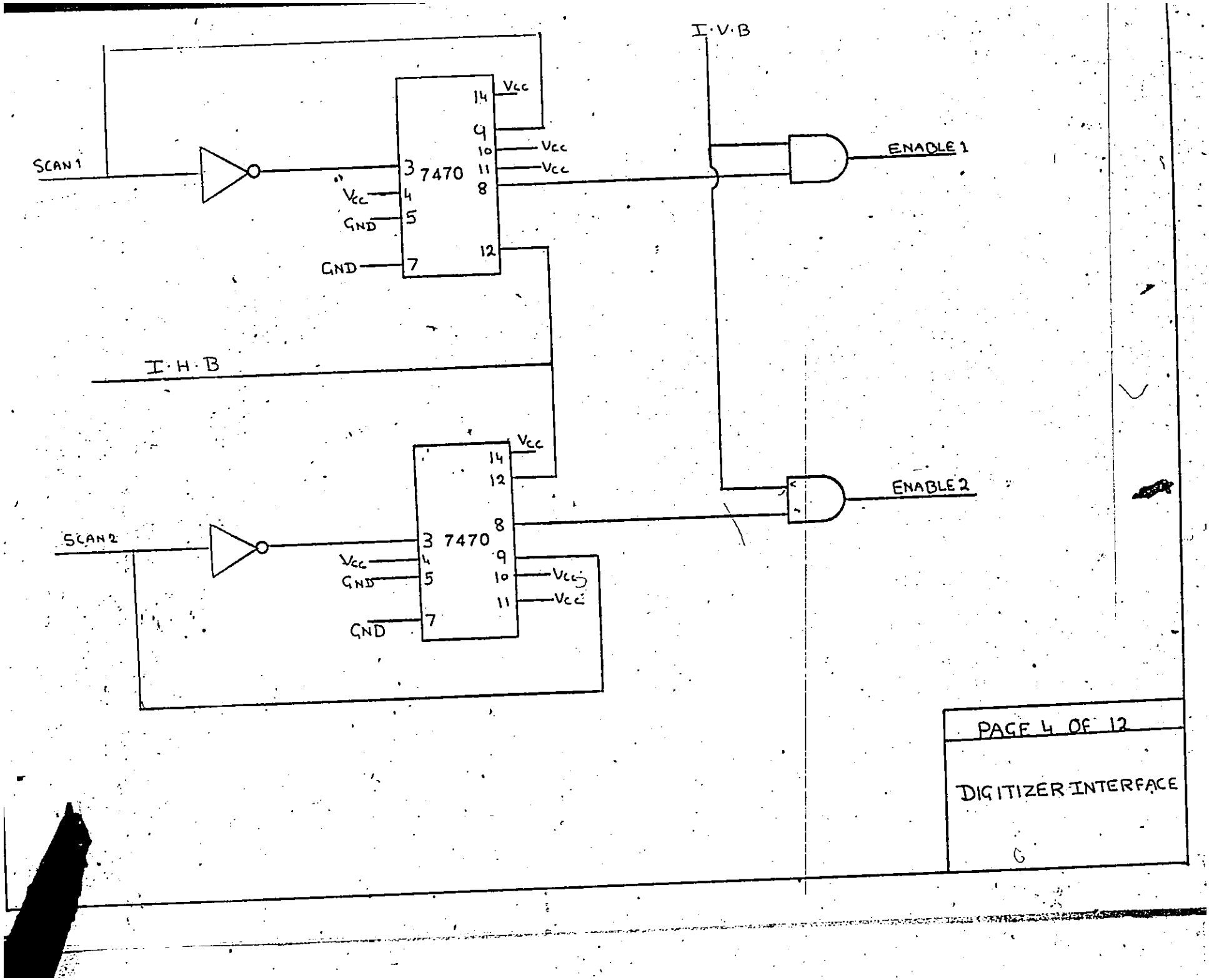
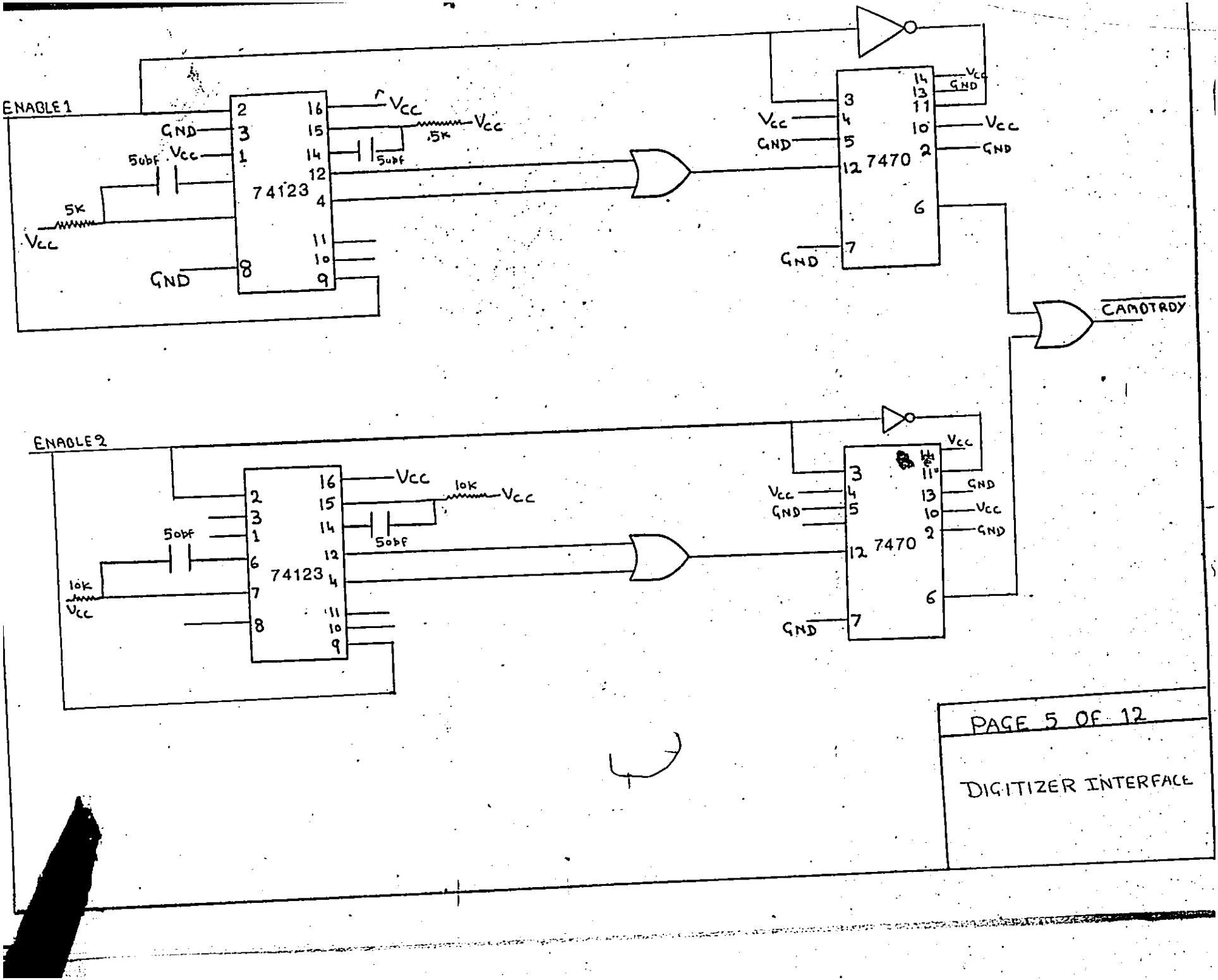
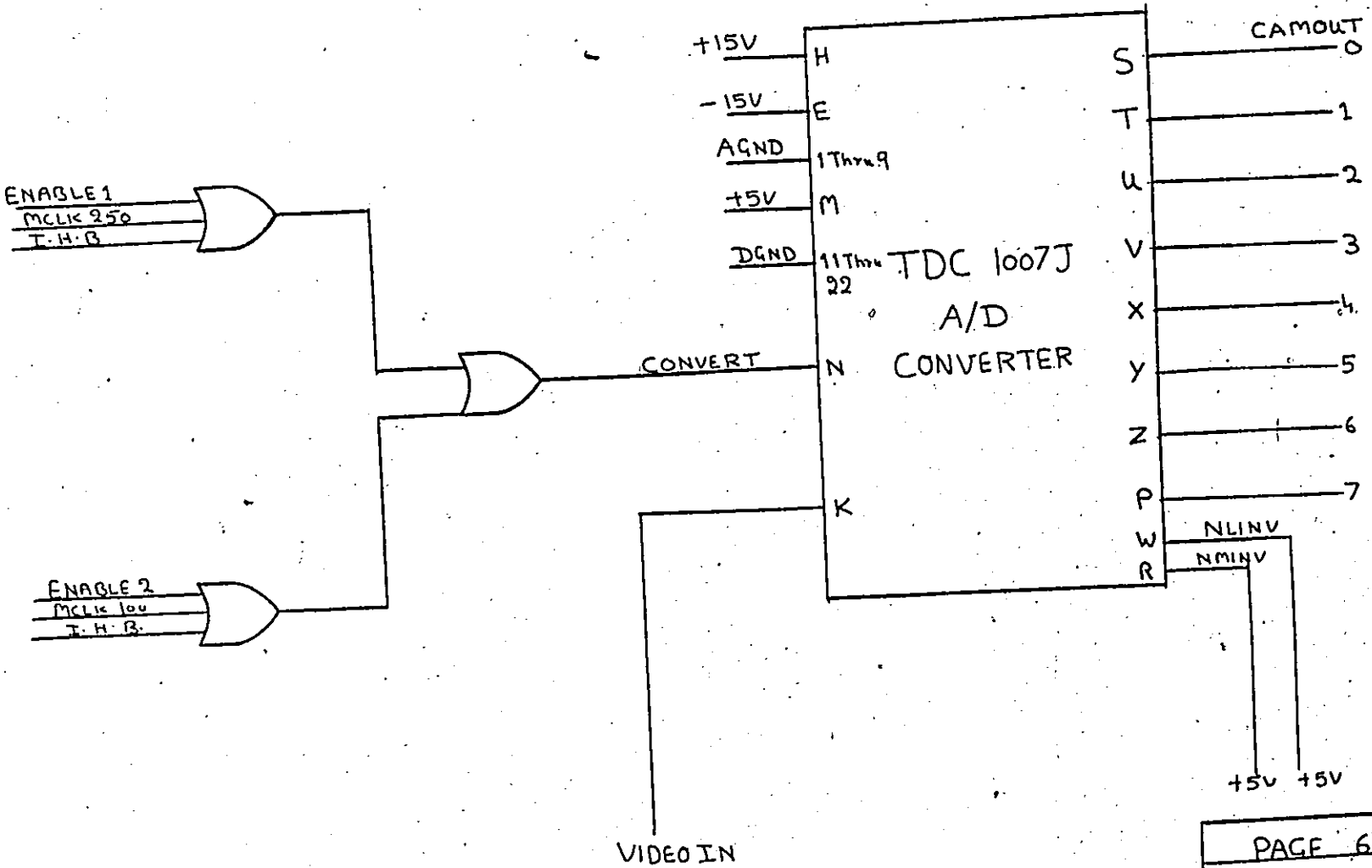
DIGITIZER INTERFACE


I·V·B
SCAN 1
7470
Vcc
GND
ENABLE 1
I·H·B
SCAN 2
7470
ENABLE 2
PAGE 4 OF 12
DIGITIZER INTERFACE


ENABLE1
GND
50pF
Vcc
5K
Vcc
74123
GND
5K
Vcc
50pF
Vcc
GND
7470
Vcc
GND
CAMDTRDY
ENABLE2
50pF
10K
Vcc
74123
10K
Vcc
50pF
Vcc
GND
7470
Vcc
GND
PAGE 5 OF 12
DIGITIZER INTERFACE



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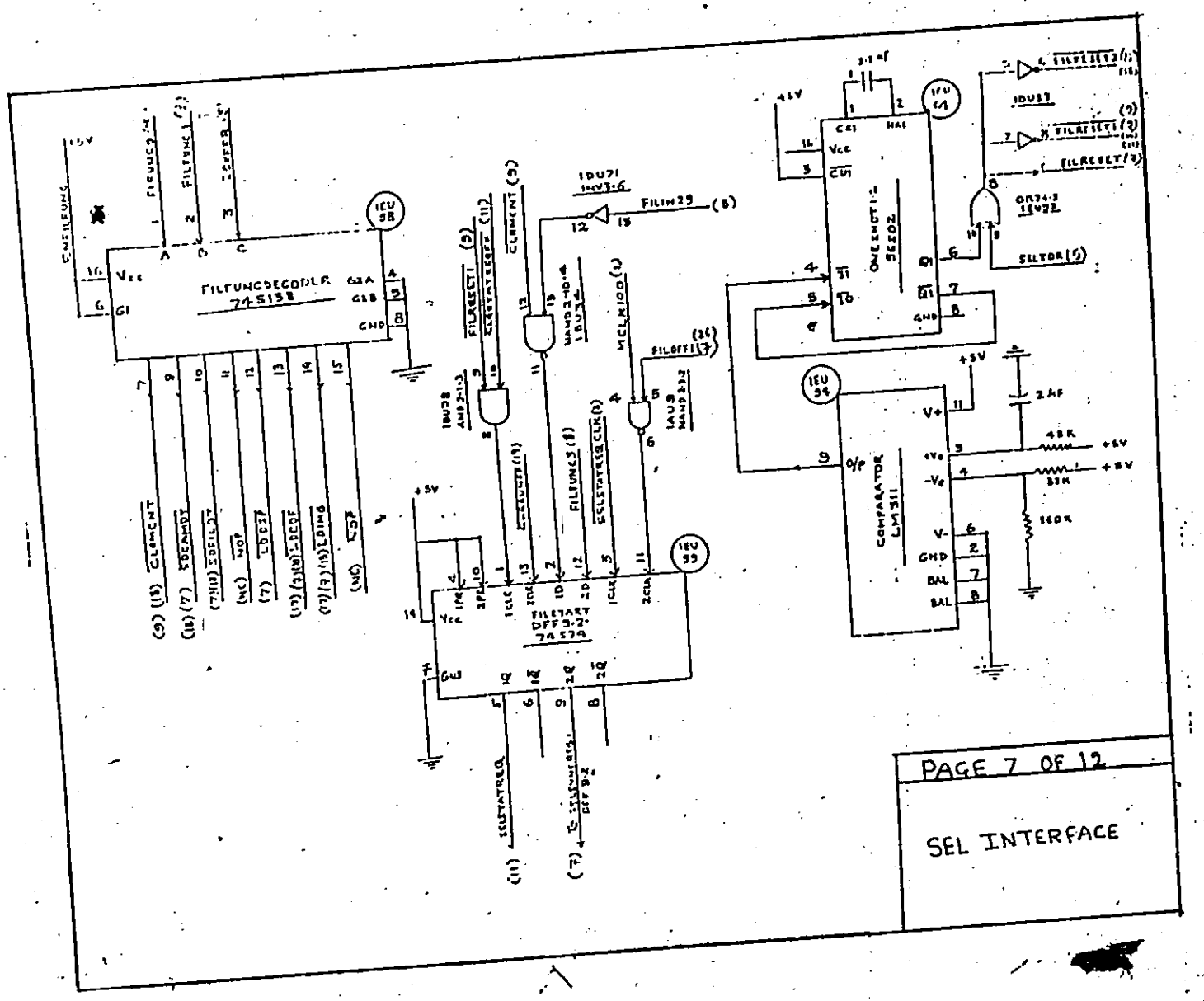
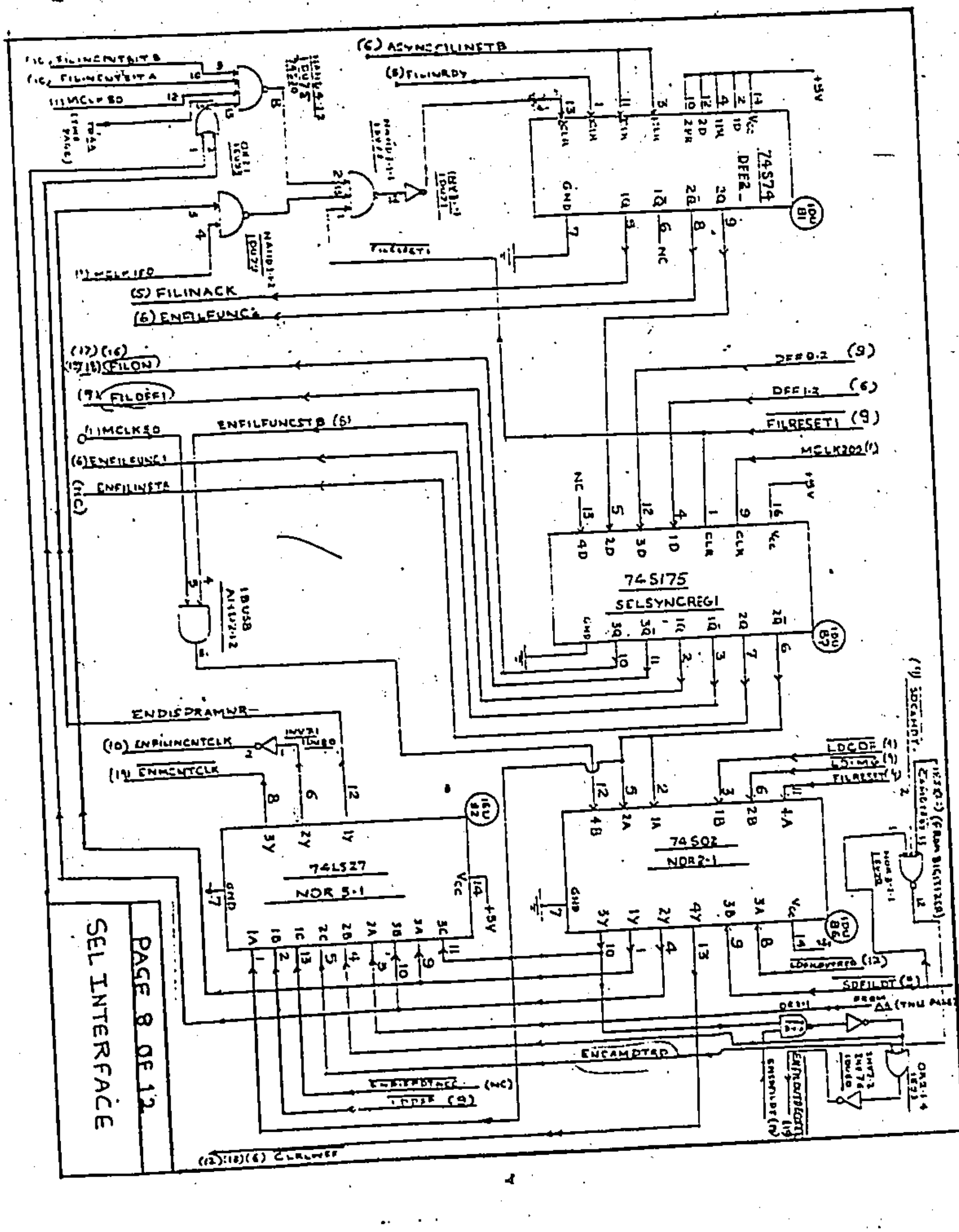
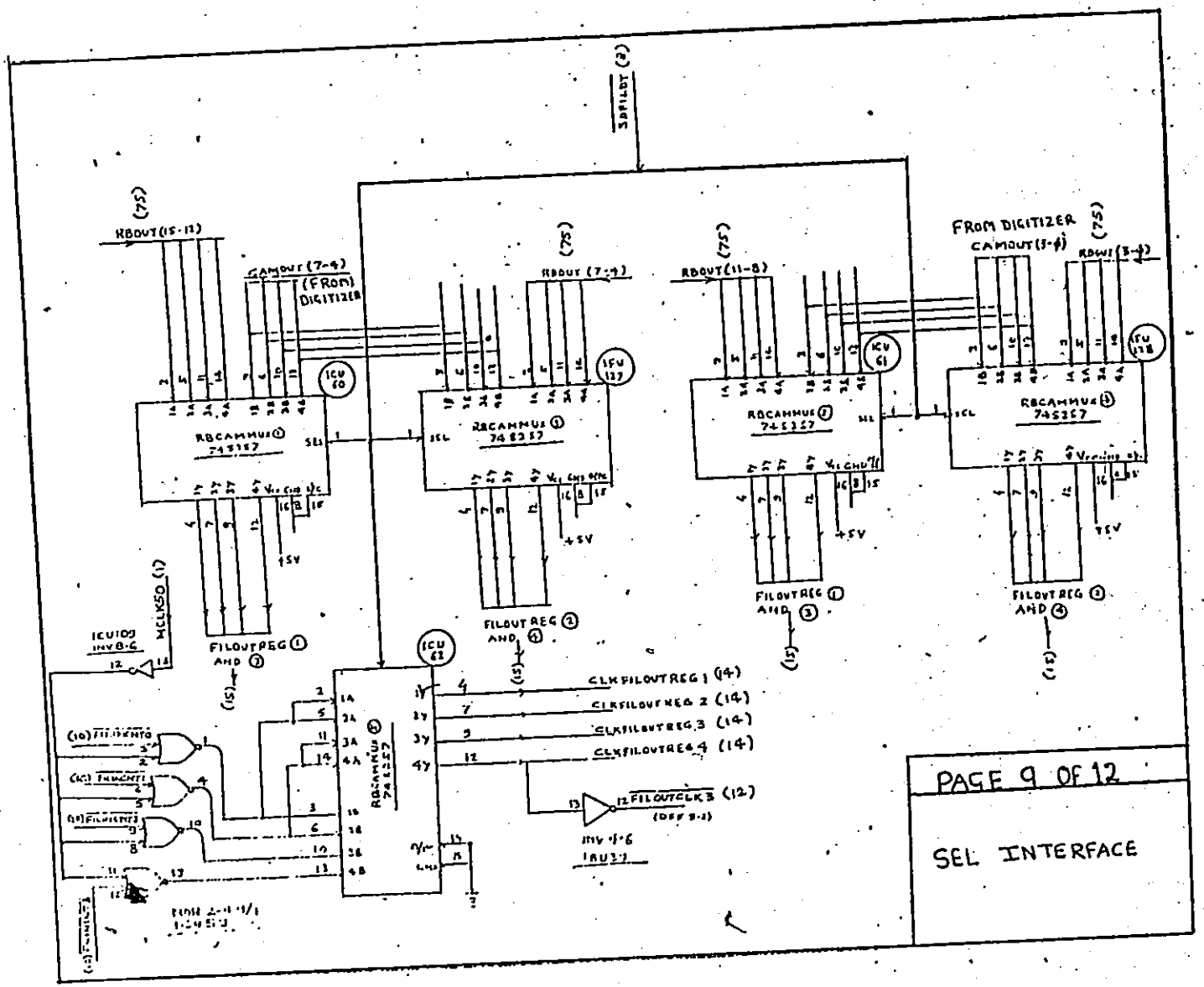
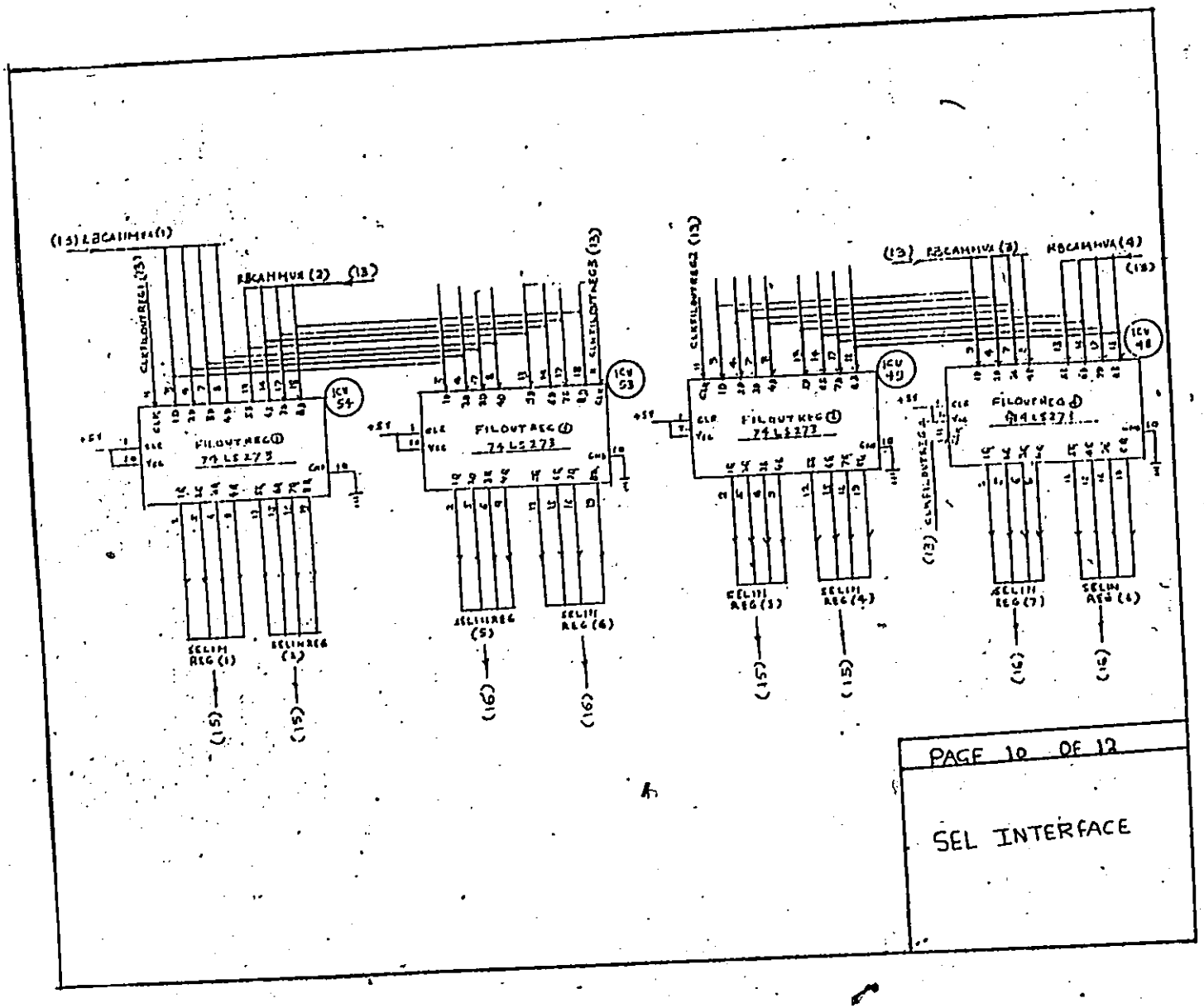
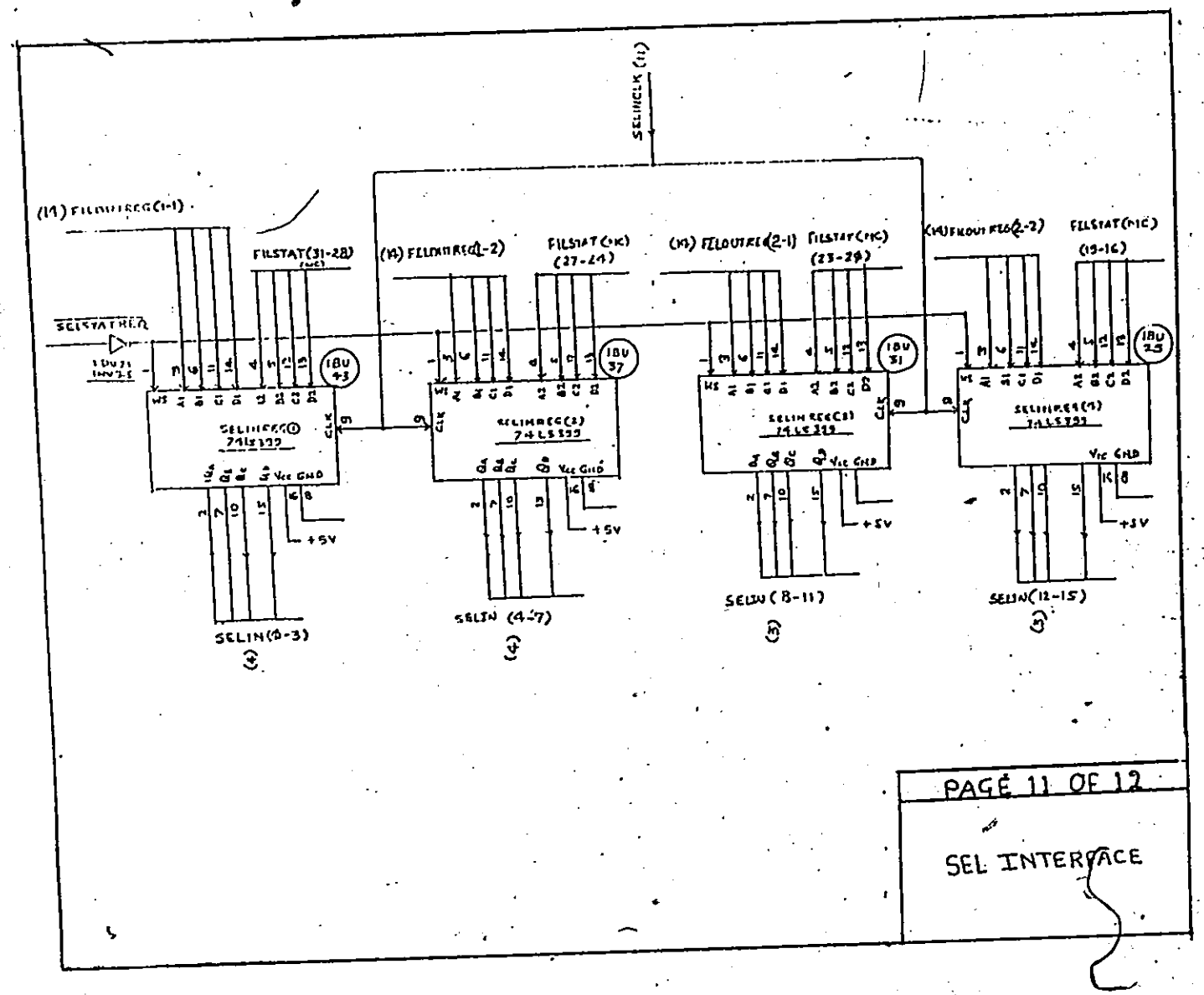
DIGITIZER INTERFACE


FILFUNCDECODER
74S138
ONESHOT 1/2
9602
COMPARATOR
LM311
FILSTART
OFF 3-2
74S74
SEL INTERFACE


SEL INTERFACE
PAGE 8 OF 12
(6) ASYNCFILINSTB
(8) FILINRDY
74S74
DFF2
74S175
SELSYNCREG1
74LS27
NOR 3-1
74S02
NOR2-1
(5) FILINACK
(6) ENFILFUNC2
(9) FILOFF1
ENFILFUNCSTB (6)
(1) MCLK50
(6) ENFILFUNC1
ENFILINSTA
DFF0-2 (9)
DFF1-2 (6)
FILRESET1 (9)
MCLK202 (1)
ENDISPRAMWR
(10) ENFILINCNTCLK
(19) ENMCNTCLK
ENCAMDTRD
SDFILDT (8)
(12)(18)(6) CLRLWFF
+5V


SAPILOT (2)
RBOUT(15-12) (75)
CAMOUT(7-4) (FROM) DIGITIZER
RBOUT (7-4) (75)
RBOUT(11-8) (75)
FROM DIGITIZER CAMOUT(3-0) (75)
RBOUT(3-0)
ICU 60
ICU 129
ICU 61
ICU 128
RBCAMMUX ① 74S257
RBCAMMUX ② 74S257
RBCAMMUX ③ 74S257
RBCAMMUX ④ 74S257
+5V
FILOUTREG AND ①
FILOUTREG AND ②
FILOUTREG AND ③
FILOUTREG AND ④
MCLKSO (1)
ICU103 INV 8-6
ICU 62
CLKFILOUTREG 1 (14)
CLKFILOUTREG 2 (14)
CLKFILOUTREG 3 (14)
CLKFILOUTREG 4 (14)
FILOUTCLK 3 (12)
INV 1-6
PAGE 9 OF 12
SEL INTERFACE


(13) EBCAHMVA (1)
RBCAHMVA (2) (13)
(13) EBCAHMVA (3)
RBCAHMVA (4)
(13)
FILOUT REG ①
74LS273
SELIM REG (1)
SELIM REG (2)
SELIM REG (5)
SELIM REG (6)
SELIM REG (3)
SELIM REG (4)
SELIM REG (7)
SELIM REG (8)
(15)
(16)
PAGE 10 OF 12
SEL INTERFACE



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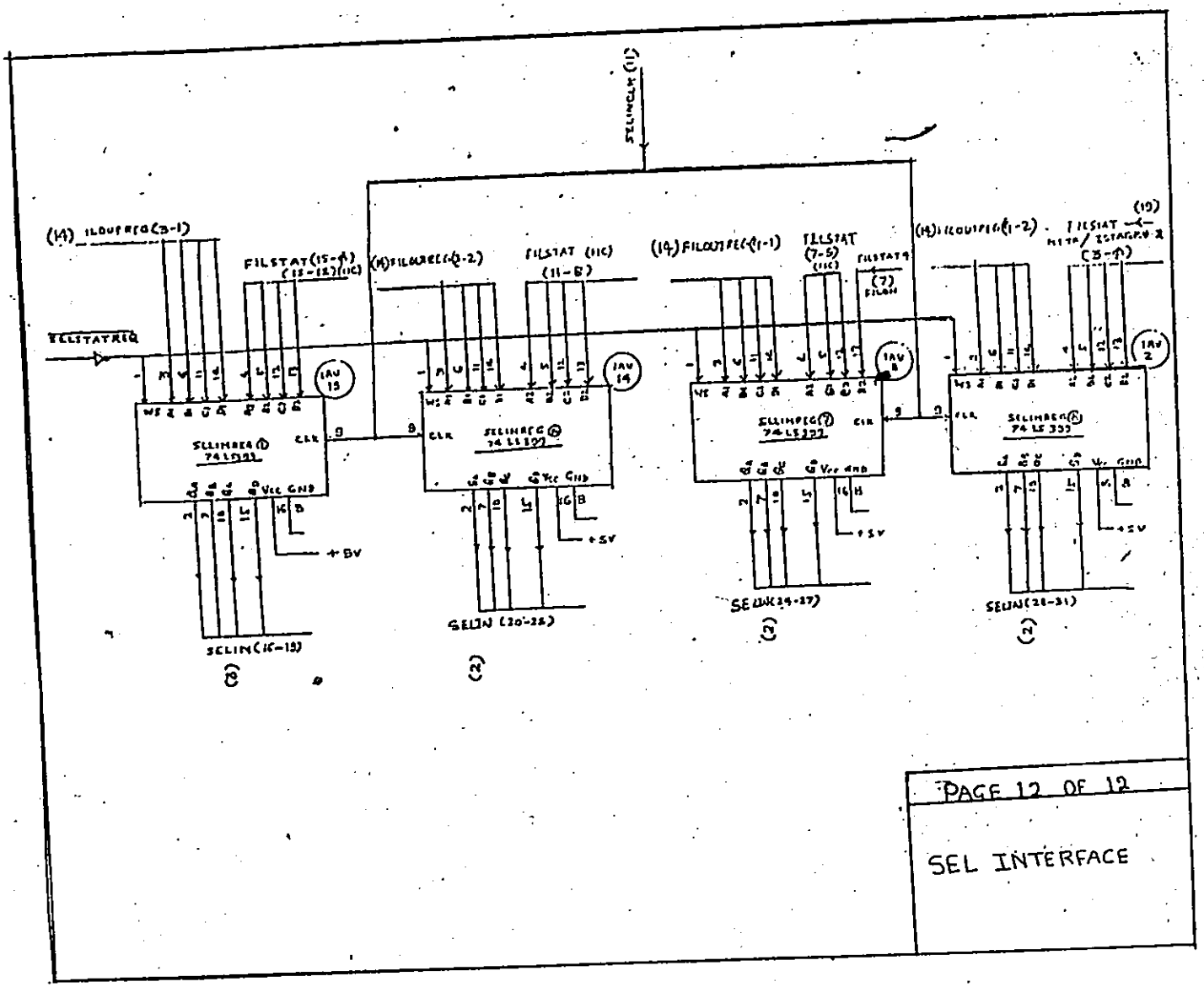
SEL INTERFACE



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SEL INTERFACE

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