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An Ultra Low Power Voltage Regulator for RFID Application

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An Ultra Low Power Voltage Regulator for RFID Application
by

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ABSTRACT

An ultra low power and low voltage regulator for radio-frequency identification (RFID) passive tags is designed and optimized in this thesis. It consists of a low power sub-1V reference voltage generator with temperature and supply voltage ripple compensation, and a low-dropout voltage (LDO) regulator. The circuits are designed in CMOS 65nm technology. The total quiescent current of 63.8nA at 1.5V supply voltage has been achieved using properly sized transistors operating in the subthreshold region. With the low voltage property of transistors operating in subthreshold region the output regulated voltage can easily achieve 1V with load capacity of 50uA. Self-biased current sources are employed and optimized to eliminate the effect of supply voltage variation and to achieve a line regulation of 4.06mV/V. A PMOS pass device with small output resistance is used to reduce the load regulation to 6.57mV/50uA. By utilizing subthreshold properties, the temperature coefficient is reduced to 12.7 and 31ppm/°C for the reference voltage and regulated voltage, respectively. The circuits can operate well from -30°C to 50°C, a typical temperature range of the environment where RFID tags are widely deployed.

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LIST OF ABBRIVATIONS

DIBL	Drain Induced Barrier Lowering
LDO	Low-Dropout
LIR	Line Regulation
LOR	Load Regulation
MOSFET	Metal-Oxide-Semiconductor Field-Effect Transistor
NMOS	N-Channel MOSFET
OPA	Operational Amplifier
PMOS	P-Channel MOSFET
PSRR	Power Rejection Ratio
RF	Radio Frequency
RFID	Radio Frequency Identification
UHF	Ultra High Frequency
TC	Temperature Coefficient

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CHAPTER I

INTRODUCTION

The demand for ultra low power voltage regulators has been driven by the extensive use of RFID applications. As the functions and applications of RFID become more complicated with limited power available, these circuits are forced to operate under low voltage and low power consumption conditions. Furthermore, high current efficiency also becomes necessary to extend the functionality of RFID tags. Due to the limitation on the power available for a RFID tag, its functionality depends on the amount of quiescent current and load current saved. This chapter discusses the role and the characteristic of ultra low power voltage regulator in RFID applications. Moreover, the objectives of the research are identified and defined according to the demand of RFID systems.

1.1 Regulator in RFID System

Radio-frequency identification (RFID) is one of the widely used technologies for many applications, such as sensor networks, supply-chain management, security, automotive and etc. There are two major parts of RFID system; one is RFID reader and the other is RFID tag [1]. The operation principle for RFID systems is that a reader generates RF signal containing information and energy; then sends signal to tags around it. A tag receives RF signal; then it sends information back to reader according to what reader had requested.

RFID tags can be classified into two categories, passive tag and active tag. Active tags require battery power to operate. It uses battery power to operate its internal circuitry,

such as front-end analog circuit, and digital processes, and to send information back to reader. Since an active tag has battery as a support, it has longer operation range and more process complexity, but its lifetime heavily depends on the energy contained in the battery; usually, the average lifetime of an active tag is about 2 years. Also, due to large area and materials of battery, the cost of producing active tags is much higher than passive tags. Therefore, many RFID applications prefer to use passive tag if it meets requirements.

On the other hand, a passive tag utilizes only the energy generated from RF signal. All of its processes including front-end circuits and digital processors depend on the amount of energy the tag received from RF signal sent by reader, thus the energy available is very limited. In order to have higher operation range and more complex computational power on passive tags, low power design is extremely important in every aspect of passive tag circuitries. Since the passive tags do not require a battery on board, passive RFID tags are preferred if their performance meets requirements, due to their low cost, small area and longer lifespan.

Figure 1 illustrates the building blocks for passive RFID tag system. It consists of an antenna, power management circuits (rectifier, and voltage regulator), signal processing circuits (demodulator, modulator, and clock generator), and digital processors. Voltage Regulator is a very important part of a tag, because it generates regulated voltage supply to both RF front-end and digital parts that their operation accuracy depends on the precision of supply voltage. Since the power generated by rectifier is very small and the voltage supply is very low, a regulator should be able to work at low supply voltage and consume only ignorable amount of current. Moreover, RFID tags are usually placed in

harsh environments; such that, the operation of a regulator also needs to operate over a wide range of temperature and supply voltage variations. From all the requirements, series LDO voltage regulator is preferred to use as the regulator topology. The detail reasons of choosing LDO regulator will be discussed at next chapter.

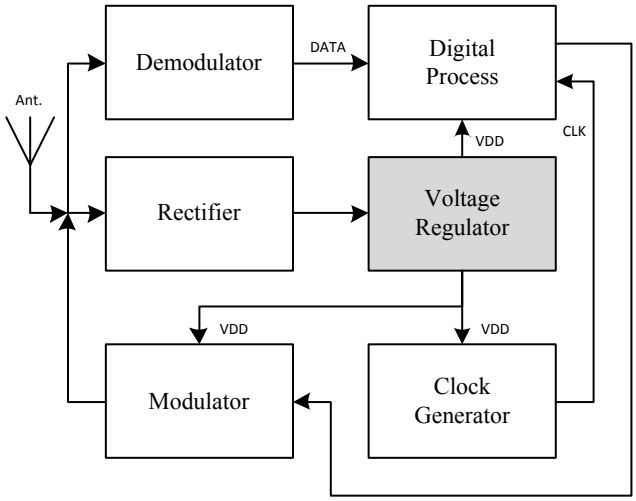

Figure 1. Building block of passive RFID tag

1.2 Definition

An ultra low power and low voltage regulator consists of two parts, a LDO series voltage regulator and a sub 1V reference generator. Ideally, a series low-dropout (LDO) voltage regulator provides a stable and constant dc voltage which is free from load current variation, input-voltage variation, temperature, and time. The dropout voltage is defined as the minimum voltage difference between the output voltage and input voltage at the point where the circuit can still regulate voltage. Also, low-dropout voltage indicates that the voltage across pass device is as low as 100mV to 200mV. The series regulator means that the pass device is connected in series with input and output

terminals of the regulator. For LDO regulator, the output voltage is always lower than input voltage by a minimum value of dropout voltage. It has low output impendence, thus the performance is enhanced. Also, the LDO can be applied to high power, low power and ultra low power applications. Since the power generated by RF signal is very small, LDO regulator is suitable for RFID application.

Figure 2 shows the block level diagram of generic series low-dropout regulator. The circuit is composed of a reference voltage generator, an operation amplifier (OPA), a pass device, a feedback network, and a storage device. The OPA, the pass device and the feedback network constitute a loop for regulation. The operation principle is that first, the output of the regulator generates an error signal through the feedback network. Secondly, the OPA compares the error signal with the reference voltage and amplifies the difference to control the pass device. Then a constant output voltage can be achieved by controlling the load current flow through the pass device.

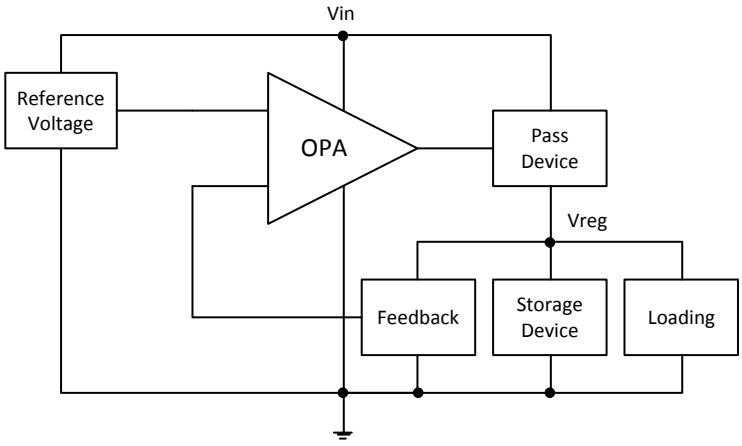

Figure 2. Block Diagram for LDO Voltage Regulator

The reference voltage generator provides stable dc voltage with a limited loading current capability. This is usually a Zener diode and bandgap reference that Zener diode is usually used in high voltage applications (approximately seven volt), and bandgap reference is better suitable for low voltage and high accuracy applications (approximately 1.2 volt) [2]. But in our application, the regulated voltage is approximately 1 volt which is lower than bandgap reference; therefore a better reference structure with sub-1-volt reference and low power dissipation is needed.

In order to have low power and low voltage operation with small chip area, most of the transistors are designed to work at the subthreshold region and no resistor or bipolar transistor is required in our voltage regulator. Feedback network in general is a voltage divider used to return part of the regulated voltage to the OPA input. As illustrated in Figure 3, if the desired regulated voltage is twice of the reference, the feedback network consists of two devices with same resistance in series with one end to output and one end to ground and the middle point connect to OPA.

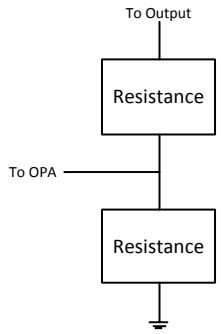

Figure 3. Example for Feedback Network

1.3 Performance Evaluation

The important performance aspects of LDO regulator and voltage reference generator can be categorized into several parts. Those aspects are important for comparing the performances between devices.

1.3.1 Reference Voltage Generator

The performance evaluation for reference voltage generator can be separated in to several parts, namely, operation temperature range, input voltage range, output voltage level, output voltage variation, temperature coefficient (TC) and quiescent current. In RFID applications, these aspects are important to see if the circuit generates stable voltage reference which meets the performance requirements.

The operation temperature region is defined according to the environment that the device going to be in, thus the circuit can be designed according to it. Input voltage range is defined as the minimum and maximum supply voltage that the device can still generate acceptable level of reference voltage. It depends on the technology used to design the device and the circuit structure of the device. Output voltage level is not as important as other aspects since the regulator can adjust its feedback network to adapt to different reference voltage and then generate desired regulated voltage level.

Output voltage variation or line regulation (LIR) is defined as the dc output voltage variation with respect to input voltage variation. It is expressed as

$$\mathrm{LIR} = \frac{\Delta V_{REF}}{\Delta V_{DD}}, \tag{1.1}$$

where ΔV_{REF} and ΔV_{DD} are the voltage variation of reference voltage and supply voltage. This parameter gives a sense of how much reference voltage changes with varying supply voltage at low frequency. If LIR value is small, the reference voltage has smaller

dependency to supply voltage variation. The power rejection ratio (PSRR) at different frequencies can be expressed as

$$\mathrm{PSRR} = 20\log\left(\frac{\Delta V_{\mathrm{REF}}}{\Delta V_{\mathrm{DD}}}\right), \tag{1.2}$$

This parameter gives the accuracy of reference voltage at different frequencies. Temperature coefficient is also a very important indication for reference voltage generator evaluation, since it represents the dependency of reference voltage on the temperature. TC can be expressed as

$$\mathrm{TC} = \frac{\Delta V_{\mathrm{REF}}}{\Delta ℃} \tag{1.3}$$

where $\Delta ℃$ is the temperature variation. Smaller TC value means that the reference voltage presents less dependency to temperature. Quiescent current is defined as the total current flow through the device when there is no input voltage variation at different temperature. This performance parameter has direct relation with power consumption of the reference circuit. Greater quiescent current introduces higher power consumption.

1.3.2 LDO Regulator

The aspects for evaluating LDO regulator are, namely, acceptable input voltage range, output voltage level, load capability, line regulation, PSRR, load regulation, TC and quiescent current. Same as the reference voltage, the input voltage range depends on the technology and reference voltage generator. The output voltage level depends on the application requirement.

Line regulation (LIR) can be defined as

$$\mathrm{LIR} = \frac{\Delta V_{\mathrm{REG}}}{\Delta V_{\mathrm{DD}}} + \frac{\Delta V_{\mathrm{REG}}}{\Delta V_{\mathrm{REF}}}, \tag{1.4}$$

As the LIR reduces, the dependency of regulated voltage on supply voltage and reference voltage variation decreases. Also, the LIR at reference voltage has significant impact on the LIR of the regulator, since the regulated voltage is based on reference voltage.

Load regulation (LOR) is given by

$$\mathrm{LOR} = \frac{\Delta V_{REG}}{\Delta I_L} \tag{1.5}$$

where ΔI_L is the change in dc load current. It gives the variation of regulated voltage with respect to variation of load current; smaller value means the regulated voltage variation has less dependence on load current. TC is defined as the variation of regulated voltage with respect to changing temperature. There are two main TC contributors, one from the reference voltage generator and the other one from the offset voltage of the amplifier. Finally, quiescent current is the net current flow when there is no load current and voltage variation at different temperature.

1.4 Objective

The goal of this design is to minimize the power dissipation of the LDO and voltage reference and at the same time, to maintain the objectives. Since the voltage regulator is designed for passive RFID tags, the objectives are defined according to the environment the tag is going to be, amount of energy available to tag, the internal circuit requirements and demands of the future. As seen in most of RFID applications, tags are placed in variety of environment. They can be placed at hot weather condition or put into freezer; therefore, the temperature range is set from -30°C to 50°C, and temperature coefficient should be as small as possible. As for UHF RFID application, the reading range can vary from several centimetres to several meters; as a result, the amount of

power is unstable and very limited. Since passive tags use only the energy from RF signal generated by readers, the total quiescent current should be less than 100nA to be ignorable. Due to the unstable input, the LDO regulator and its associated circuits should be able to sustain the output for input voltage range from 1.1V to 2.5V.

The available current from rectifier for UHF RFID application is from about 30uA to 50uA; thus, the load current requirement for LDO regulator is 50uA. Due to the large input variation, the LIR should be less than 1% to ensure the operation of other circuits. Table I gives the summarized objectives.

Table I. Research Objectives

Description	Specification
Input Voltage	1.1V-2.5V
Output Voltage	1V
Load Capability	50uA
Quiescent Current	<100nA
LIR	<1%
PSRR	at 100K<-40dB
LOR	<10mV/50uA
Temperature range	-30°C to 50°C
TC	<40ppm/°C
Technology: 65nm	

CHAPTER II

REVIEW OF LITERATURE

Many reference voltage generators and voltage regulators are proposed to deal with different performance issues. The major issues they focused on are temperature coefficient, line regulator and power dissipation. In section 2.1, the property of transistor operating in the subthreshold region is presented. In section 2.2, several low voltage reference voltage generators are presented. Finally, in section 2.3, three low power voltage regulators for RFID application are presented.

2.1 Transistor in the Subthreshold Region

The operation principle of transistors in the subthreshold region is illustrated in this section. By definition, the transistors with gate-source voltage lower than threshold voltage are considered operating at the subthreshold region. In most of the applications, this region is considered as "off" state, since the drain current is very small compared to other operation regions. With this low current and low operation voltage, the characteristics of transistor operating in the subthreshold region can be used for low voltage and ultra low power design. The subthreshold current is expressed as [3]

$$I_D = KI_0 \exp\left(\frac{V_{GS} - V_{TH}}{nV_T}\right)\left(1 - exp\left(-\frac{V_{DS}}{V_T}\right)\right), \qquad I_0 = \mu C_{OX}(n-1){V_T}^2, \quad V_T = K_B T/q. \tag{2.1}$$

where $I_D$is the drain current of a transistor operating in the subthreshold region, K is the aspect ratio (width/length) of a transistor, V_{GS} and V_{DS} are the gate-source voltage and drain-source voltage, respectively, n is the subthreshold slope, V_T and T are the thermal

voltage and the absolute temperature, respectively, μ and C_{OX} are the carrier mobility and gate-oxide capacitance, respectively, K_B and q are the Boltzmann constant and the elementary charge, respectively. For $V_{DS} > 4V_T$, the subthreshold current I_D is independent of V_{DS} and it is expressed as

$$I_D = KI_0 \exp\left(\frac{V_{GS} - V_{TH}}{nV_T}\right). \quad (2.2)$$

The temperature-dependent factors, threshold voltage (V_{TH}) and mobility (μ), can be expressed as

$$V_{TH} = V_{TH0} - \kappa T \quad (2.3)$$

$$\mu = \mu_0 \left(\frac{T}{T_0}\right)^{-m} \quad (2.4)$$

where V_{TH0} and μ_0 are the threshold voltage and mobility at 0°K, respectively, T and T_0 are the absolute temperature and reference temperature which is 25°C [4].

Since I_D depends on V_{GS} exponentially, the transistors have high transconductance, so they are useful for amplifier design. The derivation of small signal response is illustrated in Appendix A.

2.2 Low Power and Low Voltage Reference Circuit

In this section, several low voltage reference voltage generators are presented. They use different architectures and techniques to resolve the performance issues. The techniques they used can be separated into four basic categories, namely, voltage reference based on bandgap reference, voltage reference based on ΔV_{GS}, voltage references based on MOSFETs operated in the saturation region, and voltage references constructed by MOSFETs operated in the subthreshold region.

2.2.1 Voltage Reference Based on Bandgap Reference Circuits

Bandgap voltage references are widely used as low voltage reference [2]. The circuit can generate reference voltage independent of process, temperature and supply voltage variation. It consists of MOSFETs, substrate PNP bipolar transistors, and resistors. Figure 4 shows the conventional bandgap reference and sub 1V bandgap reference circuits. The operation principles are shown in the following.

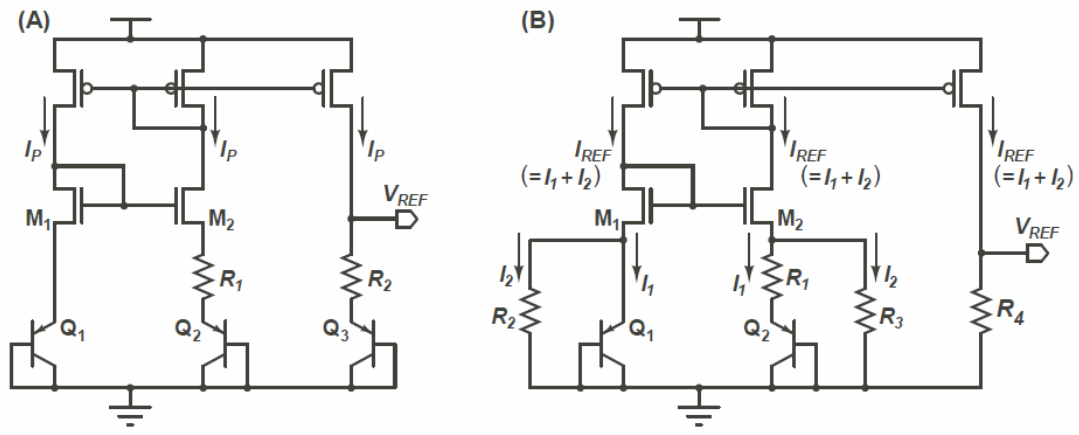

Figure 4. (A)Conventional bandgap reference [2] (B) Sub 1V bandgap reference [16]

In bipolar transistors, the collector current can be expressed as

$$I_C = KI_S \exp\left(\frac{V_{BE}}{V_T}\right), \tag{2.5}$$

where I_C and I_S are collector current and substrate current, respectively, K is the size of bipolar transistor, and V_{BE} is base-emitter voltage. In Figure 4 (A), the current I_P is controlled by bipolar transistors, Q_1 and Q_2, and resistor, R_1. It can be expressed as [2]

$$I_P = \frac{V_{BE1} - V_{BE2}}{R_1} = \frac{V_T \ln\left(K_2/K_1\right)}{R_1}, \tag{2.6}$$

Since V_T is proportional to absolute temperature (PTAT), I_P is also PATA. I_P is copied by current mirror and flows through the resistor, R_2 and the bipolar transistor, Q_3 to produce a reference voltage, which is give as [2]

$$\mathrm{V_{REF}} = \mathrm{V_{BE3}} + \mathrm{I_P R_2} = \mathrm{V_{BE3}} + \frac{\mathrm{R_2}}{\mathrm{R_1}} \mathrm{V_T} \ln\left(\frac{\mathrm{K_2}}{\mathrm{K_1}}\right). \tag{2.7}$$

V_{REF} is expressed as sum of base-emitter voltage and multiplication of thermal voltage. Since base-emitter voltage has negative TC and thermal voltage have positive TC, by adjusting the size of transistors, Q_1 and Q_2, and resistors, R_1 and R_2, the voltage level of V_{REF} is independent of temperature. Because the $\mathrm{V_{REF}}$ is based on bandgap energy of silicon, it is usually around 1.25V.

Figure 4 (B) gives a modified version of bandgap reference which can be generated reference voltage below 1V. The currents, I_1 and I_2, are given by

$$I_1 = \frac{V_{BE1} - V_{BE2}}{R_1} = \frac{V_T \ln(K_2/K_1)}{R_1}, \qquad I_2 = \frac{V_{BE1}}{R_2}, \tag{2.8}$$

The resistor, R_4, takes the current, I_{REF}, which is the sum of I_1 and I_2 and generates a output voltage which can be expressed as

$$V_{REF} = I_{REF} R_4 = \frac{R_4}{R_2} V_{BE1} + \frac{R_4}{R_1} V_T \ln\left(\frac{K_2}{K_1}\right), \tag{2.9}$$

By adjusting the ratios between resistors, the circuit can generate a reference voltage under 1V and independent of temperature. But, the power consumption of the circuits is still large. In order to achieve sub-microwatts power dissipation, the sizes of resistors should be in hundred of megaohms and the size of bipolar transistors would be large, too.

2.2.2 Voltage Reference Based on ΔV_{GS}

Figure 5 shows the schematic diagram of the reference voltage generator based on difference between gate-source voltage of PMOS and NMOS transistors [11]. The circuit consists of MOSFETs and resistors. A low-voltage bias circuit is used to generate bias current to drive reference core circuit.

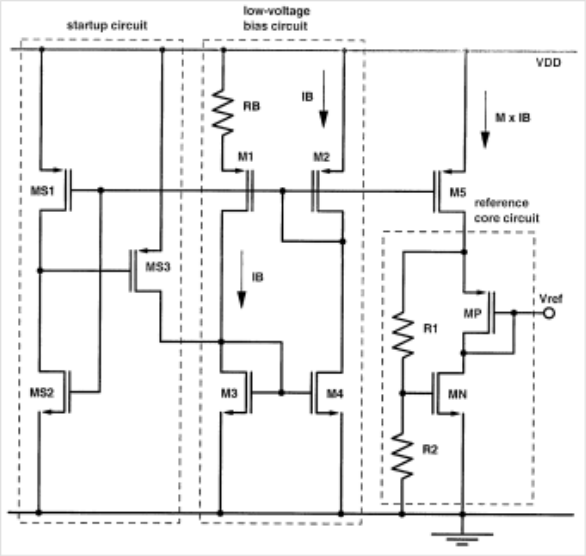

Figure 5. The schematic structure of reference voltage generator using ΔV_{GS} [11]

With bias current through transistors, MP and MN, and resistors, R1 and R2, the reference voltage is given by [11]

$$V_{REF} = (1 + \frac{R_1}{R_2})V_{GSn} - V_{GSp}, \qquad (2.10)$$

where V_{GSn} and V_{GSp} are the gate-source voltage of NMOS and PMOS transistors. Zero TC can be achieved by adjusting the sizes of resistors, R_1 and R_2, and of transistors, MP and MN. The resistor sizes are calculated according to following equation

$$\frac{R_1}{R_2} = \frac{\kappa_P}{\kappa_N} - 1, \tag{2.11}$$

where κ_P and κ_N are the temperature coefficient of threshold voltage of PMOS and NMOS transistors [11]. The effect of nonlinear terms can be minimized by adjusting the sizes of MP and MN, K_P and K_N. It can be expressed as [11]

$$\frac{K_P}{K_N} = \frac{\frac{\mu_n T_o}{\mu_p T_o}\left(\frac{T_r}{T_o}\right)^{m_p - m_n}}{\left(\frac{\kappa_P}{\kappa_N}\right)^2 \left(\frac{1}{2} + \frac{m_n}{2m_p}\right)^2}, \tag{2.12}$$

where T_o and T_r are the reference temperature and room temperature, μ_n and μ_p are the mobility of NMOS and PMOS transistors, m_n and m_p are the TC of mobility of NMOS and PMOS transistors. Since the aspect ratios of MP and MN are obtained at room temperature, a nonlinear temperature-dependent error voltage caused by TC of mobility would occur if the device did not operate at room temperature, so the temperature operation range is limited.

2.2.3 Voltage References Constructed by Saturation MOSFETs

Figure 6 shows the schematic diagram of a reference voltage generator based on MOSFETs operated at saturation region [17]. The circuit consists of only MOSFETs. The transistors, M_1 and M_2, operate in the subthreshold region, and M_3 to M_8 operate at saturation region. The bias current I_B can be expressed as [17]

$$I_B = \frac{\mu C_{OX}}{2} n^2 {V_T}^2 K_4 ln^2 \left(\frac{K_2}{K_1}\right)\left(\frac{\sqrt{K_3}}{\sqrt{K_3} - \sqrt{K_4}}\right). \tag{2.13}$$

Then, transistors, M_5 to M_8, accept bias current I_B and produce a reference voltage which can be expressed as [17]

$$V_{REF} = V_{GS8} + V_{GS5} - V_{GS7}$$

$$= V_{TH} + nV_T ln\left(\frac{K_2}{K_1}\right)\left(\frac{\sqrt{K_3}}{\sqrt{K_3}-\sqrt{K_4}}\right)\left(\frac{1}{\sqrt{K_8}}\left(1+\sqrt{\frac{K_6}{K_5}}\right)-\frac{1}{\sqrt{K_7}}\right). \quad (2.14)$$

Since V_{TH} and V_T have opposite TC, a reference voltage with zero TC can be obtained by carefully adjusting the aspect ratios of the transistors M_1 to M_8. Because transistors, M_3 to M_8, operate in saturation region, the aspect ratios of them needs to be carefully adjusted to keep the operation.

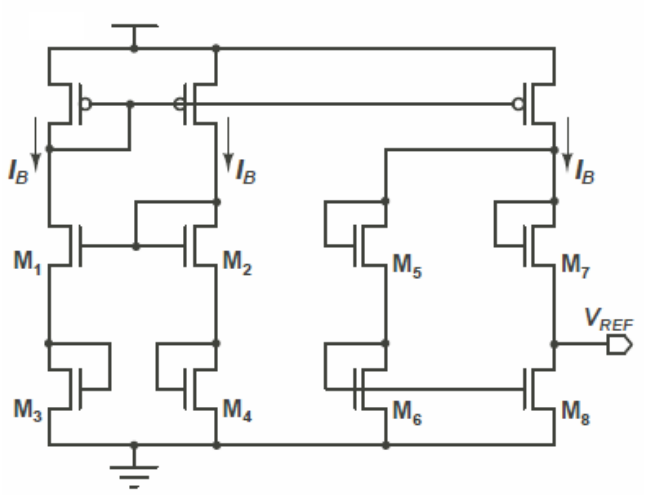

Figure 6. A Reference voltage generator work at saturation region [17]

2.2.4 Voltage References Constructed by Subthreshold MOSFETs

A reference voltage generator consisted of subthreshold MOSFETs is proposed in [12]. Figure 7 gives the schematic of the reference voltage generator. Through the self-biased current mirror, the currents, I_A and I_B, can be expressed as [12]

$$I_A = \frac{1}{R_2} nV_T ln\left(\frac{K_9}{K_8}\right), \quad I_B = \frac{V_{GS3}}{R_1} - I_A \frac{K_5}{K_6}, \quad (2.15)$$

The output voltage, V_R, is a function of, I_A and I_B, and can be expressed as [12]

$$V_R = \left(\frac{K_{10}}{K_7} I_A + \frac{K_{11}}{K_2} I_B\right) R_3$$
$$= \frac{K_{11}}{K_2}\frac{R_3}{R_1} V_{GS3} + \left(\frac{K_{10}}{K_7} - \frac{K_{11}K_5}{K_2K_6}\right)\frac{R_3}{R_2} nV_T ln\left(\frac{K_9}{K_8}\right). \quad (2.16)$$

Since V_{GS3} and V_T have opposite TC, the temperature variation would have less effect on V_R by carefully adjusting the ratio of transistors and resistors.

However, the TC is large because of the non-linear temperature-dependent voltage of V_{GS3}. Furthermore, the power dissipation of the circuit is high, or the circuit can achieve nanowatts power consumption by using resistors with hundreds of megaohms, such that the chip area will be very large.

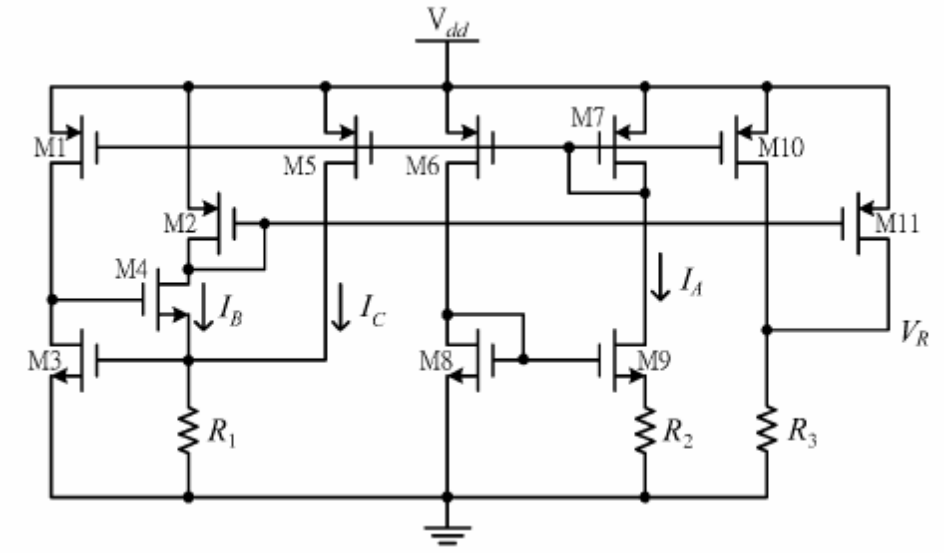

Figure 7. Reference voltage generator working in subthreshold with channel-length modulation compensation [12]

Figure 8 shows the other design of reference voltage generator with all of the transistors operated in the subthreshold region [15]. The circuit consists of three kinds of MOSFET transistors, namely, NMOS transistors with two different threshold voltages

and PMOS transistors. The characteristic equation for current I_{10} is obtained mathematically by compensating the TC of the voltage across the diode connected transistor, M_{10}. In order to have V_{REF} free from temperature variation, transistors, M_1, M_2 and M_3, are used to generate I_{10} physically. Since $V_{GS2} - V_{GS3} = V_{GS1}$, the current, I_1, can be expressed as [15]

$$I_1 = Q^{1/\Sigma_n} u C_{OX} V_T{}^2 \exp\left(-\frac{\Delta V_{TH}}{V_T \Sigma_n}\right), \tag{2.17}$$

$$\Delta V_{TH} = V_{TH1} + V_{TH3} - V_{TH2},$$

$$Q = \left(\frac{K_7}{K_5}\right)^{n_2 - n_3} \left(\frac{(K_3 C_{OX3})^{n_3} (K_1 C_{OX1})^{n_1}}{(K_2 C_{OX2})^{n_2}}\right),$$

$$\Sigma_n = n_1 + n_3 - n_2.$$

The current, $I_{10} = I_1 \times K_9/K_5$, passes through diode connected transistor, M_{10}, to produce a reference voltage, V_{REF} which is expressed as

$$V_{REF} = V_{TH10} + n_{10} V_T \ln\left\{Q^{\frac{1}{\Sigma_n}} \frac{K_9}{K_5 K_{10} C_{OX10}}\right\} - \frac{n_{10}}{\Sigma_n} \Delta V_{TH}. \tag{2.18}$$

Because the equation consists of the threshold voltages, V_{TH10} and ΔV_{TH}, with negative TC and thermal voltage with positive TC, a reference voltage with zero TC can be obtained by careful adjustment of aspect ratios of transistors [15]. The resulting TC is 142ppm/°C, and the power dissipation is only 2.6nW. Although, the power dissipation is very low, the TC coefficient is still too large and the reference voltage generator requires two kinds of NMOS transistors such that the mask cost is doubled.

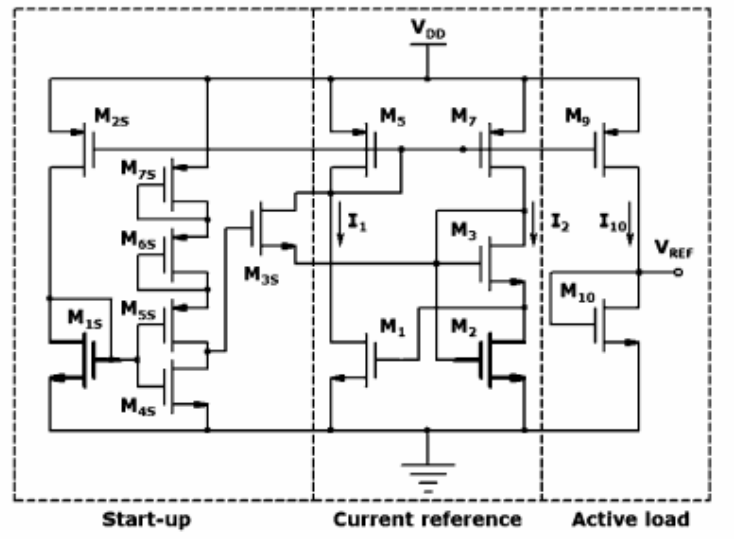

Figure 8. Reference voltage generator with temperature compensation using transistors with different threshold voltage

2.3 Low Power Voltage Regulator

Error! Reference source not found. illustrates the schematic diagram of a LDO oltage regulator for RFID application [7]. It consists of a temperature stabilizer (TS), ripple stability (RS), fixed voltage reference (FVR), operational amplifier (OPA), and a load circuit. The circuit is constructed using bipolar transistors, MOSFET transistors, resistors, and a large capacitor. The operation principle of LDO voltage regulator was demonstrated in Chapter I. The OPA consists of a differential amplifier. This literature uses a PMOS, M_{Pass}, as the pass device. The feedback network consists of two resistors and creates feedback signal V_s to OPA. The reference voltage generator of the device consists of TS, RS and FVR. A pair of cascade self biased low voltage current source is used as RS, and the MOSFET transistors in RS are operating at saturation region. The RS generates a bias current I_{reg} passing through FVR; then, FVR creates a reference voltage free from supply variation.

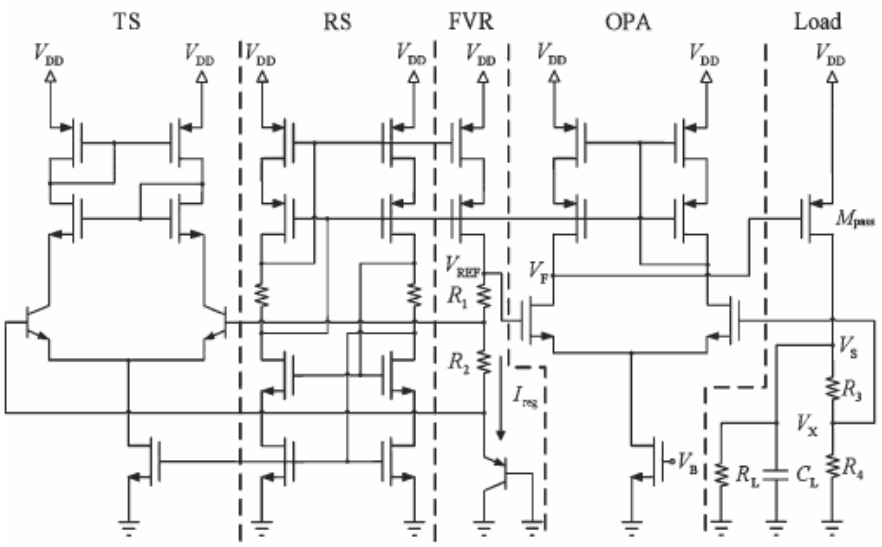

Figure 9. Schematic of LDO voltage regulator with ripple reduction and temperature compensation [7]

Temperature stabilizer, TS, consists of self bias current mirror using MOSFET transistor and a differential pair constructed by bipolar transistors to generate a ΔV_{BE} which has positive TC. ΔV_{BE} is expressed as [7]

$$\Delta V_{BE} = V_T \ln(n) \tag{2.19}$$

$$\frac{\delta \Delta V_{BE}}{\delta T} = \frac{K_B}{q} \ln(n) \tag{2.20}$$

where n is the ratio between currents flow through each bipolar transistors. The variable, n, can be controlled by adjusting the aspect ratios of the transistors in self bias current mirror. The negative TC generated by V_{BE} of the bipolar transistor at bottom of FVR can be expressed as [7]

$$\frac{\delta V_{BE}}{\delta T} = \frac{V_{BE} - (3+m)V_T - E_g/q}{T} \tag{2.21}$$

where $E_g$is the bandgap energy of silicon which is about 1.12eV. The reference voltage can be represented as sum of V_{BE} and multiplication of ΔV_{BE}, that the function for reference voltage is given by [7]

$$V_{REF} = \left(1 + \frac{R_1}{R_2}\right)\Delta V_{BE} + V_{BE} \tag{2.22}$$

From (2.20) , (2.21) and (2.21) the overall TC is expressed as [7]

$$\frac{\delta V_{REF}}{\delta T} = \left(1 + \frac{R_1}{R_2}\right)\frac{K_B}{q}\ln(n) + \frac{V_{BE} - (3+m)V_T - E_g/q}{T} \tag{2.23}$$

In order to achieve zero TC around room temperature, the ratio, R_1/R_2, has to be adjusted according to (2.23). The result shows that TC is about 200ppm/°C and LIR is 12mV/V. Due to the non-linear temperature-dependent error voltage, the TC is relatively large.

Figure 10 shows the schematic of the reference voltage generator proposed in [6]. It consists of a voltage-current convertor, a reference core and a low-pass filter. The device is built by MOSFET transistors and resistors. The circuit utilizes the concept of zero temperature coefficient point in diode connected NMOS transistors. The reference voltage can be expressed as [6]

$$V_{REF} = V_{THN} + \sqrt{2I_{D15}/[\mu_n C_{OX}(K_{15})]}, and\ I_{D15} = \frac{V_{REF}}{R_1}, \tag{2.24}$$

$$V_{REF} = V_{THN} + \sqrt{2V_{REF}/[\mu_n C_{OX}(K_{15})R_1]}, \tag{2.25}$$

$$K_{15} = \frac{I_{D15}}{2\mu_n C_{OX}\kappa^2}\left(\frac{m}{\mu_n} + \frac{t_{c1}}{R_1}\right), \tag{2.26}$$

Where $t_{c1} = -8.34 \times 10^{-4}$. Once I_{D15} and R_1 are designed, the size of M_{15} can be determined. Thus, the reference voltage is independent of temperature.

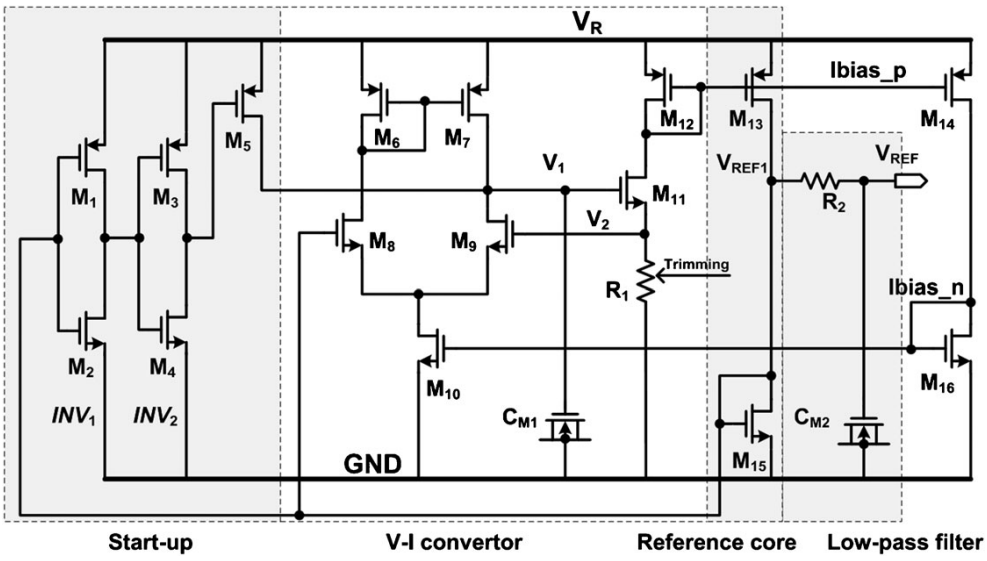

Figure 10. Schematic of reference voltage generator in reference [6]

Figure 11 shows the schematic diagram of the LDO regulator used in this device. Accompany with reference voltage generator, the regulator can generate stable output. The result shows that, TC is 43ppm/°C, LIR is 22mV/V, LOR is 20mV/50uA and the quiescent current is 700nA which consumes a lot of power.

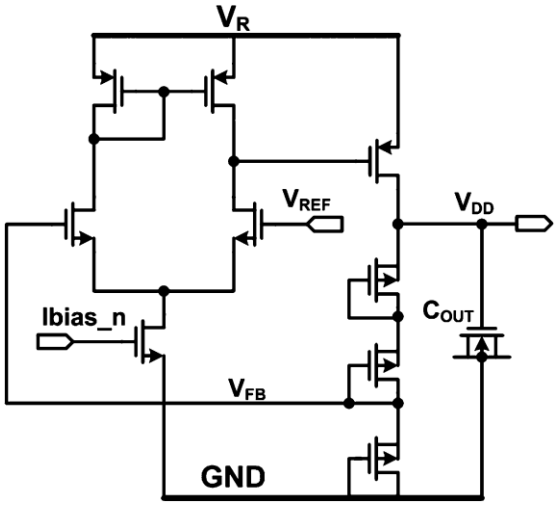

Figure 11. Schematic diagram of LDO regulator [6].

Figure 12 shows the schematic for ultra low power LDO voltage regulator [8]. The LDO regulator can be separated into two parts: a reference voltage generator and a series voltage regulator. The reference voltage generator consists of a self biased current source and reference circuit, and LDO regulator consists of a single differential amplifier, NMOS pass transistor and load capacitor. There is no feedback network, since the amplifier directly compares the output of the regulator with reference voltage.

Due to the special application that the regulator is going to use, the device does not use any temperature compensation technique. TC is -2000ppm/°C. The quiescent current is 34nA which is a very small value. The LIR is 0.8mV/V. The major disadvantage is the absence of temperature compensation.

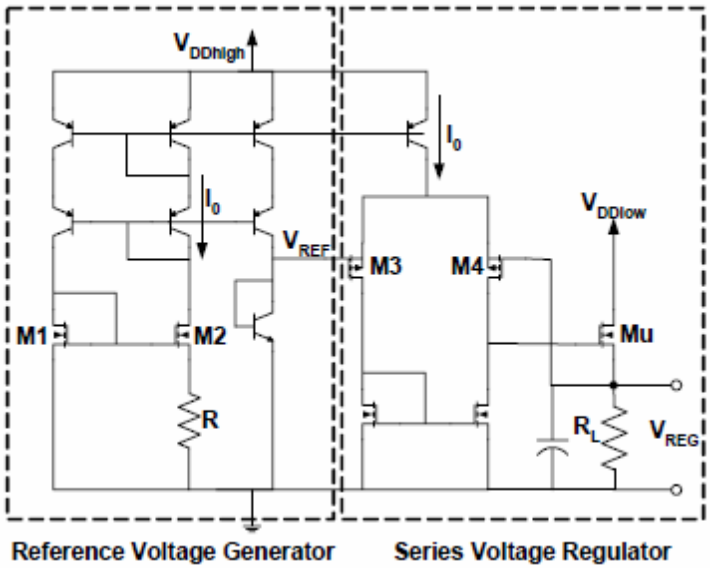

Figure 12. Schematic for ultra low power LDO Voltage Regulator [8]

CHAPTER III

DESIGN CONSIDERATION

3.1 Reference Voltage Generator

As an ideal reference voltage generator in RFID system, it is expected to achieve constant DC voltage level independent of the amount of power received by antenna and temperature variation. The supply voltage provided by rectifier usually contains voltage ripple, wide range of input voltage and temperature-dependent, so the reference voltage has to be able to overcome the variations and to provide a constant voltage. The amount of energy received by a tag is very limited, so the reference voltage generator should consume energy in nanowatts range. Moreover, the level of reference voltage should be designed according to regulator requirement. Because the objective for regulated voltage is 1 volt and LDO voltage regulator is the topology that is chosen, the reference needs to be less than 1 volt. The temperature coefficient for reference voltage should be as low as possible, because temperature coefficient of regulated voltage from LDO regulator has high dependency to it.

Due to very low voltage supply and low voltage requirement on reference voltage, bandgap reference which has reference voltage about 1.2V[2] is not suitable for this situation. Therefore, new method of temperature compensation with reference voltage less than one volt is required. There were many techniques shown in previous literatures. Sub-1V bandgap reference was proposed to deal with the low voltage issue and to keep the advantage of conventional bandgap reference at the same time [16]. However, the power consumption is too large, so they need resistors with hundreds of megaohms to

achieve sub-microwatt operation. A resistor with that side is very area consuming. There is voltage reference generator designed based on ΔV_{GS} [11]. It reduces TC by controlling the difference between gate voltage of PMOS and NMOS and adjusting the ratio between resisters. Since the gate-source voltage contains nonlinear temperature-dependent error, it can only work at the temperature around room temperature. Moreover, The power consumption is high.

A low power voltage reference utilizes the properties of MOSFET transistors operating in saturation region [17]. It utilizes the opposite TC from threshold voltage and multiplication of thermal voltage to generate a reference voltage free from temperature variation, but the aspect ratios of transistors need to be precise to ensure the operation. Some low power voltage reference generators utilize the properties of subthreshold MOSFET. In [12], it did not only utilize positive TC of V_T and negative TC of V_{GS} but also adjusted them by control the aspect ratio of transistors and the size of transistors to achieve zero TC. Nevertheless, the power dissipations were still large. In order to achieve sub-microwatt operation, this circuit requires resistors with very high resistance values. In [13] and [15], they achieved zero TC by using the difference between two V_{TH} values. From what has been discussed above, we can come to a conclusion that two types of transistors with different threshold voltages are required, thus, the mask cost for chip production will be doubled.

3.2 Series Voltage Regulator

There are great amount of topologies used for building voltage regulator can be generally classified into two major categories, switch regulators and linear regulators.

Depending on the application, they can be used at different places. Furthermore, both advantages and disadvantages of regulators in different categories will be discussed in this section. Finally, some of the previous literatures on voltage regulator for RFID application will be presented.

In RFID application, a voltage regulator circuit with simple structure and low power dissipation is needed for low voltage operation. Switching regulators operate with higher efficiency than linear regulators at high power applications, because the former converts power while the latter wastes power. However, switching regulators consume more power at ultra low power applications, because an extra clock signal is required and it requires inductance which is very area consuming, such that, they are not desired for low power operation [10]. In linear regulators, shunt voltage regulators have only small sensitivity to variations of the supply voltage, and they have undesired current flowing through shunt resistors. Therefore, Due to the ultra-low-power and low-cost condition, series voltage regulators, so called low-dropout (LDO) regulator, is suitable as power management circuit for RFID operation.

A LDO consists of an operational amplifier (OPA), a pass device, feedback circuit and a large capacitor. Ideally, OPA compares the output voltage (V_{REG}) with reference voltage (V_{REF}) and produces an error signal that can drive the pass device to keep V_{REG} at constant level. Therefore, V_{REG} should be robust against supply voltage variation, load current variation and temperature variation. A large capacitor is used as energy storage; also, it can serve as a low pass filter to minimize the voltage ripples and improve the stability of output signal.

First, we consider the effect of supply voltage variation. It is the major contributor to LIR. Figure 2 shows the LDO regulator as a close loop feedback circuit. From it, we are able to derive a close feedback loop to illustrate the effect of supply voltage variation to regulated output voltage. The feedback loop is shown on Figure 13. The variation is given by

$$\frac{\Delta V_{REG}}{\Delta V_{DD}} = \frac{P_1}{1 + P_2 A_V F_B} \cong \frac{P_1}{P_2 A_V F_B}, \tag{3.1}$$

where P_1 and P_2 are the voltage gain from ΔV_{DD} to ΔV_{REG} and output of OPA to ΔV_{REG}, A_V is the voltage gain of OPA, and F_B is the gain of feedback network. Usually, the pass device is a single PMOS transistor; therefore, P_1 and P_2 cancel each other, and F_B is a fixed component depending on the relationship between reference voltage and regulated voltage. Finally, A_V plays the most important role in equation (3.1); thus, a higher A_V can introduce a lower LIR value. Therefore, an OPA with high voltage gain is desired in this application.

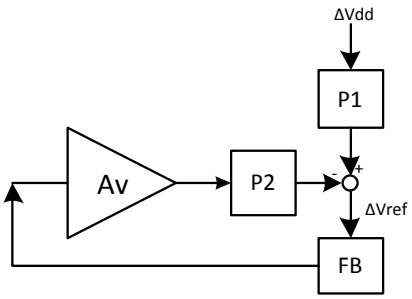

Figure 13. Supply voltage to regulated voltage feedback loop

Reference voltage variation also has great impact on the stability of the regulated voltage. It is also another source of LIR. The relationship between reference voltage variation and regulated voltage variation can be derived from the feedback loop. The

schematic of the feedback loop is shown in Figure 14. As a close loop feedback circuit, the gain of voltage variation can be expressed as

$$\frac{\Delta V_{REG}}{\Delta V_{REF}} = \frac{A_V P_2}{1 + A_V P_2 F_B} \cong \frac{1}{F_B}. \tag{3.2}$$

Since F_B is a fix number, the effect of reference voltage variation to regulator output is independent from regulator structure. It is important to have a stable reference voltage. Similarly, load current can change the output voltage level. In the close loop system, it can be expressed as

$$\frac{\Delta V_{REG}}{\Delta I_L} = \frac{R_{o,Pass}}{1 + A_V P_2 F_B}. \tag{3.3}$$

where $R_{o,Pass}$ is the output resistance of the pass device. The stability can be improved as A_V increases and output resistance of pass device reduces. Moreover, there are some more non-ideal factors, such as bias current variation and offset voltage for amplifier, which can affect the performance of the LDO voltage regulator. As consequence, we also have to consider those effects in the design process.

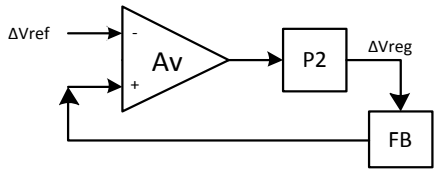

Figure 14. Reference Voltage to Regulated Voltage Feedback Loop

Reference [7] uses self-bias cascade current mirror to reduce supply voltage ripple, and it reduces the effect of TC by combining multiplication of ΔV_{BE} and V_{BE} that they have opposite TC. Attributed to the nonlinear temperature-dependent voltage, the

temperature operation range is small and the resulting TC is high. Also, the power consumption is high. It can achieve nanowatts operation only by using large size of bipolar transistors and resistors; such that, the chip area increases dramatically.

The property of zero-temperature coefficient on NMOS transistor is utilized to obtain a reference voltage independent of temperature [6]. The regulator uses low pass filter to eliminate the effect of voltage ripple. Due to multiple amplifiers used in the circuit, the quiescent current, which is 700nA, is still higher than the one in the objective. Reference [8] also uses self-biased cascade current mirror to reduce the effect of supply voltage variation, but the regulator lacks a temperature compensation technique; thus, the TC is -2000ppm/°C which is much worse than what we want to achieve.

From what has been discussed above, we can draw a conclusion that the LDO voltage regulator for RFID application should be capable of eliminating the effects from supply voltage ripple, temperature variation and load current variation. Also, while all these objectives have to be met, the circuit should consume power in nanowatts level.

CHAPTER IV

CIRCUIT IMPLEMENTATION AND OPTIMIZATION

The circuit implementation is separated into two parts, sub 1V reference voltage generator and series voltage regulator. The main contributions for voltage reference are transistors resizing for the circuit proposed in [14] and optimizing the quiescent current to a value much less than the value previously reported while all the objectives are met. The regulator is fully designed in MOSFET transistors without any bipolar transistors or resistors; such that, the area and power dissipation can be minimized. Both the reference voltage generator and the series voltage regulator are implemented by using MOSFET transistors operated in the subthreshold region to further reduce power consumption and to minimize TC of output voltages. The subthreshold current of a transistor can be expressed as

$$I_D = KI_0 \exp\left(\frac{V_{GS} - V_{TH}}{nV_T}\right), \qquad \text{for } V_{DS} > 4V_T. \tag{4.1}$$

Section 4.1and 4.2 illustrate the implementation with optimization of sub 1V reference voltage generator and series voltage regulator, respectively.

4.1 Sub 1V Reference Voltage Generator

A sub 1V reference voltage generator is implemented and optimized in this section. The circuit consists of transistors operating in the subthreshold region. The aspect ratios of the transistors are defined according to the objectives such as TC and LIR. Section 4.1.1 gives the detail of implementing the reference circuit, and section 4.1.2 explains the ways to obtain optimized aspect ratios.

4.1.1 Reference Circuit Implementation

In order to resolve low power and low voltage issues, the reference circuit consists of MOSFETs operating in the subthreshold region. Although the operation principle comes from [14], the structure of the circuit is slightly modified, and the sizes of the transistors are optimized to have minimum power dissipation which is much less than the value proposed in [14].

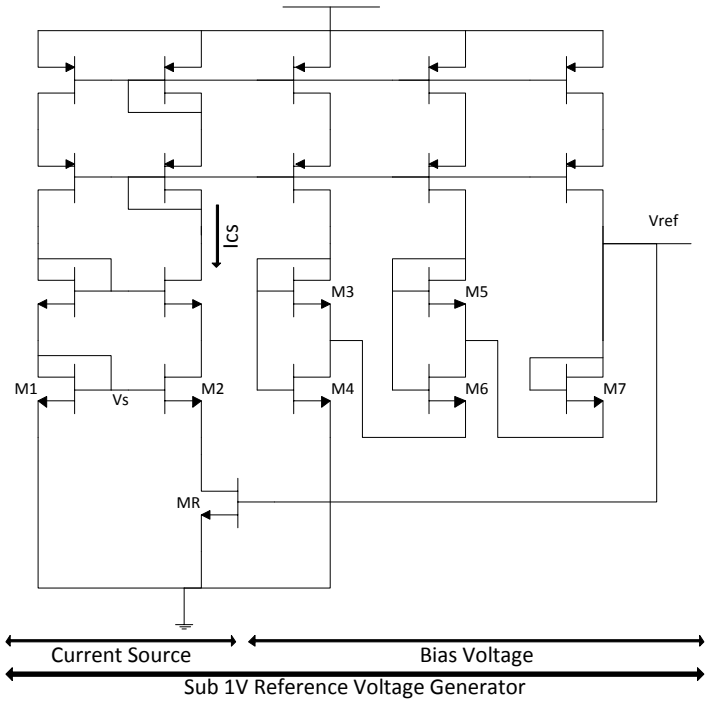

Figure 15. Schematic of Voltage Reference Generator

Figure 15 gives the schematic diagram of the sub 1V reference voltage generator. The circuit can be separated into two parts, current source subcircuit and bias voltage subcircuit. The operation principle of the reference is that the current source subcircuit generates a stable bias current I_{CS}. The bias voltage subcircuit accepts I_{CS} through PMOS current mirror and produces a reference voltage, V_{REF}. Then, V_{REF} feedbacks to M_R as gate-source voltage in current source subcircuit to form a close loop. All the transistors

work in the subthreshold region expect M_R, which is in deep-triode region, so the quiescent current and power consumption can be minimized while chip area can be reduced and low voltage operation is assured.

The temperature-compensation technique comes from the combination of two opposite TCs. This circuit takes the sum of a negative TC from threshold voltage and multiplication of positive TC from thermal voltage to generate a reference voltage independent of temperature variation. Also, TC of I_{CS} has to be able to cancel the TC of I_0 to eliminate a nonlinear temperature-dependent error current from I_0; thus, the multiplication factor on thermal voltage can be independent of temperature.

The current source subcircuit utilizes the property of a self-biasing current mirror to generate a stable bias current I_{CS}, but instead of having a large resistor, transistor M_R operates as MOS resistor. Ideally, supply voltage variation should not affect the current of self-bias current mirror, but due to Drain Inducted Barrier Lowering (DIBL), body effect and other second order effects, I_{CS} is not a constant value and varies with supply voltage. As a result, some optimization techniques are required to generate a stable I_{CS}.

The current I_{CS} is controlled by three major transistors (M_1, M_2 and M_R). The drain currents flowed through transistors, M_1, M_2 and M_R can be assumed to be equal because of a PMOS current mirror on top of them. Since $V_{GS} = V_{TH} + nV_T \ln(I_D/KI_0)$, I_{CS} can be derived as follow [14]

$$V_{GS1} = V_{GS2} + V_{DSR},$$

$$V_{TH1} + nV_T \ln\left(\frac{I_{CS}}{K_1 I_0}\right) = V_{TH2} + nV_T \ln\left(\frac{I_{CS}}{K_2 I_0}\right) + I_{CS} R_{M_R}. \qquad (4.2)$$

where V_{GSi} is the gate-source voltage of transistor M_i. By assuming $V_{TH1} = V_{TH2}$, we have

$$I_{CS} = \frac{1}{R_{M_R}} \times nV_T \ln\left(\frac{K_2}{K_1}\right), \tag{4.3}$$

$$R_{M_R} = \frac{1}{K_R \mu C_{OX}(V_{REF} - V_{TH})}, \tag{4.4}$$

where R_{M_R} is the MOSEFT resistance of M_R [14]. Therefore, from (4.2), (4.3) and (4.4), the current I_{CS} can be expressed as [14]

$$I_{CS} = \mu C_{OX}(V_{REF} - V_{TH}) nV_T K_R \ln\left(\frac{K_2}{K_1}\right). \tag{4.5}$$

From the expression, I_{CS} can be adjusted by modifying the aspect ratios of transistors, M_R, M_1 and M_2. Also, the V_{REF} has control over this current.

The bias voltage subcircuit consists of transistors, M_3 to M_7, and PMOS transistors of the current mirror. The transistors, M_3 to M_7, produce a reference voltage V_{REF} by accepting the current, I_{CS}. The reference voltage is the combination of gate-source voltage and is given by [14]

$$\begin{aligned} V_{REF} &= V_{GS4} - V_{GS3} + V_{GS6} - V_{GS5} + V_{GS7} \\ &= V_{TH} + nV_T \ln\left(\frac{6I_{CS}}{I_0}\frac{K_3 K_5}{K_4 K_6 K_7}\right). \end{aligned} \tag{4.6}$$

At this state, the mismatch between threshold voltages of transistors is assumed to be ignorable. The voltage level of the reference voltage depends not only on the aspect ratios of transistors, but also on the bias the current, I_{CS}.

In order to obtain zero TC for V_{REF}, first we have to identify the temperature-dependent factor of threshold voltage which can be expressed as

$$V_{TH} = V_{TH0} - \kappa T, \tag{4.7}$$

where V_{TH0} and κ are the threshold voltage at temperature 0K and the TC of threshold voltage, respectively. From Equation (4.5), (4.6) and (4.7), V_{REF} can expressed as [14]

$$V_{REF} = V_{TH0} - \kappa T + nV_T \ln\left[\frac{6n(V_{REF} - V_{TH})}{(n-1)V_T}\frac{K_3K_5}{K_4K_6K_7}K_R\ln\left(\frac{K_2}{K_1}\right)\right]. \quad (4.8)$$

The V_{REF} is expressed as the sum of threshold voltage and multiplication of thermal voltage. These two voltages have opposite TC; such that zero TC for V_{REF} is possible to be obtained by carefully adjusting the aspect ratios of transistors. The expression for TC of V_{REF} is the derivation of (4.8) with respect to T, and is given by

$$\frac{\delta V_{REF}}{\delta T} = -\kappa + \frac{nK_B}{q}\ln\left[\frac{6nq\kappa}{(n-1)K_B}\frac{K_3K_5}{K_4K_6K_7}K_R\ln\left(\frac{K_2}{K_1}\right)\right], \quad (4.9)$$

where we assume that $(V_{REF} - V_{TH}) \ll \kappa T$ and $nV_T \ll \kappa T$ [14], so zero TC can be obtained by set $\delta V_{REF}/\delta T = 0$, and the aspect ratios can be expressed as [14]

$$-\kappa + \frac{nK_B}{q}\ln\left[\frac{6nq\kappa}{(n-1)K_B}\frac{K_3K_5}{K_4K_6K_7}K_R\ln\left(\frac{K_2}{K_1}\right)\right] = 0,$$

$$\frac{K_3K_5}{K_4K_6K_7}K_R\ln\left(\frac{K_2}{K_1}\right) = \frac{(n-1)K_B}{6nq\kappa}\exp\left(\frac{\kappa q}{nK_B}\right). \quad (4.10)$$

Zero TC could be achieved by setting aspect ratios to proper values according to (4.10). From equation (4.7) and (4.10), the optimum reference voltage is

$$V_{REF} = V_{TH0}. \quad (4.11)$$

The optimum reference voltage is equal to threshold voltage at 0K. From (4.5), (4.7) and (4.11), the current, I_{CS}, with optimum reference voltage can be expressed as [14]

$$I_{CS} = \mu C_{OX}\kappa T n V_T K_R \ln\left(\frac{K_2}{K_1}\right). \quad (4.12)$$

As a result, if V_{REF} is independent of temperature, the current I_{CS} from current source is independent from V_{REF} and depends only on aspect ratios of M_1, M_2 and M_R.

4.1.2 Reference Circuit Optimization

Due to the enormous amount of parameters affecting the model of MOSFET transistors in 65nm technology, we can only approximate the aspect ratios of transistors in course source and bias voltage subcircuit from expressions from previous section, but because of the unclear body bias on M_2, the approximation from (4.10) is not accurate. The general optimization steps are shown below. First, since we already know the intended reference voltage, V_{REF}, which is shown in (4.11), we can first find the optimized I_{CS} value by identifying the optimized aspect ratios of transistors in current source subcircuit from both calculation and simulations. Then the optimized I_{CS} and the extracted parameters from model of CMOS 65nm technology are substituted to equation (4.6). A better approximation of the aspect ratios can be obtained. Finally, with further simulation, the exact aspect ratios for having reference voltage independent from temperature can be obtained.

The first step in optimization is to find the optimum I_{CS} from current source subcircuit. The stability of I_{CS} has direct impact on V_{REF}; therefore, a constant I_{CS} is desired. However, due to the second order effect of transistors and large variation of supply voltage, the use of cascade current mirror is important for self-biased current mirror to stabilize I_{CS}. With the consideration on the DIBL effect of NMOS and PMOS transistors operated in subthreshold region, the expression for subthreshold current is given as

$$I_D = KI_0 \exp\left(\frac{|V_{GS}| - |V_{TH}|}{nV_T}\right) \exp\left(\frac{\eta |V_{DS}|}{nV_T}\right), \qquad (4.13)$$

where η represents the DIBL coefficient of transistor operating in the subthreshold region. If only one pair of PMOS current mirror is used instead of cascade current mirror, the

ratio, m, which is the ratio between currents on two branches of the current mirror, can be expressed as

$$m = \exp\left(\frac{\eta_P\left(V_{DD} - V_{GS1} - V_\gamma\right)}{nV_T}\right), \tag{4.14}$$

where $\eta_P$is the DIBL coefficient for PMOS transistor and V_γ is the voltage across diode-connected PMOS transistor that it is proportional to the supply voltage, V_{DD}. The expression of current I_{CS} is given by

$$I_{CS} = \mu C_{OX} \kappa Tn V_T K_R \ln\left(m\frac{K_2}{K_1}\right). \tag{4.15}$$

The variation of V_{GS1} is much smaller than the variation of supply voltage, V_{DD}. When V_{DD} varies between its maximum and minimum values, m changes between m_{max} and m_{min} causing the variation on current I_{CS}. As the consequence, the variation of I_{CS} due to DIBL effect can be approximated

$$\frac{\Delta I_{CS}}{I_{CS}} = \frac{\ln\left(m_{max}/m_{min}\right)}{\ln\left(K_2/K_1\right)}. \tag{4.16}$$

With large variation of supply voltage and limited power availability, the use of cascade current mirror is inevitable, although it leads to a reduction of dynamic range. In previous paper, they use an extra differential amplifier to equalize the current flow on two branches of current mirror instead of cascade current mirror to stabilized I_{CS}, thus the quiescent current increases substantially.

The same principle also applies to NMOS current controller consisting of M_1, M_2 and M_R. The current I_{CS} variation caused by DIBL effect of current controller can be approximated as

$$\frac{\Delta I_{CS}}{I_{CS}} = \frac{\eta_N (V_{DD,max} - V_{DD,min})}{nV_T \ln (K_2/K_1)}, \quad (4.17)$$

where η_N is the DIBL coefficient for NMOS transistor. The effect is stronger, since nV_T is a small number, so a cascade NMOS current mirror has to be used to reduce the DIBL effect. With these cascade current mirrors, the current I_{CS} depends less on V_{DD}.

From (4.12), it seems that by choosing smaller K_2/K_1 would lead to lower I_{CS} and smaller size of M_R, but from (4.16), (4.17) and further simulation, both aspect ratios of M_1 and M_2 as well as K_2/K_1 have significant impact on stability of I_{CS}. Figure 16 demonstrates the simulation result for $\Delta I_{CS}/I_{CS}$ as function of the ratio, K_2/K_1, with different transistor widths as parameters. Variation of I_{CS} reduces as the value of K_2/K_1 increases. Furthermore, a decrement in width of M_1 also leads to the reduction of I_{CS} variation. With more simulation and analysis, we set K_2/K_1 to 1.5 with the width of M_1 (W_1) and channel length to 0.2um and 3um, respectively. The $\Delta I_{CS}/I_{CS}$ is approximately 0.44%, which is much lower than one percent.

The second reason to choose the width of M_1 to 0.2um is related to the voltage operation region of the current source. The maximum operation voltage depends on the aspect ratios of the transistors, M_1 and M_2. If the ratio reduces, the maximum operation voltage would increases. Figure 17 illustrates the effect of supply voltage on I_{CS}. As W_1 reduces (the width of M_2, W_2, is the multiplication of W_1 and W_2/W_1 is 1.5 in Figure 17), the maximum supply voltage for correct operation increases. In order to have higher operational voltage, W_1 has to be small enough. Also, we have to consider the effect of temperature operation region. Since I_{CS} increases with temperature, the maximum operation voltage reduced. In order to have desired maximum operation voltage at 50°C, the simulation shows that the better choice is set W_1 to 0.2um.

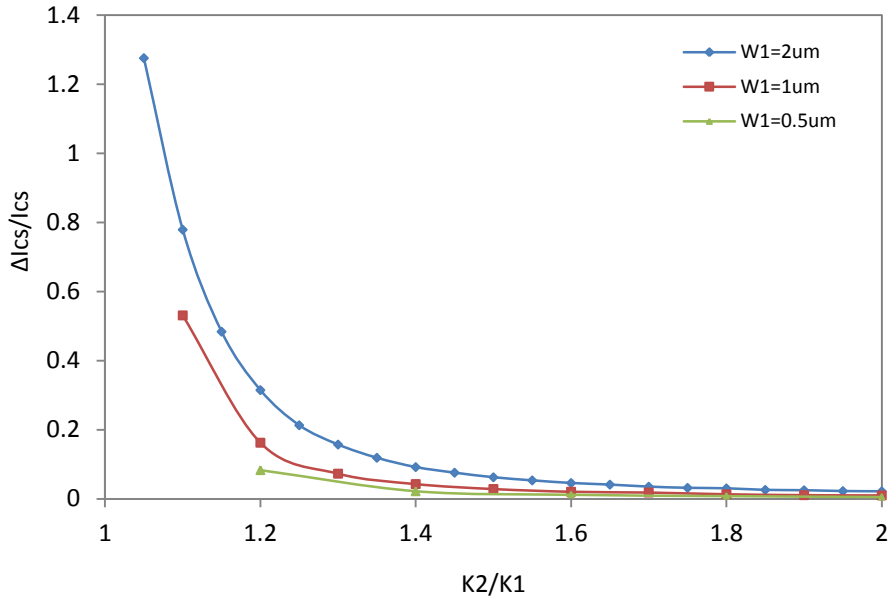

Figure 16. $\Delta I_{CS}/I_{CS}$ as function of K_2/K_1 with width of M_1 and M_2as parameters.

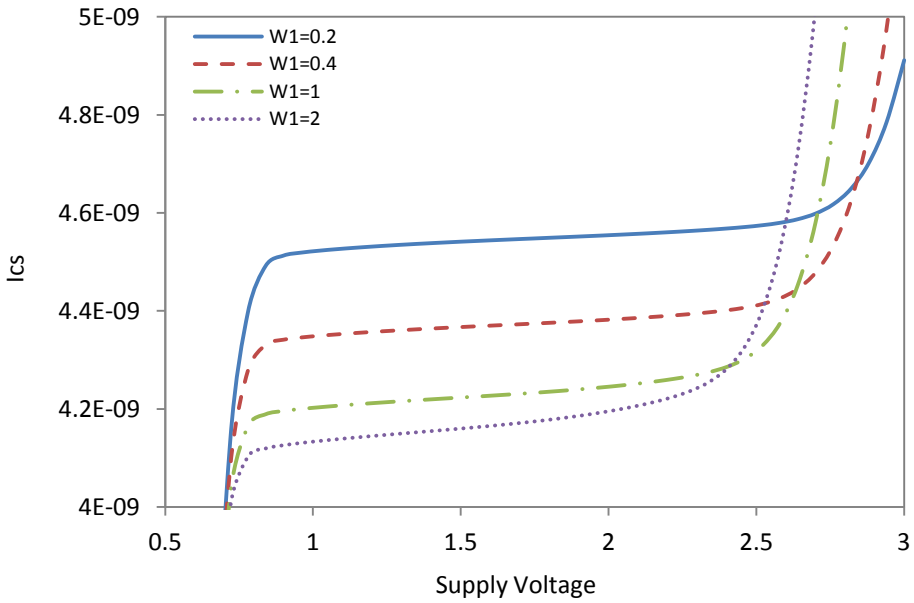

Figure 17. I_{CS} as function of supply voltage with width of M_1as parameter

Furthermore, we have to consider the body effect. Since body bias has small effect on the TC of threshold voltages, the zero TC can still be obtained, but aspect ratios

of transistors have to go through some minor changes. With body bias, current I_{CS} is given by

$$I_{CS} = \frac{1}{R_{M_R}} \times \left[\Delta V_{TH} + nV_T \ln\left(\frac{K_2}{K_1}\right)\right], \tag{4.18}$$

where ΔV_{TH} is the difference between threshold voltage of transistors M_1 and M_2. The body biases of transistors, M_3 to M_7, have little to no effect on overall system due to the structural advantage of the bias voltage subcircuit. Such that, from expressions (4.8) and (4.19), the reference voltage can be expressed as

$$V_{REF} = V_{TH0} - \kappa T + nV_T \ln\left\{\frac{6n(V_{REF} - V_{TH})}{(n-1)V_T} \frac{K_3K_5}{K_4K_6K_7} K_R[\Delta V_{TH} + \ln\left(\frac{K_2}{K_1}\right)]\right\}. \tag{4.19}$$

Because the TCs of the V_{TH1} and V_{TH2} are almost the same even with body effect [4], TC of ΔV_{TH} can be ignored. Therefore, the TC of reference voltage and aspect ratios can be expressed as

$$\frac{\delta V_{REF}}{\delta T} = -\kappa + \frac{nK_B}{q} \ln\left\{\frac{6nq\kappa}{(n-1)K_B} \frac{K_3K_5}{K_4K_6K_7} K_R[\Delta V_{TH} + \ln\left(\frac{K_2}{K_1}\right)]\right\}, \tag{4.20}$$

$$\frac{K_3K_5}{K_4K_6K_7} K_R[\Delta V_{TH} + \ln\left(\frac{K_2}{K_1}\right)] = \frac{(n-1)K_B}{6nq\kappa} \exp\left(\frac{\kappa q}{nK_B}\right). \tag{4.21}$$

The effect of body bias is not significant to temperature compensation technique, because zero TC on reference voltage can still be achieved, but the resulting optimized aspect ratios are different from what is defined in (4.10), and it is harder to find aspect ratios from (4.21), since the magnitude of ΔV_{TH} is unclear. Therefore, instead of solving equation (4.21), we first find I_{CS} through the optimization method discussed previously,

such that the size of transistors, M_3 to M_7 can be approximated by using (4.6) with optimized I_{CS} to find the aspect ratios of transistors in bias voltage subcircuit.

The aspect ratios of transistors, M_3 to M_7, have to be properly determined to satisfy the design requirements. Due to the very small current passing through those transistors, the lengths of the transistors have to be long enough to keep the voltage level of V_{REF} to V_{TH0}. At higher temperature, the dc voltage across transistor M_3 to M_7 increases slower than it at room temperature, since the transistors have higher current throughput. Thus, if the channel length is not long enough, the minimum operation voltage will increase to an unaccepted level at higher temperature. Therefore, from the simulation of the circuit architecture with temperature as parameter, the minimum channel length for the device to have desired operation at 50°C is 20um.

4.2 Series Voltage Regulator

In this section, a series voltage regulator for RFID application is implemented and optimized according to the objectives. The LDO regulator topology is utilized to have low power and low voltage operation with good voltage regulating ability. Section 4.2.1 illustrates the circuit implementation of the regulator. Section 4.2.2 shows the optimization for improving the performance of the regulator.

4.2.1 Regulator Circuit Implementation

The schematic diagram of LDO is shown in Figure 18. It uses a differential amplifier, which consists of M_S, M_{D1}, M_{D2} and a pair of PMOS active current mirror, as OPA, a large PMOS transistors, M_{Pass}, as pass device, 4 diode-connected PMOS transistors M_{F1} to M_{F4}, as feedback network and a large capacitor, C_L, as storage device.

The operation principle is illustrated as following: the OPA compares the feedback signal from V_f with V_{REF}, and then it produces an error signal to control the current flowing through M_{Pass} to produce a constant V_{REG}. For example, if any small variation occurs as at V_{REG}, feedback network would generate a small feedback voltage, v_f. Then the OPA adjusts the error signal according to the v_f to control the magnitude of the current flow of M_{Pass} to compensate the variation of V_{REG}.

In order to save power and area, all of the transistors operate in the subthreshold region. From (4.1), higher voltage gain for amplifier can be expected, because the subthreshold current depends exponentially on gate-source voltage.

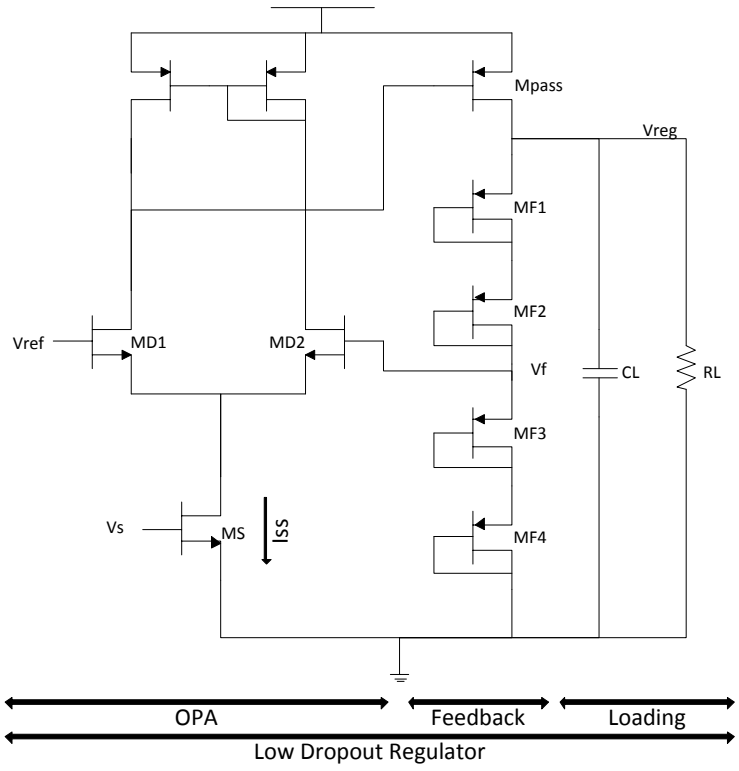

Figure 18. Series Voltage Regulator Circuit Structure

A single stage differential amplifier is adopted as the OPA for LDO to save power dissipation. The bandwidth is small for amplifiers designed using transistors in the

subthreshold region, so Figure 18 shows that only one pair of PMOS current mirror is used as active resistance instead of a cascade current mirror, because an active cascade current mirror can reduce the bandwidth of amplifier. Multiple amplification stages are not necessary, since the gain is high enough for transistors in the subthreshold region and the bandwidth of OPA reduces as number of amplification stage increases.

A PMOS transistor (M_{Pass}) is used as a pass device, because the dropout voltage is lower for PMOS transistors. A pass device needs to accept great amount of current in order to drive the rest of RFID circuits, so the channel length of the PMOS transistor is short and the channel width of is long.

The feedback network consists of four PMOS transistors, M_{F1} to M_{F4}. The advantages of using PMOS transistors as active resistances are illustrated in [10]. They reduce current passing through feedback network, reduce chip area compared with ordinary resistor and eliminate body effect. Also, the noise property and thermal disturbance are more predictable. As four transistors are put in series, all of them operate at the subthreshold region, since the voltages across each of them are lower than threshold voltage. Thus, the current through feedback generator can be minimized.

4.2.2 Regulator Optimization

Before optimizing the series voltage regulator circuit, we have to obtain the expressions for transconductance and output resistance of transistor operated in the subthreshold region. The transconductance can be expressed as [5]

$$g_m = \frac{I_D}{nV_T}, \tag{4.22}$$

where g_m is the general expression of transconductance. From the equation, the transconductance is proportional to I_D. The output resistance is given by

$$r_o = \frac{1}{\eta g_m} = \frac{nV_T}{\eta I_D}, \tag{4.23}$$

where r_o is the general expression for output resistance [5]. Output resistance is inversely proportional to both η and I_D, so small drain current can introduce large output resistance. Moreover, η reduces as channel length of a transistor increases; therefore, the output resistance is higher for transistors with longer channel length.

In order to have stable V_{REG}, we have to understand the property of line regulation, LIR. LIR caused by ΔV_{DD} is expressed as

$$\begin{aligned}
\frac{\Delta V_{REG}}{\Delta V_{DD}} &\cong \frac{P_1}{P_2 A_V F_B} \\
&\cong -\frac{\frac{g_{mPass} r_{oPass} R_L}{r_{oPass} + R_L}}{\frac{g_{mD}(r_{on}||r_{op}) g_{mPass}(r_{oPass}||R_L) R_{F3,4}}{R_{F3,4} + R_{F1,2}}} \\
&\cong \frac{1}{g_{mD}(r_{on}||r_{op})} \frac{R_{F3,4} + R_{F1,2}}{R_{F3,4}}.
\end{aligned} \tag{4.24}$$

where r_{oPass} and R_L are the output resistance of M_{Pass} and the load resistor, respectively, r_{on} and r_{op} are output resistance of NMOS and PMOS transistor, respectively, g_{mD} and g_{mPass} are transconductance of M_{D1} and M_{Pass}, respectively, and $R_{F1,2}$ and $R_{F3,4}$ are the equivalent resistance of feedback transistors, M_{F1} to M_{F4}, respectively. Since the ratio of the resistors, $R_{F1,2}$ and $R_{F3,4}$, is a fixed value depended on the relationship between reference voltage and regulated voltage, LIR caused by ΔV_{DD} strongly depends on the voltage gain, $g_{mD}(r_{on}||r_{op})$, of the differential amplifier, so the use of subthreshold

amplifier is good for this application, since it has high voltage gain at very low current. Furthermore, a longer channel length NMOS transistor is desired.

Besides ΔV_{DD}, the variation of reference voltage also has significant effect on LIR of regulated voltage. The LIR caused by ΔV_{REF} is approximated as

$$\frac{\Delta V_{REG}}{\Delta V_{REF}} \cong \frac{g_{mD}(r_{on}||r_{op})g_{mPass}(r_{oPass}||R_L)}{1+g_{mD}(r_{on}||r_{op})g_{mPass}(r_{oPass}||R_L)\frac{R_{F3,4}}{R_{F3,4}+R_{F1,2}}} \cong \frac{R_{F3,4}+R_{F1,2}}{R_{F3,4}}. \quad (4.25)$$

The LIR caused by ΔV_{REF} cannot be reduced anyway, since it only depends on the feedback factor. This result makes sense, since the reference voltage is used as the baseline for comparison, so reference voltage generator should provide very stable reference voltage, or otherwise, the stability of regulated voltage would be compromised

The stability of V_{REG} also strongly depends on the bias current, I_{SS}, of OPA. We can estimate the effect of biasing current by

$$\frac{\Delta V_{REG}}{\Delta I_{SS}} \cong -\frac{(\frac{r_{on}||r_{op}}{2})g_{mPass}(r_{oPass}||R_L)}{1+(\frac{r_{on}||r_{op}}{2})g_{mpass}(r_{oPass}||R_L)\frac{g_{mD}R_{F3,4}}{R_{F3,4}+R_{F1,2}}} \cong -\frac{1}{g_{mD}}\frac{R_{F3,4}+R_{F1,2}}{R_{F3,4}}, \quad (4.26)$$

If the current variation is too strong, its effect on regulated voltage would be significant. Since I_{CS} is extremely stable due to the cascade self-biased current, it is a great source of bias current for the differential amplifier.

The load regulation, LOR, is also an important parameter for performance evaluation, since it gives the information about how well regulators deal with the variation of load current. LOR of this regulator can be approximated as

$$\frac{\Delta V_{REG}}{\Delta I_L} \cong \frac{R_{o,Pass}}{1 + A_V P_2 F_B}$$

$$= \frac{r_{o,Pass}}{1 + g_{mD}(r_{on}||r_{op}) g_{mpass}(r_{oPass}||R_L) \frac{R_{F3,4}}{R_{F3,4} + R_{F1,2}}}$$

$$\cong \frac{1}{g_{mD}(r_{on}||r_{op}) \eta_{pass} (g_{mpass})^2 (r_{oPass}||R_L) \frac{R_{F3,4}}{R_{F3,4} + R_{F1,2}}}. \quad (4.27)$$

where $r_{o,Pass}$ and η_{pass} are the output resistance and DIBL coefficient of M_{Pass}, respectively. In order to reduce the effect of ΔI_L, two ways can be employed. The first one is to increase η_{pass}. Since η_{pass} depends on the channel length of M_{Pass}, η_{pass} increases as the channel decreases. The second way is to increase $g_{mD}(r_{on}||r_{op})$, which is the voltage gain for OPA. The value of g_{mpass} is hard to predict, because it changes with loading current which is also the current passed through M_{Pass}. Thus, the channel length for M_{Pass} should be very short. From the simulation results, the optimum channel length of M_{Pass} is set to be 0.1um.

The width of the pass transistor is modified according to the maximum loading current. With high loading current, the gate-source voltage of the pass transistor has to operate within the range of output voltage of the differential amplifier. The width of M_{Pass} is chosen to be 30um, so the series voltage regulator would not drop regulation at higher load current.

Feedback network consists of 4 diode-connected PMOS transistors M_{F1} to M_{F4}. Since we want the current flowed through feedback network to be ignorable, the aspect ratios, K_{Fi}, should be small enough. Also, in order to have an even division ratio, all four aspect ratios are the same. Therefore, we choose the W/L to be $1um/10um$. The

resulting current passing though feedback circuit is less than 1nA which is ignorable compared to total quiescent current of 64nA. Table II gives the detail aspect ratios of transistors in both reference voltage generator and series voltage regulator.

Table II. Aspect Ratios of the Transistors

Transistor	Aspect Ratio (W/L)
M_1	0.2um/3um=(0.1um/3um)×2
M_2	0.3um/3um=(0.1um/3um)×3
M_3, M_5	88um/20um=(2um/20um)×44
M_4, M_6, M_7	4um/20um=(2um/20um)×2
M_R	1um/150um
M_{D1}, M_{D2}	0.5um/1um=(0.1um/1um)×5
M_S	1um/1um=(0.1um/1um)×10
M_{Pass}	30um/0.1um
$M_{F1} \sim M_{F4}$	1um/10um

CHAPTER V

SIMULATION RESULT AND ANALYSIS

The optimized circuits are simulated in 65nm technology in cadence environment with Spectre simulator. For DC simulation, the supply voltage starts from 1V to 3V. For AC simulation which is related to PSRR, the frequency starts from 1Hz to 1MHz. In order to find the effect of different temperature, all circuits are simulated in temperature range from -30°C to 50°C with 10°C as a step. The performance of each circuit is evaluated according to the simulation results and compared with previous works.

5.1 Simulation Result for Sub 1V Reference Voltage Generator

The simulation results of sub 1V reference voltage generator are presented based on the order of parameters from LIR, PSRR, and TC to quiescent current. These parameters indicate the performance of the reference voltage generator. The result will be presented in plots as well as average numbers.

Figure 19 shows the output voltage as a function of supply voltage at room temperature. The operation voltage ranges from 0.8V to 2.5V. Since the objective is from 1.1V to 2.5V, the reference voltage generator works well in this range at room temperature. The LIR is 0.90mV/V at room temperature. With the small LIR on reference voltage, the operation of regulator can be assured. Figure 20 gives the value of LIR at different temperature. The LIR generally increases with temperature. The worst case happens at 50°C. At this point, the LIR is 1.0mV/V, which is low enough for regulator to operate within the objective. Figure 21 shows the PSRR as the function of frequency at room temperature. The result indicates that, PSRR is -62dB at 100Hz and -50dB at 1MHz.

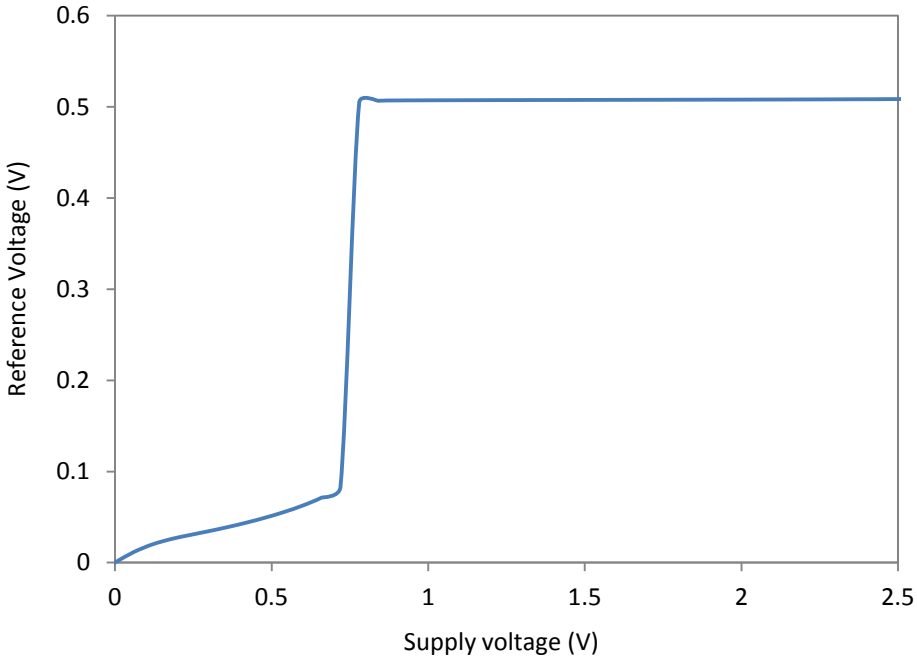

Figure 19. The simulation result of reference voltage as function supply voltage

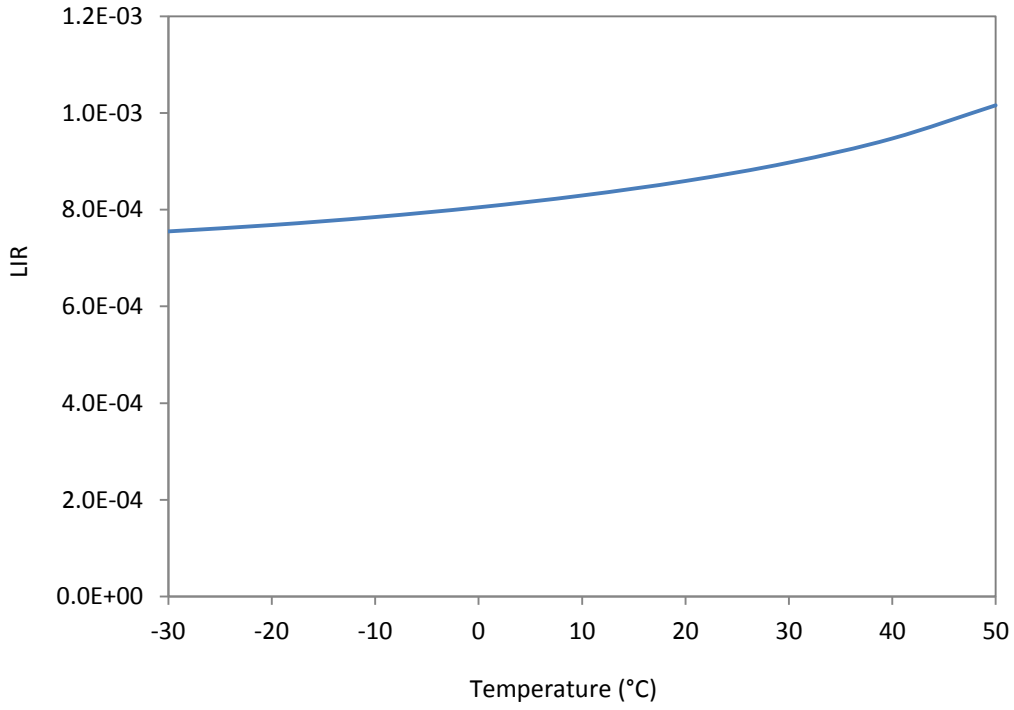

Figure 20. LIR as the function of temperature

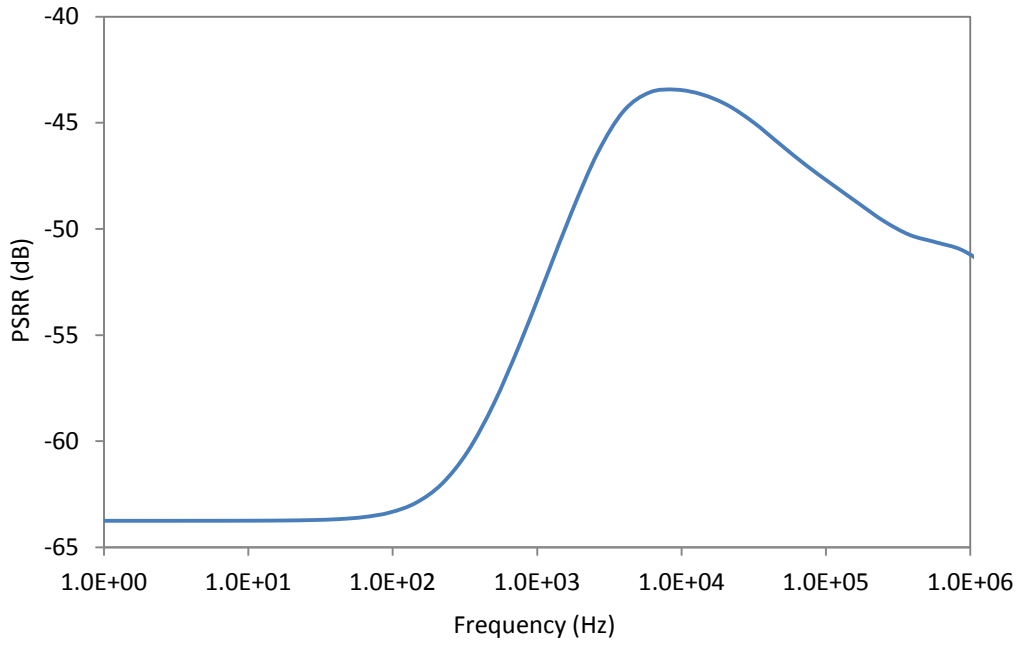

Figure 21. PSRR as function of frequency at room temperature

Reference voltages are expressed as function of temperature with different supply voltage in Figure 22. The reference voltage is 507.8mV at room temperature with supply voltage of 1.5V. The highest reference voltage is 508.7mV at 20°C with supply voltage of 2.5V. From the curves in Figure 22, the highest voltage point usually offers between 10°C and 20°C. From the highest point, we can obtain two sets of TCs; one set is positive TC, which means the voltage increase with temperature, occurred below the temperature at highest voltage. The other set is negative TC which occurs at the temperature above the highest voltage. When supply voltage is at 1.5V, the positive TC is 11.9ppm/°C, and the negative TC is -12.7ppm/°C. Both of them are very small value. Figure 23 shows the TC as function of supply voltage. Both positive TC and negative TC increase with temperature. It means that the temperature performance is worse for positive TC and better for negative TC, when temperature increases.

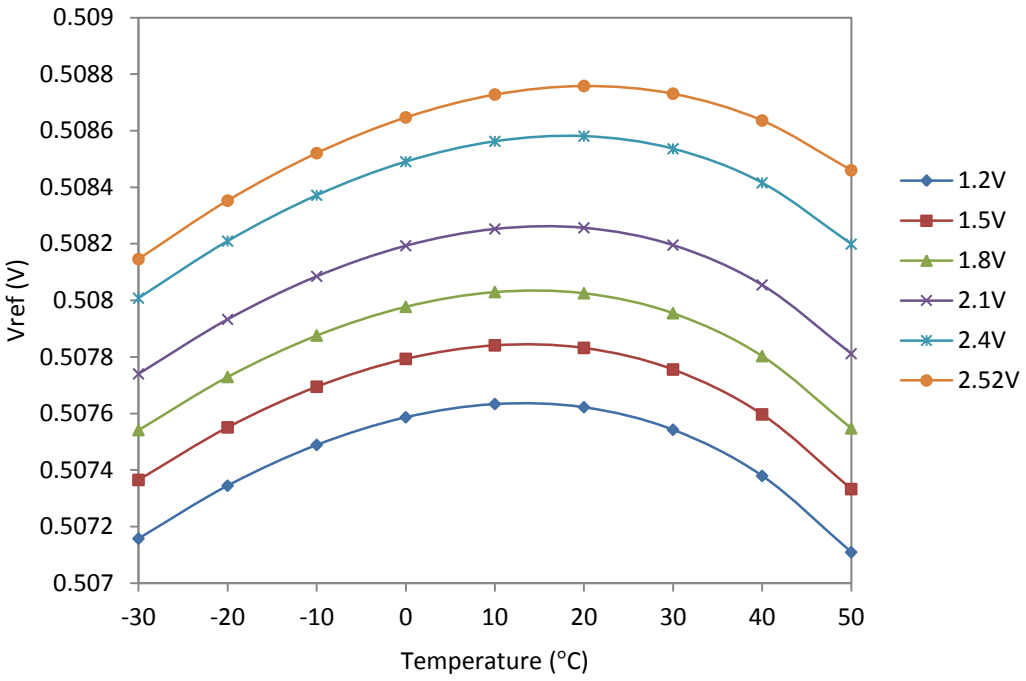

Figure 22. Reference voltage as function of temperature with supply as parameters

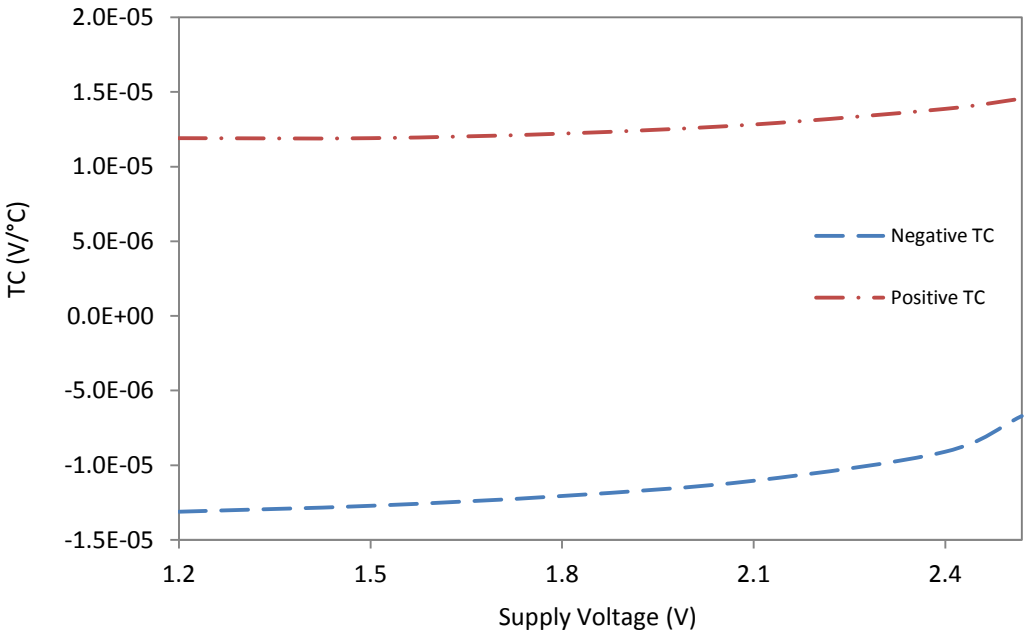

Figure 23. Temperature coefficient as function of supply voltage

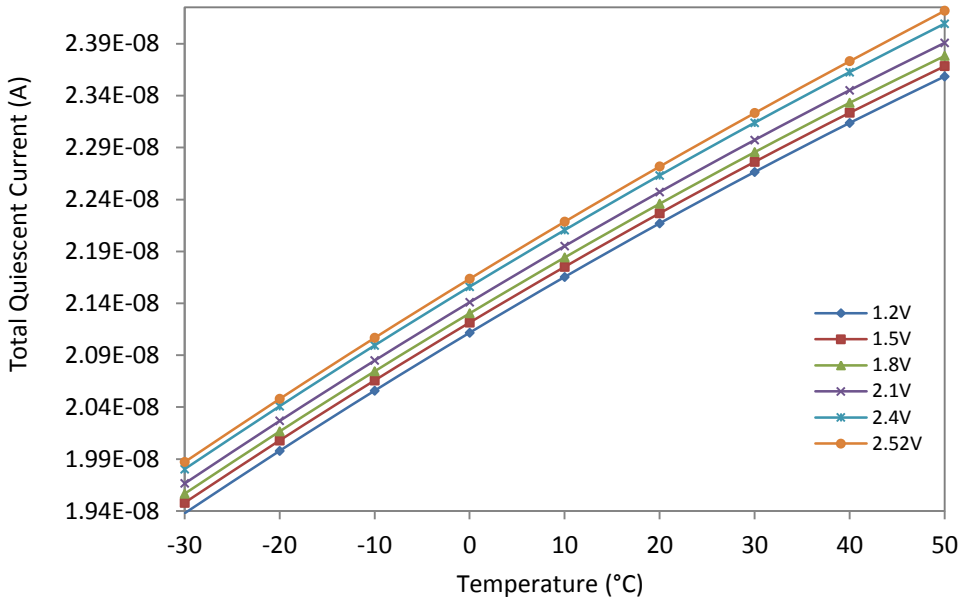

Figure 24. Quiescent current as function of temperature with supply voltage as parameter

Figure 24 explains the quiescent current as function of temperature with supply voltage as parameters. Quiescent current is almost proportional to temperature. The maximum quiescent current is 24.2nA at 50°C with supply voltage 2.5V and the minimum value is 19.4nA at -30°C with supply voltage 1.1V. These values are much smaller than the voltage reference proposed in [14] which is 214nA. The quiescent current through the voltage reference is low enough to be ignored by comparing with other circuits in the RFID system.

5.2 Simulation Result for Series Voltage Regulator

This section presents the simulation results for the voltage regulator with reference voltage generator. The results show the performance of the voltage regulator at varies environment. These are presented in order from LIR, LOR, and TC to quiescent current.

The DC change of regulated voltage at room temperature is shown as function of supply voltage in Figure 25. The operation range for the voltage regulator is from 1.1V to 2.5V where the level is stable at about 1.01V. The LIR for the regulator is 4mV/V at room temperature. Figure 26 illustrates the LIR as function of temperature and it gently increases with temperature. The highest LIR is 4.3mV/V at temperature 50°C. At the best case, the LIR is only 2.8mV/V. These values are considered to be great since the objective is to reduce the effect to less than 1% of voltage variation, and also, the value is small compared to other works. The curve of PSRR as function of different frequency at room temperature is shown in Figure 27. At 100Hz and 1MHz, the PSRR is -46dB and -62dB, respectively. The worst case occurs at around 10KHz; the value is -35.4dB which is a little worse than the desired value.

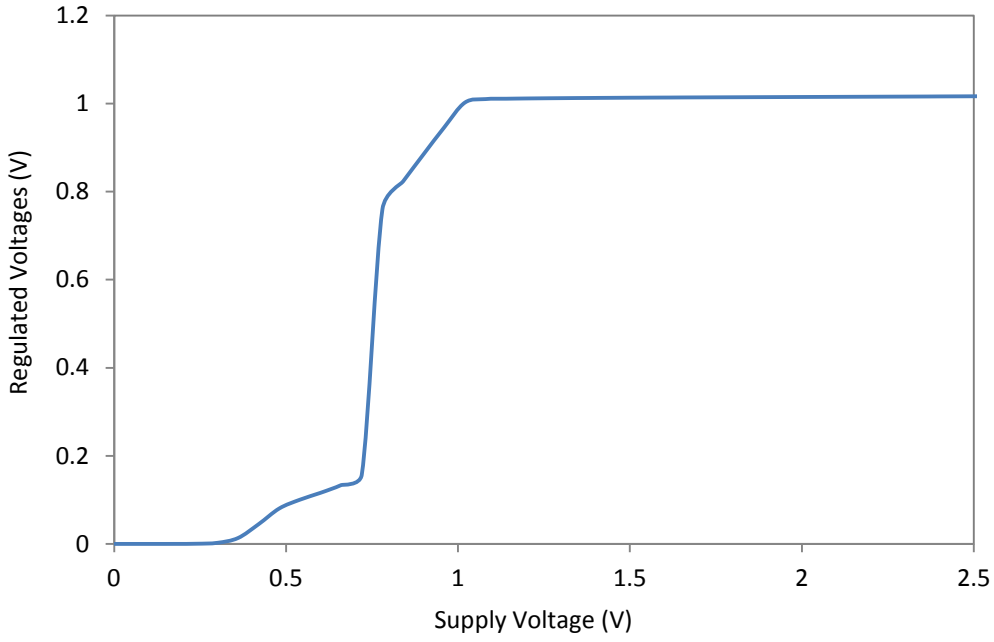

Figure 25. Regulated voltage as function of supply voltage

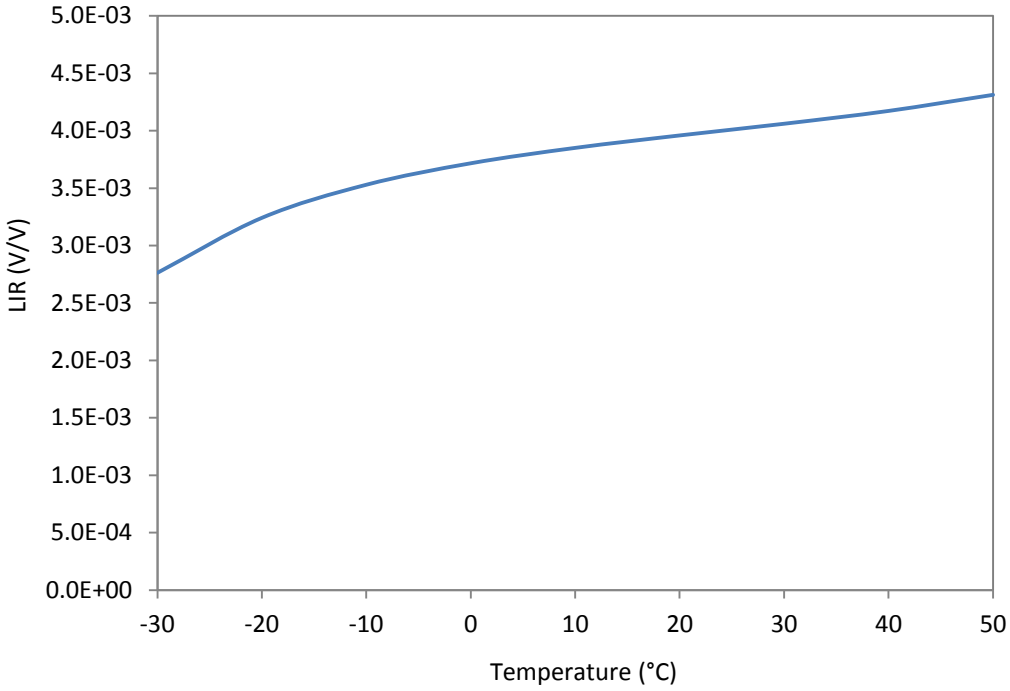

Figure 26. LIR value as function of temperature

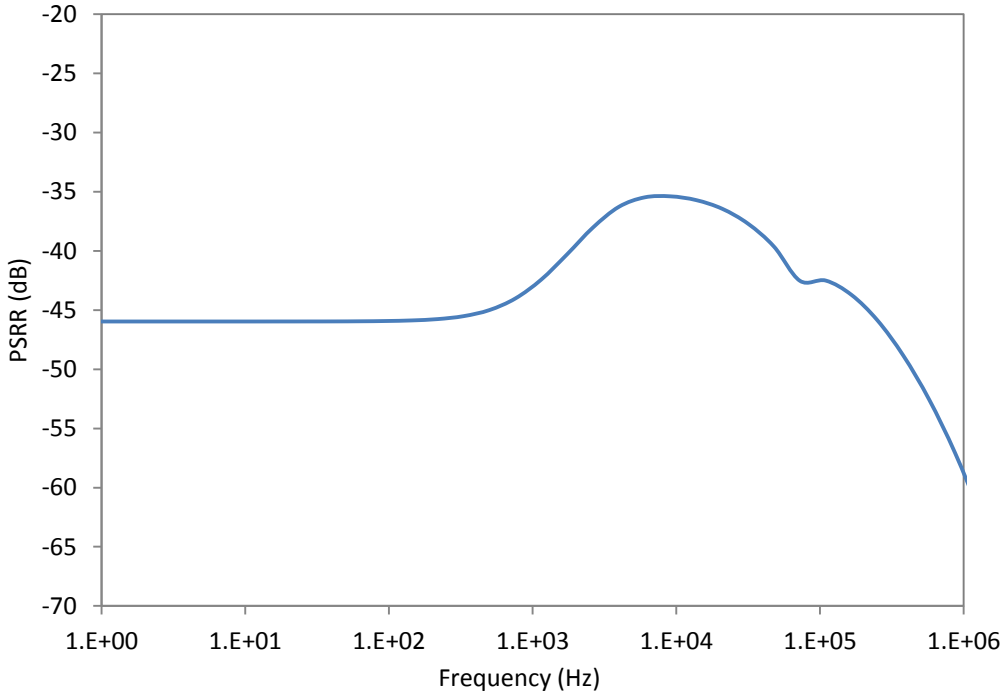

Figure 27. PSRR as function of frequency at room temperature

Figure 28 gives the regulated voltage as function of load current with different supply voltage. The curve looks like an exponential function, because the current depends on the voltage exponentially. Therefore, at load current above 10uA, only minor variation occurs in regulated voltage if load current varies. At room temperature with supply voltage 1.5V, the LOR is 6.57mV/50uA. This value is acceptable, since the voltage variation does not exceed 1% of the regulated voltage. LOR as a function of supply voltage at room temperature is shown Figure 29. LOR decreases when the temperature increases, because the pass transistor M_{PASS} has higher current throughput at higher temperature. The worst LOR is at the lowest supply voltage 1.1V, and the value is 9mV/50uA. The value still stays at the acceptable range.

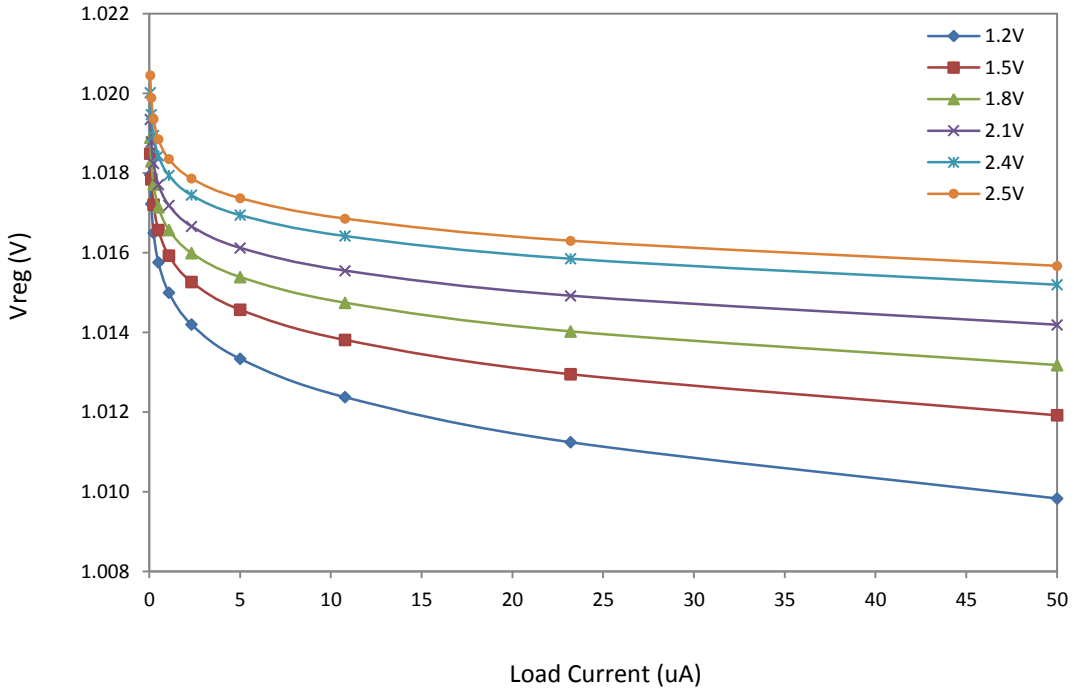

Figure 28. Regulated voltage as function of load current with supply voltage as parameter

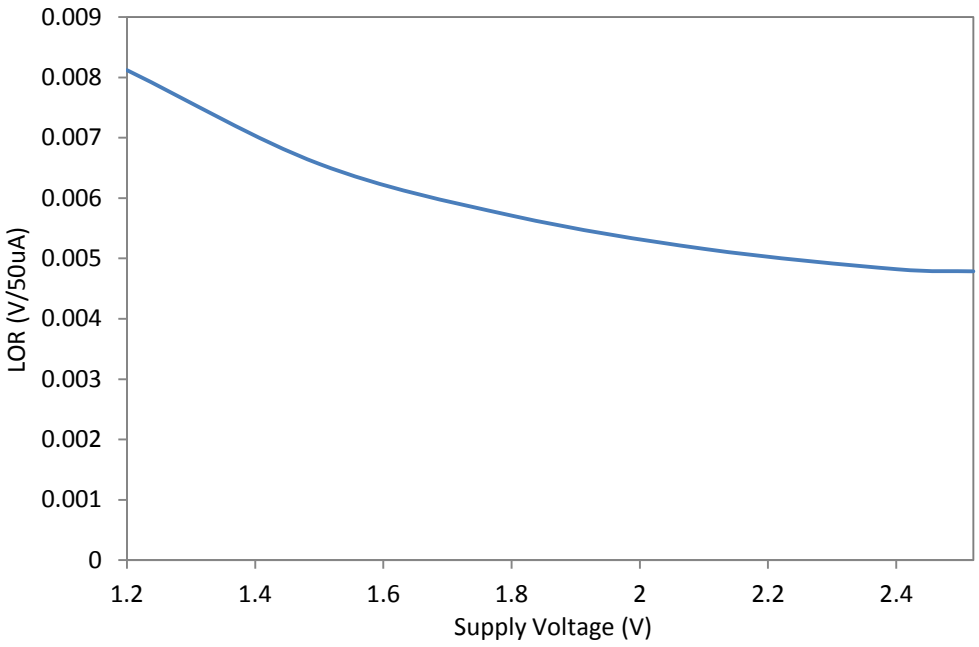

Figure 29. LOR as function of supply voltage at room temperature

Temperature coefficient is also an important parameter since the regulator is going to work at environment with varies temperature. Figure 30 gives the regulated voltage as function of temperature with different supply voltages. The circuit is simulated at maximum load current capacity. Similar to reference voltage generator, the highest voltage occurs at around 20°C. Above 20°C, the TC is negative, and below that point, the TC is positive. At supply voltage equaling to 1.5V, the values for positive TC and negative TC are 21.7ppm/°C and -31ppm/°C, respectively. The values are higher than they are in reference voltage generator, because of the effect of offset voltage of the differential amplifier. Figure 31 gives the variation of TC as function of supply voltage for both positive TC and negative TC. Both of them increase with temperature. On one hand, as the supply voltage gets higher especially at 2.5V, the positive TC becomes stronger; on the other hand, the negative TC becomes weaker as the supply voltage rises.

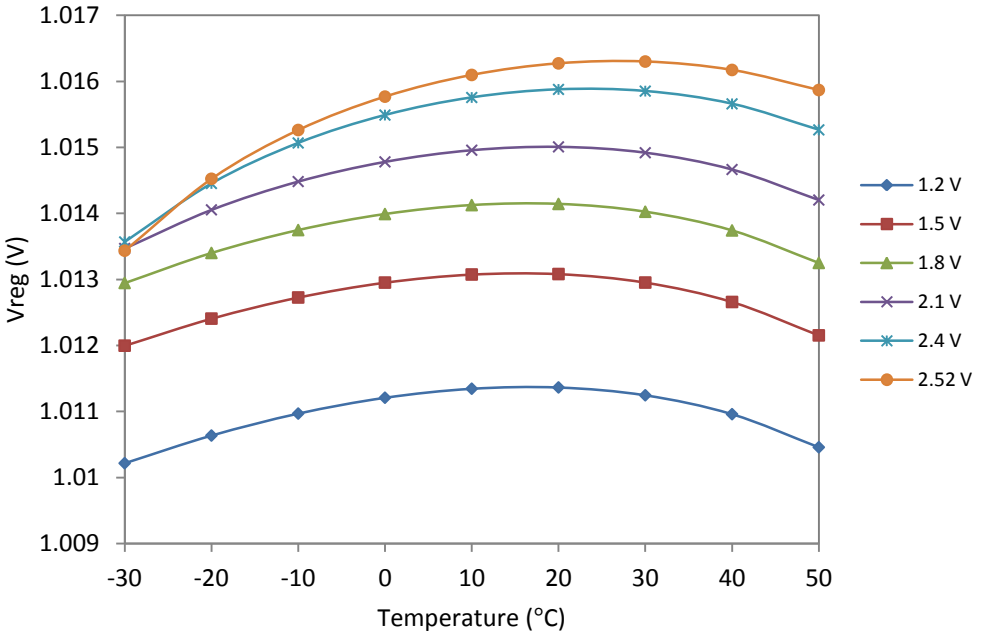

Figure 30. Regulated voltage as function of temperature with supply voltage as parameter

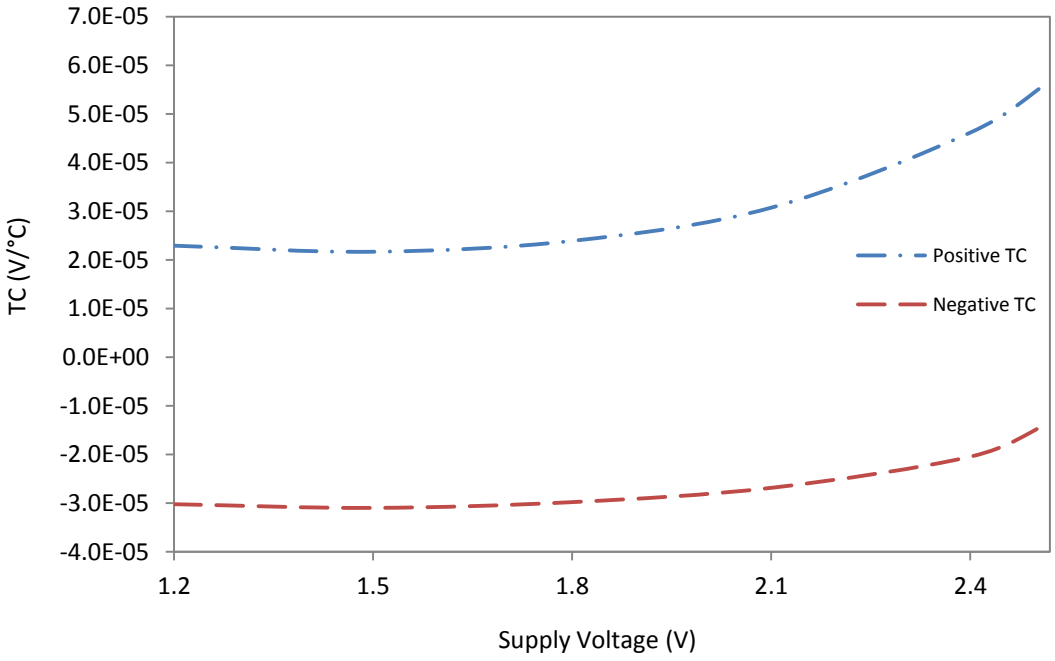

Figure 31. TC as function of supply voltage

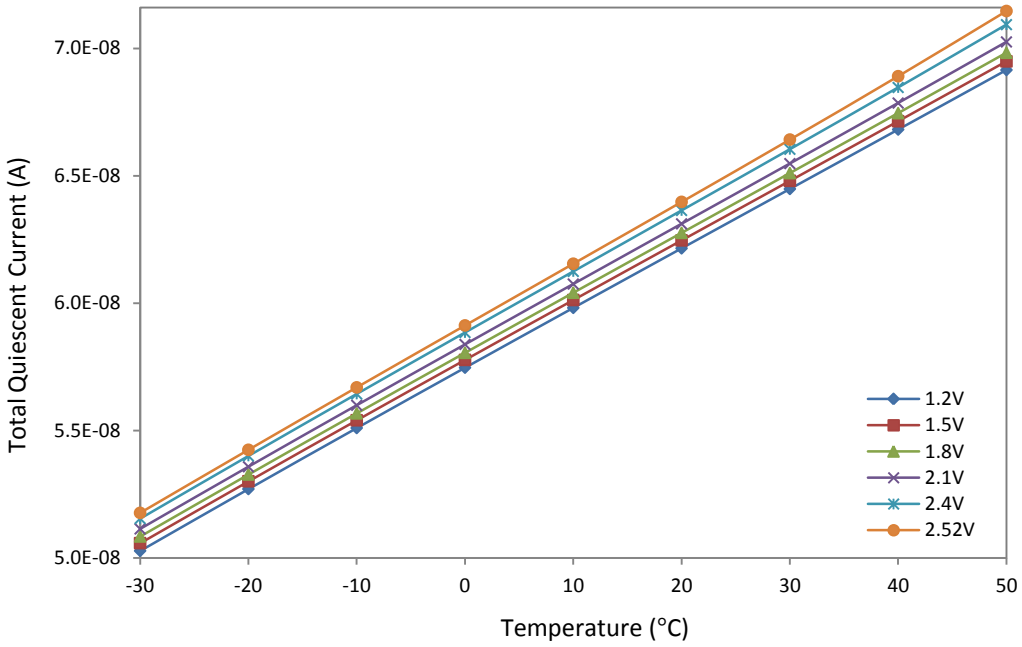

Figure 32. Total quiescent current as the function temperature with supply voltage as parameter

Figure 32 demonstrates measured total quiescent current as function of temperature, with different supply voltage. It increases proportionally with temperature. The total quiescent current reaches 66.4nA at room temperature and reaches the maximum 71.5nA at 50°C. The minimum current, 50.3nA occurs at -30°C with 1.1V supply voltage. The variation is about 0.24nA/°C. With 1.5V supply voltage at room temperature, the power dissipation is 97.2nW.

5.3 Analysis and Comparison

In this section, the results of simulation data are analyzed and compared with previous literatures. Section 5.3.1 gives analysis and comparison of the results from reference voltage generators. Section 5.3.2 shows analysis and comparison of the results from series voltage regulators.

5.3.1 Reference Voltage Generator

Table III gives the summarized performance data from the voltage reference generators of this work and previous literatures. Due to the technology constrain, the highest operational supply voltage is 2.5V. The minimum input put voltage is 0.8V; it is restrained by the circuit structure. As for RFID applications, this operation range is acceptable, but a voltage limiter has to put in place to prevent the circuit from quitting caused by excess voltage. The output reference voltage is restrained by the temperature compensation and the circuit property which is expressed in (4.11). The adjusting of reference voltage is a complicated work. Therefore, we would rather control the feedback network to adjust regulated voltage than change the reference voltage value. The line regulation is fairly small compared with previous literatures. The smallest LIR occurs in reference [15] because of its structural advantage. It uses an extra pair of differential amplifier to stabilize supply voltage ripple, but the disadvantage is the higher power dissipation. Besides, with this LIR value, the series voltage regulator can still achieve objectives.

The temperature operation range is defined according to the environment where RFID tag would be placed. The temperature range is 80℃ which is not the widest compared with previous literatures, but it can work well for most of RFID applications. Temperature coefficient for this work is fairly low. Although, some other reference generators have better TC, but the power consumption is higher or carries out worse LIR. The TC is acceptable by series voltage regulator.

The quiescent current is another important performance evaluation, since the value is proportional to the power dissipation of a reference generator. Since only 22.8nA

of current is consumed and the current is almost ignorable compared the consumption of other component in RFID circuit, the current is considered to be very low. One previous literature has quiescent current much lower than this work [15], because the structure of the circuit is very simple, but the disadvantage is that the circuit has less stable reference voltage output.

5.3.2 Series Voltage Regulator

The summery of characteristics of the proposed series voltage regulator along with previous literatures is shown in Table IV. These characteristics give a way to compare the performance of different voltage regulators. For instance, LIR of this is 4.06mV/V, which is less than 0.5% of the voltage variation. The previous literatures, [6] and [7], with similar application do not have the same capability. The input voltage range is fixed due to the technology constrain and the circuit structure. Since the maximum input voltage cannot excess 2.5V, a voltage limiter is required. The output regulated voltage level depends on RFID application, and it can be adjusted by changing the feedback factor of the feedback network.

The load capability is also an important factor since it provides the power for computational needs. 50uA of load capability is good enough for most of RFID application. The LOR gives the stability of the regulated voltage as function of load current variation. LOR in this work is 6.57mV/50uA at room temperature with supply voltage 1.5V. The value is acceptable since the variation is less than 1% of regulated voltage. By comparing with previous literatures, although the LOR is not outstanding in this work, it is within the objective.

Temperature ranges for the presented literatures cover the temperature around room temperature. The circuit in [6] works at higher temperature with wider range. Meanwhile, the circuit in [7] works only around room temperature. At the same time, the proposed regulator works with lower temperature within acceptable range. But the TC for this work is excellent since it is only 31ppm/°C which is the lowest compared with three previous literatures. Since reference [8] is specially designed for digital circuits operating in the subthreshold region, it does not include any design to compensate the temperature variation.

The quiescent current is compared in Table IV. In this work, the value is only 63.8nA. It is more than 10 times lower than the quiescent current in reference [6] which has similar feature with this work. Although the quiescent is twice higher than what is presented in reference [8], this work has more completed feature for TC and load capacity.

Table III. Comparison of Low Power Voltage Reference Generators

	This Work	[15]	[14]	[13]	[12]	[11]
Year	2012	2011	2009	2007	2006	2003
Technology	65nm	0.18um	0.35um	0.35um	0.18um	0.6um
Input Voltage (V)	0.8 - 2.5	0.45 - 2	1.4 - 3	0.9 - 4	0.85 - 2.5	1.4 - 3
Output Voltage (mV)	507.8	263.5	745	670	221	309.3
Line Regulation (mV/V)	0.9	4.4	0.02	2.7	9	0.8
Temperature Range	-30 - 50	0 - 125	-20 - 80	0 - 80	20 - 120	0 - 100
TC (ppm/°C)	12	142	7	10	271	36.9
Quiescent Current (nA)	22.8	7	214	40	3882	9700

Table IV. Comparison of Low Power Voltage Regulators

	This work	[6]	[7]	[8]
Year	2012	2010	2010	2006
Technology	65nm	0.18um	0.18um	0.35um
Input Voltage (V)	V_{REF}: 0.8-2.5 V_{REG}: 1.1-2.5	V_{REF}: 1-2 V_{REG}:1.6-2	N/A	V_{DDlow}: 0.63-5.6 V_{DDhigh}: 1.4-6.3
Output Voltage (V)	V_{REF}: 0.508 V_{REG}: 1.012	V_{REF}: 0.505 V_{REG}: 1.45	N/A V_{REG}: 1.5	V_{REF}: 0.605 V_{REG}: 0.605
Line Regulation (mV/V)	V_{REF}: 0.90 V_{REG}: 4.06	V_{REF}: 7.2 V_{REG}: 22	N/A V_{REG}: 12	V_{DDhigh}:0.8 V_{DDlow}: 0.18
Load Capability	50uA	50uA	N/A	5uA
Load Regulation	6.57 mV/50uA	20mV/50uA	0.34 mV/mA	0.5mV/5uA
Temperature Range(°C)	-30 - 50	-15 - 75	10 - 50	N/A
TC (ppm/°C)	V_{REF}: 12.7 V_{REG}: 31	V_{REF}: 9 V_{REG}: 43	N/A V_{REG}: 200	N/A V_{REG}: -2000
Quiescent Current (nA)	63.8	700	N/A	34

CHAPTER VI

CONCLUSIONS AND RECOMMENDATIONS

The objective of this thesis is to design and optimize an ultra low power and low voltage regulator for passive RFID tag. With such regulator, a passive tag can adopt more complicated functionality. The popularity of UHF RFID has shown that optimization techniques will be great interest in various applications from access control to sensor networks.

Passive tags operate in various environments with different and limited amount of input energy. A stable supply voltage that is insensitive to temperature changes and input power variations is needed for RFID front-end and digital circuits. The main challenge comes from the limited power available. The regulator must operate at sub-microwatts. This research work shows that it is possible to have stable regulated voltage under these conditions. The regulator is able to generate an output voltage that is insensitive to temperature variations and supply voltage ripples. Moreover, the reference voltage generator is optimized to have almost negligible amount of power consumption and can still perform the task as previously proposed. Since resistors and bipolar transistors take large area for implementation at sub-microwatts circuits, the regulator uses only MOSFET transistors.

One possible future work will be focused on compensation for process variations and trimming technique. Since the output voltage is based on threshold voltage and aspect ratios of transistors, any mismatch and change in transistor parameters can vary the voltage level of regulated voltage and compromise temperature compensation

technique. Therefore, the circuit needs trimming techniques such as programmable MOSFET transistor arrays or adjustment of the bulk voltage of the MOSFET. Moreover, protection circuitry is also worth to investigate, since it is related to the reliability issues and the usability of the device at harsh environment.

With the outstanding performances, this ultra low power and low voltage regulator will be useful for various applications using RFID technology.

APPENDICES

APPENDIX A

Small-Signal Analysis of Transistor Operating in the Subthreshold Region

The ac small signal equivalent circuit of the transistor operating in the subthreshold region is presented in this section [3], [5]. The equivalent circuit is important to predict the behavior of amplifiers and transistors operating in small signal mode. The v_{GS} and i_D can be expressed as sum dc and ac components shown as

$$v_{GS} = V_{GS} + v_{gs}, \tag{A.1}$$

$$i_D = I_D + i_d, \tag{A.2}$$

where v_{GS}, V_{GS}, and v_{gs} are the total gate-source voltage, the dc gate-source voltage and the ac small signal gate-source voltage, respectively; i_D, I_D, and i_d represent the total drain current, the dc drain current and the ac small signal drain current, respectively. From (A.1) and (2.2), i_D can be expressed as [5]

$$i_D = KI_0 \exp\left(\frac{V_{GS} + v_{gs} - V_{TH}}{nV_T}\right)$$

$$= KI_0 \exp\left(\frac{V_{GS} - V_{TH}}{nV_T}\right) \exp\left(\frac{v_{gs}}{nV_T}\right). \tag{A.3}$$

By expressing the term, $\exp\left(\frac{v_{gs}}{nV_T}\right)$, with a Taylor-Series expansion, the i_D can be obtained by [5]

$$i_D = KI_0 \exp\left(\frac{V_{GS} - V_{TH}}{nV_T}\right) \times$$

$$\left[1 + \frac{v_{gs}}{nV_T} + \left(\frac{v_{gs}}{nV_T}\right)^2 + \left(\frac{v_{gs}}{nV_T}\right)^3 + \cdots\right]. \tag{A.4}$$

Since the second order term and higher order terms in (A.4) are very small compared to the first order term, $\frac{v_{gs}}{nV_T}$, for v_{gs} less than one tenth of the nV_T, only the first order term needs to be considered. The i_D is expressed with first order term as [5]

$$\begin{aligned} i_D &= I_D + i_d \\ &= KI_0 \exp\left(\frac{V_{GS} - V_{TH}}{nV_T}\right)\left(1 + \frac{v_{gs}}{nV_T}\right) \\ &= I_D + \frac{I_D}{nV_T} v_{gs} = I_D + g_m v_{gs}, \end{aligned} \tag{A.5}$$

where g_m represents the transconductance of the transistor operating in subthreshold region and is shown as [5]

$$g_m = \frac{I_D}{nV_T}. \tag{A.6}$$

In order to have a better small signal model, the DIBL effect has to be considered. The subthreshold current with DIBL effect can be expressed as [3]

$$i_D = KI_0 \exp\left(\frac{v_{GS} - V_{TH}}{nV_T}\right) \exp\left(\frac{\eta v_{DS}}{nV_T}\right). \tag{A.7}$$

The small signal output resistance, r_o, is defined as [5]

$$\begin{aligned} r_o &= \left.\frac{\delta v_{DS}}{\delta i_D}\right|_{v_{GS}=\text{constant}} \\ &= \frac{1}{KI_0 \exp\left(\frac{V_{GS} - V_{TH}}{nV_T}\right)\frac{\eta}{nV_T} \exp\left(\frac{\eta v_{DS}}{nV_T}\right)} \\ &= \frac{nV_T}{\eta I_D} = \frac{1}{\eta g_m}. \end{aligned} \tag{A.8}$$

From (A.6) and (A.8), the intrinsic gain of a transistor operating in the subthreshold region can be obtained by [5]

$$g_m r_o = g_m \times \frac{1}{\eta g_m} = \frac{1}{\eta}. \qquad (A.9)$$

From the expression, the intrinsic gain depends on the DIBL coefficient only. In conclusion, (A.6) and (A.8) present the equation for transconductance and output resistance of the transistor operating in the subthreshold region, respectively.

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VITA AUCTORIS

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