A DLL Based Test Solution for 3D ICs

Vladimir Spartakovitch Mashkovtsev
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A DLL Based Test Solution for 3D ICs

By

Vladimir S. Mashkovtsev

A Thesis

Submitted to the Faculty of Graduate Studies through the Department of Electrical and Computer Engineering in Partial Fulfillment of the Requirements for the Degree of Master of Applied Science at the University of Windsor

Windsor, Ontario, Canada

2015

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A DLL Based Test Solution for 3D ICs

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DECLARATION OF ORIGINALITY

I. Co-Authorship Declaration

I hereby declare that this thesis incorporates the outcome of a joint research in collaboration with, and under the supervision of, Dr. Rashid Rashidzadeh, with the review and revision being provided by Dr. Rashid Rashidzadeh.

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ABSTRACT

Integrated circuits (ICs) are rapidly changing and vertical integration and packaging strategies have already become an important research topic. 2.5D and 3D IC integrations have obvious advantages over the conventional two dimensional IC implementations in performance, capacity, and power consumption. A passive Si interposer utilizing Through-Silicon via (TSV) technology is used for 2.5D IC integration. TSV is also the enabling technology for 3D IC integration. TSV manufacturing defects can affect the performance of stacked devices and reduce the yield. Manufacturing test methodologies for TSVs have to be developed to ensure fault-free devices.

This thesis presents two test methods for TSVs in 2.5D and 3D ICs utilizing Delay-Locked Loop (DLL) modules. In the test method developed for TSVs in 2.5D ICs, a DLL is used to determine the propagation delay for fault detection. TSV faults in 3D ICs are detected through observation of the control voltage of a DLL. The proposed test methods present a robust performance against Process, supply Voltage and Temperature (PVT) variations due to the inherent feedback of DLLs. 3D full-wave simulations are performed to extract circuit level models for TSVs and fragments of an interposer wires using HFSS simulation tools. The extracted TSV models are then used to perform circuit level simulations using ADS tools from Agilent. Simulation results indicate that the proposed test solution for TSVs can detect manufacturing defects affecting the TSV propagation delay.
DEDICATION

“If you Believe in yourself and have Dedication and Pride and Never Quit,
you’ll be a Winner. The Price of Victory is high but so are The Rewards”

BEAR BRYANT

To my Parents...
ACKNOWLEDGEMENTS

I would like to thank my committee members for their valuable comments and suggestions. A special thanks to Dr. Rashid Rashidzadeh and Dr. Esam Abdel-Raheem, my supervisors, for giving me this wonderful chance to join their research team and lead me during my research studies. Without their constant support and guidance, my research would not have been so successful and interesting. I would like to express my thanks and appreciations to Dr. Kemal Tepe and Dr. Ahmed Azab for accepting to server on my examination committee and for their time and technical expertise. Thank you Dr. Arash Ahmadi for his support and invaluable advices.
# TABLE OF CONTENTS

DECLARATION OF ORIGINALITY ................................................................. iii

ABSTRACT ....................................................................................................... v

DEDICATION .................................................................................................... vi

ACKNOWLEDGEMENTS ................................................................................. vii

LIST OF TABLES ............................................................................................. xi

LIST OF FIGURES ........................................................................................... xii

LIST OF ABBREVIATIONS/SYMBOLS ............................................................ xv

CHAPTER 1 INTRODUCTION .............................................................................. 1

1.1 Motivation and problem statement .............................................................. 1
1.2 Thesis Contributions .................................................................................. 4
1.3 Thesis Organization ................................................................................... 4

CHAPTER 2 2.5D & 3D ICs INTEGRATION ....................................................... 5

2.1 Evolution from Traditional PCB to 2.5D and 3D ICs Integration .................... 5
2.2 2.5 D Integration with passive Si Interposer structure .................................. 7
  2.2.1 Common Types of Defects of IW .......................................................... 9
2.3 3D ICs Integration stack by TSVs ............................................................... 9
  2.3.1 Common Types of Defects in TSVs during Fabrication Process ................. 10
2.4 Test Methodology for 2.5D and 3D ICs Integration ...................................... 12
  2.4.1 Existing testing methodology for passive SI interposer in 2.5D IC .............. 13
  2.4.2 Existing testing methodology for TSV in 3D integration .......................... 14
6.1 Simulations Results for DLL Based Time Amplifier for Testing 2.5D ICs Interposer

6.2 Simulations Results for 3D ICs TSV Using a Delay Lock Technique.

6.3 Summary

CHAPTER 7 SUMMARY AND CONCLUSIONS

REFERENCES/BIBLIOGRAPHY

VITA AUCTORIS
LIST OF TABLES

TABLE I  COMPARISON OF RLCG-PARAMETERS FOR FAULTY FREE TSVs  26
LIST OF FIGURES

1.1 Moor’s Law (a) Cost vs. time depiction from Moore’s notebook [49], (b) Moore’s Law, (source: Intel.com)................................................................. 2

2.1 2.5D & 3D IC Integration.............................................................................. 6

2.2 Typical 2.5 ICs integration........................................................................... 7

2.3 Redistribution layer in 2.5D ICs (a) Faulty (b) fault Free......................... 8

2.4 Fragment of interposer with defects: resistive open and bridge............. 9

2.5 3D ICs stack with TSVs.............................................................................. 10

2.6 (a) TSVs with micro void defect [47] (b) Faulty-free TSV; cross section view of a TSV with thin line process [5]................................................................. 11

2.7 TSV, types of defects: (a) Fault-free (b) Micro void (c) Pinholes........... 12

2.8 Thermal imaging and clustering algorithm [24]........................................... 13

2.9 The architecture for a TSV pair (a) [11] (b) [12]........................................ 15

3.1 A segment of an interposer with two interconnects implemented in HFSS environment......................................................................................... 19

3.2 Low bandwidth fault free equivalent model of IW extracted from 3D Full wave simulation................................................................................. 20

3.3 Equivalent IW model with segmented line Parameters (R, L, C, G)
(a) Faulty Free (b) Resistive open (c) Bridge................................................. 22

3.4 S-parameters of fragment of Interposer in HFSS: (a) S11, (b) S21........... 23

3.5 Cylinder view of a TSV.............................................................................. 24

3.6 TSV equivalent model with segmented R, L, C, G line (a) Faulty Free
(b) Micro void (c) Pinhole.............................................................................. 27

3.7 (a) Transmission line π Model of TSV (b) Equivalent faulty free
TSV model with parameters........................................................................... 28

4.1 Delay Lock Loop (block schematic)......................................................... 30
4.2 Designed schematic of DLL in locked condition

4.3 Vcontrol in locked condition in designed DLL schematic

4.4. Schematic of DFF, PFD and performance [44]

4.5 PFD at gate level

4.6 PFD signals from simulation

4.7 AND Gate in transistor level

4.8 NOR Gate in transistor level

4.9 Charge pump schematic with DC operating points when NMOS switch is on (a); curve that shows current charges the capacitor (b)

4.10 Charge pump schematic with DC operating points when PMOS switch is on (a); curve that shows current charges the capacitor (b)

4.11 Delay element unit cell

5.1 (a) Conventional DLL; (b) DLL with Vernier delay line to capture short time intervals

5.2 Test setup for interposer utilizing a DLL based time amplifier

5.3 DLL based time amplifier used to test interposer

5.4 Simulation results with time amplifier with Gain=3

5.5 DLL based time amplifier used to test interposer

5.6 ADS simulation delay example of proposed schematic

5.7 Block diagram of the proposed TSV tester utilizing two DLLs as a differential pair

5.8 Example of simulation with two DLL blocks

5.9 Simulation results with two parallel VCD lines

5.10 Linear model with two blocks of DLL

5.11 Block diagram of the proposed TSV tester utilizing N blocks of DLLs

5.12 Example of simulation with three blocks of DLL: Vcnt1-no TSV;
Vcnt2-micro void defect; Vcnt3-pinholes defect
5.13 Linear model with N blocks of DLL in test structure
5.14 DLL1 configuration for post-bond TSV tests
6.1 Test setup utilizing a DLL based time amplifier
6.2 (a) A segment of an interposer with two interconnects implemented in HFSS environment (b) Low bandwidth circuit model extracted from 3D Full wave simulation
6.3 Input and output signals of the time-amplifier when gain =10; (a) Applied input (b) Simulated output
6.4 Variations of the propagation delay with resistive open defects
6.5 Test setup for bridge fault detection
6.6 Variations of the propagation with the bridge resistance
6.7 Equivalent circuit TSV for simulations
6.8 Input signal. (b) Output signal (c) Vcont of DLL1 in the locked stat
6.9 Phase difference between the input and output of DLL1 in the locked state
6.10 Variations of ΔVcntl with number of TSVs connected to the tester
6.11 Variations of ΔVcntl with (a) Supply voltage (b) Process (c) Temperature
6.12 Simulations results with micro void defect (a) Vcont1 with no TSV (b) Vcont2 with tested TSV (c) ΔVcont
6.13 Simulations with Pinhole Defect by changing the Rp and CTSV separately (a) Vcont1 and Vcont2 with ΔRp (b) Vcont and Vcont2 with CTSV
6.14 Pinhole defect (a) ΔV with Rp (b) ΔV with CTSV
**LIST OF ABBREVIATIONS/SYMBOLS**

<table>
<thead>
<tr>
<th>Abbreviations/Symbols</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>IC</td>
<td>Integrates Circuit</td>
</tr>
<tr>
<td>IW</td>
<td>Interposer wire</td>
</tr>
<tr>
<td>TSV</td>
<td>Through-Silicon Via</td>
</tr>
<tr>
<td>DLL</td>
<td>Delay Lock Loop</td>
</tr>
<tr>
<td>PLL</td>
<td>Phase Lock Loop</td>
</tr>
<tr>
<td>HFSS</td>
<td>High Frequency Structural Simulator</td>
</tr>
<tr>
<td>ADS</td>
<td>Advanced Design System</td>
</tr>
<tr>
<td>CMOS</td>
<td>Complementary Metal-Oxide-Semiconductor</td>
</tr>
<tr>
<td>C4</td>
<td>Controlled collapse chip connection</td>
</tr>
<tr>
<td>PFD</td>
<td>Phase Frequency Detector</td>
</tr>
<tr>
<td>PD</td>
<td>Phase Detector</td>
</tr>
<tr>
<td>CP</td>
<td>Charge Pump</td>
</tr>
<tr>
<td>LPF</td>
<td>Low Pass Filter</td>
</tr>
<tr>
<td>VCDL</td>
<td>Voltage Control Delay Line</td>
</tr>
<tr>
<td>TA</td>
<td>Time Amplifier</td>
</tr>
<tr>
<td>IUT</td>
<td>Interconnect Under Test</td>
</tr>
<tr>
<td>$\rho_{Cu}$</td>
<td>Resistivity of material of IW</td>
</tr>
<tr>
<td>$l_{IW}$</td>
<td>Length of IW</td>
</tr>
<tr>
<td>$S_{IW}$</td>
<td>Cross sectional area of IW</td>
</tr>
<tr>
<td>$C_{IW}$</td>
<td>IW capacitance</td>
</tr>
<tr>
<td>$\varepsilon_{o}$</td>
<td>Vacuum permittivity</td>
</tr>
<tr>
<td>$\varepsilon_{r}$</td>
<td>Material permittivity</td>
</tr>
<tr>
<td>($d$)</td>
<td>Distance between wires</td>
</tr>
<tr>
<td>Symbol</td>
<td>Description</td>
</tr>
<tr>
<td>--------</td>
<td>-------------</td>
</tr>
<tr>
<td>( r )</td>
<td>Radius of wires</td>
</tr>
<tr>
<td>( C_{IW} )</td>
<td>TSV capacitance</td>
</tr>
<tr>
<td>( l_{IW} )</td>
<td>TSV length</td>
</tr>
<tr>
<td>( \varepsilon_{SiO_2} )</td>
<td>Permittivity of SiO2</td>
</tr>
<tr>
<td>( S_{TSV} )</td>
<td>TSV cross sectional area</td>
</tr>
<tr>
<td>( R1 )</td>
<td>TSV radius</td>
</tr>
<tr>
<td>( R2 )</td>
<td>TSV sheath radius</td>
</tr>
</tbody>
</table>
CHAPTER 1
INTRODUCTION

1.1 Motivation and problem statement

Since 1965, the "Moore's Law" predicted the quantitative trend of development of Integrated Circuits. Gordon Moore, Fairchild Semiconductor’s Director of R&D, a well-known scientist, wrote in his internal papers prediction and tendency representing the number of components for each integrated circuit with minimum cost by components [48]. He projected that the number of components per chip would be doubled every 12-24 months, Fig. 1.1(a) [49-51]. Nowadays, the dimensions of CMOS transistors in integrated circuits have reduced to 7nm. With such a significant size reduction, some manufacturing issues have emerged requiring advanced test methodologies for defect detection. The topic of testing integrated chips is becoming more important due to the high density of current ICs and the next generation of 2.5D and 3D integrated circuits, Fig. 1.1(b).

Through-silicon vias (TSV) and passive silicon (Si) interposer wires (IW) have become important components of 2.5D and 3D chip integration. Defects in the passive Si interposer and TSVs greatly decreases the yield and reliability, and they have to be captured at the early stages of device manufacturing. In this chapter, we will introduce the motivation for our research, and present the organization of the thesis. In fact, the TSVs is the enabling technology for Three-Dimensional Integrated Circuits (3D ICs), and through-silicon vias are primarily responsible for vertical interconnects for stacked dies. The initial idea for 3D integration was first time mentioned in 1964, and patented by Merlin Smith and Emanuel
Stern: “Method of Making Thru-Connections in Semiconductor Wafers”. The patent was filed on December 28, 1964 and granted on September 26, 1967 [1]. However, the

Figure 1.1 Moor’s Law

(a) Cost vs. time depiction form Moore’s notebook [49]

(b) Moore’s Law, (source: Intel.com)
technological capabilities to implement 3D ICs were not in place that times. After almost fifty years, we can build 3D stacked ICs using TSV technology. The main advantages of 3D ICs is the higher density for almost the same footprint which results in a more functionality and higher speed [6].

The equivalent circuit model of passive Si interposer wires (IW) and TSV with RLCG-parameters has explicit variations is affected by manufacturing defect. Variations of performance parameters of interposer wires and TSVs from their nominal values can be used as indicators to detect their faults. The common defects for TSV are micro voids and pinholes, and for passive Si interposers are resistive open and bridge.

In this thesis, we present two test methodologies using the concept of phase locking:

1. The first method involves the idea of using a time amplifier based on a Delay locked loop with a resolution of 1.5ps. In this approach, short-time intervals are first amplified and then measured. The propagation delay for signals passing through the device-under-test (DUT) used as indicator for determining and analyzing defects. Simulation are conducted with 65 nm CMOS technology using ADS software tool from Agilent.

2. In the second method, the values of Voltage Control Delay Line (VCDL) which controls the propagation delay in the DLL are used for fault detection. The control voltage across the delay cells in the locked state varies with TSV defects from its nominal value.
1.2 Thesis Contributions

The major contributions of this thesis include:

- New test solutions for TSVs utilizing delay-locked loops (DLLs) are presented
- The proposed test solutions present a robust performance against Process, supply Voltage and Temperature variations (PVT) due to the inherent feedback of DLL systems
- The proposed test methods allow to detect TSV’s common defects including pinholes and micro-voids. The test solution can also detect resistive open and bridge defects of passive Si interposers.
- The proposed methods have diagnostic components, which can be used to analyze the extent of defects.

1.3 Thesis Organization

This thesis includes 7 chapters. In Chapter 1, the research motivation and the contributions are covered. Chapter 2 presents the overview of 2.5D and 3D ICs integration, and reviews the previous related works. In Chapter 3 the equivalent circuit models are presented for (a) fragment of interposer wire (IW) and (b) a through-silicon via (TSV). Chapter 4 presents the design and description of the employed DLL circuit. In Chapter 5 the circuit implementation of the DLL used for 2.5Ds Interposer and 3D ICs TSV are presented. Chapter 6 covers the simulation results using 65 nm CMOS technology and finally, chapter 7 summarizes the results and presents conclusions.
CHAPTER 2
2.5D & 3D ICs INTEGRATION

2.1 Evolution from Traditional PCB to 2.5D and 3D ICs Integration

Continuous development of microelectronic technologies especially in the area of chips integration allows to fabricate high-speed and high-performance of ICs. An illustrative example is the evolution between traditional printed circuit board and three-dimensional integration (Fig. 2.1). The 2.5D and 3D integrations allows semiconductor manufacturers to create devices that surpass the traditional single die implementations. This relatively new integrations offer the advantages of performance, power consumption, capacity, and system size over the traditional printed circuit boards (PCBs).

Passive silicon interposer containing TSVs and redistribution layers is the key technology for 2.5D realization. It is should be noted that 2.5D IC integration with passive Si interposer can be considered as a part of continuous transition toward 3D IC integration model.

It has compelling advantages in terms of composite integration of numerous microelectronic devices (memories, logic chips, etc). As it can be seen in Fig. 2.1 the differences between the traditional PCB, 2.5D and 3D IC are considerable in terms of power consumption, size, latency, and I/O density [2]. A three-dimensional integrated circuit (3D IC) is implemented by stacking a number of silicon dies and connecting them vertically by TSVs.
In general, 3D ICs integration can be realized using different technologies:

- Monolithic 3D ICs;

- 2.5D and 3D interposer-based integration;

- 3D wafer-level packaging (3DWLP);

![Diagram of 2.5D & 3D IC Integration](source: [52])

**Figure 2.1 2.5D & 3D IC Integration**
• 3D stacked ICs (3D-SICs), etc.

2.2 2.5 D Integration with passive Si Interposer structure

A silicon interposer contains Through Silicon Vias (TSVs) and interconnects to connect multiple dies and components prior to connection to a substrate. This technology supports integration of various microelectronic devices such as memories, logic chips, and processors. A silicon interposer reduces the length of interconnects and contributes to lower power consumption, smaller size and higher I/O density [2]. Fig. 2.2 shows a typical 2.5D integration where multiple chips are connected through a redistribution layer and a number of TSVs [54].

Figure 2.2 Typical 2.5 ICs integration [54]
The silicon interposer is a passive device which provides horizontal interconnections between different chips and vertical interconnections between chips and substrate. The 2.5D IC in Fig. 2.2 shows how multiple chips are interconnected horizontally, next to each other, on an interposer containing the redistribution layer which is also responsible for horizontal communication. In order to connect dies to the interposer, micro-bumps are used and interconnections link the dies together. The connections between the interposer and substrate are realized using TSVs and C4 (Cu buttress) bumps. Due to the fact that the interposer is ultimately responsible for horizontal and vertical connections, as shown in

![Figure 2.3 Redistribution layer in 2.5D ICs](image)

**Figure 2.3 Redistribution layer in 2.5D ICs**

(a) Faulty  (b) Faulty Free

Fig. 2.3, the quality of the interposer is extremely important. The defect in the interposer can affect the operation of one or more dies, which increases the risk of releasing defective products even if faulty-free dies are used for the stacked dies [54].
2.2.1 Common Types of Defects of IW

Physical defects of an interposer can significantly affect the performance parameters of 2.5D ICs. Fig. 2.4 shows two common types of defects of (a) resistive open faults and (b) bridge faults.

![Figure 2.4 Fragment of interposer with defects: resistive open and bridge.](image)

2.3 3D ICs Integration stack by TSVs

Typical 3D IC integration which presents significant advantages over conventional IC implementation [6] is shown in Fig. 2.5.

TSVs testing can be performed at two different stages of (a) pre-bond and (b) post-bond [7]-[9]. Pre-bond testing enables to determine defects which originate during the fabrication of TSVs, e.g. voids, whereas post-bond testing can determine the defects introduced by bonding or alignment.
2.3.1 Common Types of Defects in TSVs during Fabrication Process

This thesis considers the parametric fault analysis with two of the following common types of TSV defects: micro voids and pinholes. Pinholes in the oxide layer between the body of TSV and substrate cause current leakage resulting in an undesirable conductive path between the TSV and the substrate. This type of deficiency is called a pinhole defect or leakage current fault [10]. A micro void defect (Fig. 2.6) begins from the formation of a cavity (void) inside of the TSV’s body. It is a malformation inside the TSV, due to imperfect manufacturing technologies, which can result in a resistive TSV.

A fragment of ICs including micro-void and pinholes is shown in Fig.2.7. The dimension
and position of the cavity or micro-void can vary and may strongly influence the TSV parameters. In most cases, the defect appears as illustrated in Fig. 2.7 (b).

Currently, there is a need for a unique test model which would allow to differentiate faulty TSVs, in order to ensure a high quality yield, while simultaneously maintaining the quality of 3D ICs integration. Many test methods have been proposed during the last five years e.g. [11]-[14] to cover TSV manufacturing faults. In these proposed methods, the concept

![Micro-void defect](image1.png)

(a)

![Cross-section view of TSV](image2.png)

(b)

**Figure 2.6** (a) TSVs with micro void defect [47]

(b) Faulty-free TSV; cross section view of a TSV with thin line process [5]
of the oscillation based test has been successfully utilized. A ring oscillator was employed in order to measure the propagation delay of the TSVs in the frequency domain.

**Figure 2.7 TSV, types of defects: (a) Fault-free. (b) Micro void (c) Pinholes**

### 2.4 Test Methodology for 2.5D and 3D ICs Integration

Test for 2.5D and 3D ICs is becoming important in the semiconductor industry [54].

Test methodologies for 2.5D and 3D ICs integration based on standards such as IEEE 1149.1 have been developed in recent years. In this chapter we will present a brief analysis of these methods.
2.4.1 Existing testing methodology for passive SI interposer in 2.5D IC

It is essential to develop manufacturing tests for interposers to detect possible faults prior to the IC integration. Test methodologies for an interposer can cover pre-bond or post-bond defects [3], [4].

**Original thermal images:**

![Image](image1.png)

(a) Functional  
(b) Defective

**Processed images by algorithm:**

(c) Functional  
(d) Defective

![Image](image2.png)

(e) The thermal image of an interposer segment is captured each time.

Figure 2.8 Thermal imaging and clustering algorithm [24]
Various test methods have been developed in the literature to cover Interposer defects [15-17]. An oscillation based test technique for interposer is developed by researchers [18-20]. In this method a ring oscillator is used to determine the propagation delay of interconnects in the interposer. A path with an excessively high or low propagation delay is detected from deviations of oscillator’s frequency. A pulse-vanishing test technique has also been proposed in the literature [21-23]. In this method a pulse is applied to the interposer and the length of the pulse is observed to determine its variations to detect faults. To pinpoint parametric faults with pulse-vanishing method accurate time measurement circuits are needed. Jui-Hung Chien et al. have proposed contactless stacked-die testing in [24] for pre-bond interposers using thermal images of an interposer as shown in Fig. 2.8. In this method, interposer defects are identified by thermal imaging and using a clustering algorithm [54].

2.4.2 Existing testing methodology for TSV in 3D integration

Test-cost analysis and test-architecture optimization for 3D IC integration are presented in [28-31]. It is shown that a test approach with pre-bond testing reduces the overall costs. An architecture for pre-bond and post-bond testing and test-optimization is presented in [32], [33]. The next paragraphs contains a brief review of the reported methodologies for testing TSVs for 3D ICs.

There are many test solutions for 3D ICs utilizing ring oscillators (RO). Huang et al. in [11], Huang et al. in [12] have proposed a test method based on the concept of the RO to detect TSV faults from propagation delay across a TSV (Fig. 2.9). The proposed structure
contains two buffer chains and connects two TSVs. The delay time between the TSVs explicitly depends on the defect type. Ring oscillators are known as a structure schematic with high jitter and temperature variations. This can obstruct the detectability of TSV faults.

Figure 2.9 The architecture for a TSV pair (a) [11] (b) [12]
Cho and Liu [9] have proposed a solution that can detect the variations of signal propagation through the TSVs due to resistive shorts or weak open resistance. The presented method can be used for pre-bond tests to determine resistive shorts and characterize the effects of TSV resistance variation through oxide liners. Tsai et al. [10] have proposed a test for detection of pin-hole defects in TSVs by using circuits to measure TSVs resistance. This study presents analog circuits to measure leakage current from a single PMOS transistor to detect TSV pinhole. The proposed methods in [9] and [10] cannot simultaneously detect both micro-voids and pinholes as there is no diagnostic component.

Lin and Huang [35] have proposed a method for parametric fault of post-bond TSVs based on VOT (Variable Output Threshold) scheme. It is a unified in-situ characterization flow for resistive open and leakage current detection. In this is method basic digital control circuit are used to measure the period of a ring oscillator to detect catastrophic leakage faults.

Chen and Wu [36] have proposed two schemes for testing and monitoring TSVs prior to wafer bonding. The first one has a floating end and utilizes a charge-sharing technique. The secondary solution uses a voltage-dividing technique. This method relies on amplification and can be used for detection of micro-void and pinhole defects. This methods provides pass and fail results and lacks a diagnostic approach to pinpoint the fault. It is also limited capacity for detection of highly resistive TSVs.

R. Rashidazdeh in [34] has proposed coupling techniques for contactless TSV probing testing technology. The proposed methods are based on capacitive, inductive and radiative
coupling techniques. The proposed contactless solutions support high-density and the tight-pitch requirements for TSV probing. The proposed probing methods support test and measurement of TSV resistance and capacitance. Due to TSV structure and impact of direct physical probing, it is highly desired to use contactless TSV probes for testing 3D ICs.

Huang et al. in [37], and Deutch et al. in [38] have proposed an oscillation based test methodology for TSVs. In [37] TSV faults are detected from variations of oscillation frequency of ring-oscillator due to TSV defects. In [38] a method is proposed that can detect TSV faults affecting its propagation delay.

2.5 Summary

This chapter describes 2.5D and 3D IC integrations and also presents typical manufacturing defects of interposer wires and TSVs. Existing test methodologies for TSVs and interposers are also presented and their advantages and disadvantages are discussed.
CHAPTER 3
Interposer Wires, TSVs and Equivalent Models

3.1 Equivalent Electrical Models

For the purpose of fault coverage evaluations a model is needed. Faulty and fault-free TSVs as well as Interposer Wires (IW) are implemented using HFFS software tool and 3D full-wave simulations are performed to extract circuit models for the implemented structures.

3.1.1 Faulty Free and Faulty Circuit Modeling for IW

The length and width of interposer wires are not strictly defined and may vary depending on the design requirements. Their length can be considerable and consequently their parasitic resistance and capacitance can be large [26]. It should be noted that an interposer interconnect can also contain TSVs for vertical connections.

A circuit model for interconnects in an interposer can be developed using analytical methods [25]. These models are generally difficult to develop and require some assumptions to simplify the problem. For instance the effect of eddy current in the substrate and its effect on the equivalent circuit model cannot be easily determined through analytical models [54].

In this work CAD tools are utilized to extract a model for interposers. The length of interposer wires vary depending on the design requirements. It can be in the range of hundreds of micrometers and consequently the resistance and capacitance can be
considerable [20]. To extract the model, a fragment of an interposer with parameters specified in [26] was implemented using High Frequency Structural Simulator (HFSS) as shown in Fig. 3.1. The length of the implemented structure which includes two TSVs is about 1300µm. Three dimensional full wave simulations were performed in the HFSS environment to determine the electric and magnetic fields within the structure. Simulation results are then used to generate a Spice model by HFSS. The Spice model is used to conduct circuit simulations using Advanced Design System (ADS) environment. Fig. 3.2 shows the low-bandwidth circuit model generated by HFSS at 1.0GHz solution frequency [54].
The model includes small resistances between the ports which represent the resistance of copper used to implement the interconnect. At high frequencies the effective cross section of the interconnect decreases due to skin effect. As a result, the resistance between the ports will increase at high frequencies. In the circuit model, this effect is represented by inductors, $L_1$ and $L_2$. The capacitances in the circuit model, $C_1$ and $C_2$, represent the capacitances formed between the ports and the substrate.

![Figure 3.2 Low bandwidth faulty free equivalent model of IW extracted from 3D Full wave simulation [54].](image)

The two resistances of $R_4$ and $R_5$ in Fig. 3.2 are used to model the AC resistance between the ports and the substrate. To evaluate the fault coverage of the proposed test solution, two types of defects are considered (a) resistive open faults and (b) bridge faults. When the resistance of interconnect exceed certain level, it is considered a resistive open. In bridge fault, one interconnect is shorted to anther through a resistor. Bridge fault affects the parasitic capacitance of interconnects. In both cases, the values of $R_1$, $R_2$, $C_1$ and $C_2$ in the equivalent model vary significantly from their nominal values [54].
Interposer wires can also be modeled using transmission lines theory, Fig. 3.3. Analytical expression for resistance and capacitance of interposer fragment wire is given in (1) and (2):

The resistance of an interposer wire, $R_{IW}$, is given by:

$$R_{IW} = \frac{\rho Cu_{IW}}{S_{IW}}$$

Where $\rho$ – resistivity of material, $l$ – length and $S$ – cross sectional area of interposer wire.

The capacitance of an interposer wire, $C_{IW}$, is given by:

$$C_{IW} = \frac{2\pi \varepsilon_0 \varepsilon_r}{ln(\frac{d}{r})}$$

Where $\varepsilon_0$ is the vacuum permittivity, $\varepsilon_r$ is the permittivity of material, $d$ is the distance between wires and $r$ is the radius of wires.

The change in magnitude in the aforementioned parameters is dependent upon the defect. Two types of interposer defects are studied in this work (a) resistive open defects and (b) resistive coupling between interposer wires. In the case of a resistive open, the resistance of the interposer wire increases ($R_{IW}$), in severe cases the connection can be open completely.

In resistive coupling, the capacitance ($C_{IW}$) of interposer wire changes. In both cases, the following model parameters are affected: $R1$ and $R2$; $C1$ and $C$. 

21
The interposer structure was implemented as a two port device in HFSS environment. The structure was simulated and S-parameters were obtained [53]. The S-parameters are shown in Fig. 3.4.

The solution frequency was set to 1.00GHz and the frequency of stimulus was swept from 1.00MHz to 1.00GHz to extract S-parameters of the implemented interposer wire. The
variations of S11 parameter in Fig. 3.4(a), shows a slight loss at high frequencies. When the frequency is high, the AC resistance increases affecting the loss. The graph in Fig. 3.4(b) shows that the S21 parameter reduced by 0.3 dB at 1 GHz.

Figure 3.4 S-parameters of fragment of Interposer in HFSS: (a) S11, (b) S21.
3.1.3 Faulty Free and Faulty Circuit Modeling for TSV

The TSVs model is include passive RLCG components. In this model, an oxide capacitor is considered (Fig. 3.6). The oxide capacitor is due to the presence of a thin layer of insulator, silicon oxide, between the body of TSV and substrate. To improve this model, the effect of depletion capacitance has to be considered. This capacitance appears in series with the oxide capacitance. To predict the behavior of a transmission line over a wide range of frequency, a RLCG model can be used. Such a model is valid only over a narrow band of frequency for TSV. TSV model using transmission line theory containing RLCG components is shown in Fig. 3.5 and Fig. 3.6.

3.1.4 Mathematical Approach and Equivalent TSV Model

Equivalent models of TSV with R, L, C, G parameters have been proposed in a number of studies [35-36], [39-41]. Analytical expression of the TSV’s resistance, capacitance and
inductance is given by equations (3), (4) and (5). The Cylinder view of a TSV is shown in Fig. 3.5 [40]:

The resistance, \( R_{TSV} \), can be calculated from:

\[
R_{TSV} = \frac{\rho_{Cu} l_{TSV}}{s_{TSV}} = \frac{4\rho_{Cu} l_{TSV}}{\pi d_{TSV}^2}
\]  

(3)

Where \( \rho \) is the resistivity of material, \( l \) represents the length, and \( S \) is the cross sectional area of TSV.

The capacitance \( C_{TSV} \) is obtained from:

\[
C_{TSV} = \frac{2\pi l_{TSV} \varepsilon_{SiO2}}{\ln\left(\frac{R_1}{R_2}\right)}
\]  

(4)

Where \( \varepsilon \) is the permittivity of SiO2, \( R_2 \) represents the radius of TSV, and \( R_1 \) is the radius TSV covered with the dioxide (Fig. 3.5).

The partial self-inductance of a TSV can be obtained equation (5) [42]:

\[
L = 2l \left( \ln\left( \frac{2l}{d} \right) \left( 1 + \sqrt{1 + \left( \frac{d}{2l} \right)^2} \right) \right) - \left( \frac{\varepsilon}{\mu} + \frac{d}{2l} \right)
\]  

(5)
Where \( l \) and \( d \) are the length and diameter of TSV and \( \mu \) is equal to \( 4\pi \times 10^{-7} \, H/m \).

In general for transmission lines we have:

\[
LC = \mu \varepsilon_{SiO2} l_{TSV}^2, \quad \text{and thus} \quad (6)
\]

\[
L_{TSV} = \frac{\ln(R_1/R_2) \mu l_{TSV}}{2\pi} \quad (7)
\]

The electrical models of two TSVs with different defects are shown in Fig. 3.6. The microvoids affect the TSV resistance, \( R_{TSV} \), in the area where they located. It can be modeled as an additional resistance, shown as \( R_m \) (micro-void) as indicated in Fig. 3.6(b). Pinholes create a conductive region (leakage current) between the body of the TSV and the substrate. The life cycle of an IC is commonly reduced due to the leakage current. The parasitic capacitance of a TSV \( (C_{TSV}) \) is the parameter which mainly dominates its circuit model [43]. The value of \( C_{TSV} \) depends on the type of defect, size and the location of pinholes.

**TABLE I**

**COMPARISON OF RLCG-PARAMETERS FOR FAULT FREE TSVs.**

<table>
<thead>
<tr>
<th>RLCG parameters of TSV</th>
<th>R (mΩ)</th>
<th>L (pH)</th>
<th>C (fF)</th>
<th>G (nS)</th>
</tr>
</thead>
<tbody>
<tr>
<td>[40] 2010</td>
<td>44-119</td>
<td>13-34</td>
<td>35-69</td>
<td>n/m</td>
</tr>
<tr>
<td>[11] 2012</td>
<td>2</td>
<td>1</td>
<td>242</td>
<td>n/m</td>
</tr>
<tr>
<td>[41] 2012</td>
<td>100</td>
<td>n/m</td>
<td>59</td>
<td>n/m</td>
</tr>
</tbody>
</table>
Table I summarizes the results of papers published in the last few years. The results reported in [40] are obtained for a TSV with the following parameters: \(d=2-5\) (\(\mu\)m), \(l=20-50\) (\(\mu\)m), \(\text{tox}=50-120\) (nm). The results in [11] are for a TSV with \(d=30\) (\(\mu\)m), \(l=75\) (\(\mu\)m), \(\text{tox}=1\) (\(\mu\)m), which are obtained through calculation using the analytical models in [40].

If a TSV is closely examined, we can see that its structure is more similar to the gate of a CMOS transistor rather than a wire. A TSV passes through a silicon substrate, isolated

![Figure 3.6 TSV equivalent model with segmented R, L, C, G line](image)

(a) Faulty Free (b) Micro void (c) Pinhole

The reported results in [41] are for a TSV with \(R=100\) m\(\Omega\), \(C=59\) fF and obtained through simulations.

If a TSV is closely examined, we can see that its structure is more similar to the gate of a CMOS transistor rather than a wire. A TSV passes through a silicon substrate, isolated
from the substrate by a thin layer of dioxide. This resembles the gate of a CMOS transistor in cylindrical coordinate. As the voltage applied to a TSV rises, a depletion region is formed within the substrate which creates a depletion capacitance. In fact, the transient behavior of a TSV cannot be fully modeled by just passive RLCG components and

Figure 3.7 (a) Transmission line π Model of TSV
(b) Equivalent faulty free TSV model with parameters implemented in HFSS
dependent sources are needed to derive an electrical model for a TSV. The behavior of a TSV can be predicted by solving Poisson’s equation [36] in cylindrical coordinate. This is similar to the approach taken to model CMOS transistors. In a steady state where the voltage applied to a TSV is settled a passive model can be developed. At high frequencies TSV resistance increases due to the skin effect. Moreover, eddy current in the substrate affect the overall TSV performance. Thus the TSV model developed for low frequencies may not accurately predict its behavior at high frequencies. It is possible to develop a passive RLCG model for TSV at high frequencies. However, such a model is valid over a narrow band of frequency.

Fig. 3.7 shows the transmission line $\pi$-model for TSV which is valid over a narrow band of frequency (a) and equivalent faulty free TSV model implemented in HFSS (b).

3.2 Summary

In this chapter circuit models for interposer wires and TSVs are presented. Equivalent Spice models extracted with High Frequency Structural Simulator (HFSS) for interposer wire are presented. Passive models based on RLCG elements for faulty TSVs were also presented in this chapter.
CHAPTER 4
THE DLL BASED STRUCTURES AND DESIGN

4.1 Phase Locked Technique PLL vs DLL

Phase locking techniques are widely employed in many microelectronic systems. These techniques are the bases for operation of Phase-Locked Loops (PLLs) and Delay-Locked Loops (DLLs). DLLs and PLLS are similar systems with an important difference between them. In a DLL instead of a Voltage-Controlled Oscillator (VCO), a Voltage-Controlled Delay Line (VCDL) is used [44].

4.2 Delay Locked Loop

DLL is a negative feedback system which presents a good performance against PVT variations. DLLs in general have less stability issues and generate lower jitter as compared to PLLs [44].

![Figure 4.1 Block Diagram of a Delay Locked Loop](image)

Figure 4.1 Block Diagram of a Delay Locked Loop
A DLLs doesn’t include a VCO and thus it is not prone to jitter accumulation. Due to the advantages of DLL over PLL for the purpose of TSV and IW testing, in the proposed test methods in this work DLLs are used. The block of diagram of conventional DLL is shown in Fig. 4.1. It consists of Phase Detector (PD), Charge Pump (CP), Low Pass Filter (LPF), and Voltage-Controlled Delay-Line (VCDL) modules. The phase detector (PD) compares the input and output phases of signals Vout (Out.clk) and Vin (Ref.clk) and creates an error signal proportional to their phase difference. The charge pump (CP) controls current sources to increase or decrease the control voltage to capture the lock. The output signal, Out. Clk, and the input signal, Ref. clk, at the locked condition are shown in Fig 4.2 where there is no phase difference between the input and output signals.

**Figure 4.2 Designed schematic of DLL in locked condition**

It should be noted that in real conditions, the phase difference it is not equal to zero, but there is small difference between them due to non-ideal components.
The control voltage determines the delay of the cells in the VCDL. The delay variations between Ref.clk and Out.clk are reduced due to the DLL’s negative feedback loop. In the locked state, the signals are aligned in phase and have an identical frequency. Fig. 4.3 shows the variations of Vcont. It takes about 9µs to capture the lock.

![Diagram](image.png)

**Figure 4.3 Vcontrol in locked condition in designed DLL schematic**

The closed loop transfer function of the DLL is given by [44]:

\[
\frac{\phi_{out}}{\phi_{in}}(s)|_{\text{closed}} = \frac{\frac{I_p k_{VCDL}}{2\pi}}{R_p C_p C_2 s^2 + \left[ C_p + C_2 + \frac{I_p k_{VCDL} C_p}{2\pi} \right] s + \frac{I_p k_{VCDL}}{2\pi}} (R_p C_p s + 1)
\]

(8)

This equation shows the relationship between \(\Phi_{out}\) and \(\Phi_{in}\) follows the behavior of a second order system.
4.3 Design and Description of DLL Circuit Topology

In this section the circuit designs and the simulation results for separate blocks of DLL are presented. All circuit designs were implemented and simulated using ADS simulation tool with 65nm CMOS technology.

4.3.1 Phase-Frequency Detector. Gate Level Design

DLLs contrary to PLLs cannot be readily used to implement synthesizer to generate signals with different frequencies from a reference signal (Fig. 4.1). Another issue in designing of DLL is limitation of propagation delay of the cells used to form VCDL.

Figure 4.4. Schematic of DFF, PFD and performance [44]
Fig. 4.4 shows the implemented phase/frequency detector which include two edge-triggered, resettable D flip-flops and an AND gate. The flip-flops were implemented using one AND gate and eight NOR gates. The schematic diagram of the implemented flip-flop is shown in Fig. 4.4 (b). There are two cross-coupled RS latches to respond to the rising edges of CK (Latch 1), and Reset (Latch 2) [44]. The PFD at gate level and the simulation results indicating the input/output signals are shown on Fig. 4.5 & 4.6.

![Schematic diagram of the implemented flip-flop](image)

**Figure 4.5** PFD at gate level

The implementation of AND and NOR gates which were used in our design are shown in Fig. 4.7 and Fig 4.8 respectively:
Figure 4.6 PFD signals from simulation

Figure 4.7 AND Gate in transistor level
4.3.2 The Charge Pump (CP). Design of the current sources of charge pump

The charge pump (CP) includes two sources which are switched during work cycle based on UP and DOWN signals. The low-pass filter (LPF) filters out the high frequency component to generate a control voltage (Vcont) for VCDL [44].

The schematic diagram of the charge pump (CP) and DC operating points together with the transient response are shown in Fig. 4.9 and Fig. 4.10.

Below are some the design consideration for the implemented CP:
Figure 4.9 Charge pump schematic with DC operating points when NMOS switch is on (a); Curve that shows current charges the capacitor (b)
Figure 4.10 Charge pump schematic with DC operating points when PMOS switch is on (a); Curve that shows current charges the capacitor (b)
• Transistors’ lengths are chosen 1um to be able to have high output resistance which is desired for good current source.

• Simulations were conducted to plot $I_D$ vs. $V_{GS}$ for both PMOS and NMOS by sweeping $V_{GS}$.

• $I_D/g_m = 10$ was chosen for the design and $V_{GS}$ and $I_D$ were selected accordingly. This will ensure that transistors work in linear region.

• Minimum length of 65nm were selected for switches to have minimum output resistance. The width of switches were calculated based on their current density and the associated $V_{gs}$ when the switches were ON.
4.3.3 The Voltage Controlled Delay Line. Delay Block.

The DLL acts as a negative feedback system, and adjusting phase difference between two signals (Ref. clk and Out. clk). The propagation delay of VCDL depends on the value of Vcont. The designed differential delay cell is shown in Fig. 4.11.

![Figure 4.11 Delay element unit cell](image_url)
4.4 Summary

In this chapter the detailed design of the implemented Delay locked Loop and simulation results of building blocks are covered. A DLL instead of a PLL is used to develop a test solution for TSVs and IW due to its superior jitter performance. Moreover, the feedback loop of a DLL has less setting issues as compared to PLL.
CHAPTER 5

DLL BASED TEST METHODOLOGIES

5.1 DLL Based Time Amplifier for Testing 2.5D ICs Interposer

In this chapter, will be proposed test solution based on Delay-Locked Loop (DLL) which is utilized to carry out manufacturing tests on interposers. The DLL circuit is utilized to determine the propagation delay variations of interconnects with a high resolution. The parametric faults affecting the propagation delay of interconnects are captured by the DLL based tester. The proposed test solutions presents a robust performance against process, supply voltage and temperature variations due to the inherent feedback of DLL systems [54].

5.1.1. DLL with Vernier delay line to capture short time intervals.

Physical defects of interconnects affect their propagation delay which can be observed to detect possible faults. To test interconnects in an interposer, test stimuli can be applied to their inputs to measure the propagation delay at the outputs. For short traces of wires in a typical interposer, the variations of the propagation delay from its nominal value can be too small to measure. To overcome this problem, a DLL is utilized in this work to act like a time amplifier to extend short-time- intervals linearly. Fig. 5.1 (a) shows the schematic diagram of a conventional DLL. It includes Phase and Frequency Detector (PFD), Charge Pump and Low Pass Filter (CP-LPF) and Voltage Controlled Delay Line (VCDL) blocks. To lock on the applied input, the system controls the VCDL propagation delay to minimize the phase difference between the input and output nodes. The time interval where the lock can be captured by the DLL is determined by the minimum and maximum VCDL
propagation delay. If the delay between the input and the reference signal falls below the minimum VCDL delay or exceeds its maximum delay, the DLL fails to lock. For the conventional DLL shown in Fig. 5.1(a) the minimum delay value for the DLL to lock is one delay cell. However, the propagation delay of interconnects in an interposer can be shorter than the propagation delay of one delay cell. To enable the DLL to lock on short time intervals, two delay cells as shown in Fig 5.1(b) is utilized. In this scheme, known as Vernier delay line [45-46], the minimum time interval is determined by the difference

![Diagram](a)

![Diagram](b)

**Figure 5.1** (a) Conventional DLL;  
(b) DLL with Vernier delay line to capture short time intervals [54]
between the propagation delays of the delay cells. Propagation delay of interconnects are commonly too small to accurately measure using on-chip circuits.

5.1.2 Test setup for interposer utilizing a DLL based time amplifier

In this test setup, short time intervals are first extended and then measured by a conventional time measurement circuit. This will relax the requirements for accurate short-time measurements. Fig. 5.2 and Fig. 5.3 shows the test setup for interposer wires utilizing a time amplifier.

Figure 5.2 Test setup for interposer utilizing a DLL based time amplifier [54]
The test stimulus is applied to an Interconnect Under Test (IUT). The stimulus is also applied to the time amplifier through a delay cell $D_1$. The IUT output is connected to the phase detector through a delay cell $D_2$. When the DLL acquires the lock, the signals, $S_1$ and $S_2$, at the phase detector input become in phase and therefore we can write:

$$t_o + T_{D1} = t_o + \Delta T + T_{D2}$$  \hspace{1cm} (9)$$

$$T_{D1} - T_{D2} = \Delta T$$  \hspace{1cm} (10)$$
Where $T_{D1}$ and $T_{D2}$ are the propagation delay of $D_1$ and $D_2$ in Fig. 5.3. This result indicate that the propagation delay of the IUT becomes equal to the delay difference between the propagation delay of $D_1$ and $D_2$ once the DLL gains the lock. In this case, the propagation delay, $\Delta T$, can readily be extended. Two arrays of delay cells are added to the circuit, the first array includes N-cells matched with $D_1$ and the second one contains N-cells matched with $D_2$. It is clear that the delay difference between the outputs, $Out_1$ and $Out_2$, becomes equal to (11) when the DLL is in the locked state.

$$N(T_{D1} - T_{D2}) = N\Delta T$$

(11)

![Time Amplifier](chart-area.png)

**Figure 5.4 Simulation results with time amplifier with Gain=3 [54]**
The proposed scheme supports high measurement resolution and dynamic range. As a result, the proposed test scheme can be used for parallel testing to carry out test on multiple interconnects simultaneously. In this case multiple interconnects are excited together with an input stimuli and the output is compared against the nominal output for multiple interconnects to detect possible faults.

To calibrate the circuit, a step signal is applied to both inputs of the time amplifier. In an ideal case the output is zero, however in practice the circuit may suffer from an offset error due to mismatch which can be deducted from the output. In the simulated schematic, 3 and 6 delay blocks were utilized and correspondingly, the time amplifier gains were 3 and 6. Fig. 5.4 demonstrates a case where for every 10 pS input delay, the output delay is increased by 30 pS, which results in a gain of 3 (Fig. 5.5).

Figure 5.5 DLL based time amplifier used to test interposer
On Fig. 5.6 shown one of number of the examples of simulations of proposed schematic.

![Figure 5.6 ADS simulation delay example of proposed schematic](image)

5.2 DLL Based Methodology for Pre-Bond TSV

TSV fault detection needs an accurate and high resolution measurement testing structure.

In this section the linear model of proposed test structure is covered.

5.2.1 Pre-Bond Test Structure

The test solution for pre-bond through-silicon vias are shown in Fig. 5.7. The voltage control delay line (VCDL) is used as an indicator for analyzing and determining TSV defects by comparing Vcnt1 and Vcnt2 signals as it shown on Fig. 5.8. The proposed solution consists of two DLL blocks used as a differential pair.
Figure 5.7 Block diagram of the proposed TSV tester utilizing two DLLs as a differential pair

Figure 5.8 Example of simulation with two DLL blocks
5.2.2 Linear Model

When the DLLs are in lock condition and there are no TSV connected to DLLs, the control voltages Vcnt1 and Vcnt2 are equal. After TSVs are connected to the delay line of DLL2 as shown on Fig. 5.7, the propagation delay in DLL2 increases and DLL2 loses the lock. However, the DLL2 will recapture the lock again due to the negative feedback. We can write the transfer function of the PD/CP/LPF (Fig. 5.9) [44] as:

\[
\frac{V_{cnt}}{\Delta \phi}(s) = \frac{I_p}{2\pi} \left( R_p + \frac{1}{C_p s} \right) \left| \left( \frac{1}{C_2 s} \right) \right| = \frac{I_p}{2\pi} \left( R_p C_p C_2 s + C_p + C_2 \right) s
\]

Thus the closed-loop transfer function is equal to:

\[
\frac{\phi_{out}}{\phi_{ref}}(s)|_{cl.} = \frac{I_p K_{VCDL}}{2\pi} \left( R_p C_p s + 1 \right) \left( R_p C_p C_2 s^2 + C_p + C_2 + I_p K_{VCDL} R_p C_p / 2\pi \right) s + I_p K_{VCDL} / (2\pi)
\]
It should be mentioned that the value of $R_p$ can be ignored because the loop contains only one pole at the origin [44]. The transfer function between the control voltage, $V_{cntl1}$, and the phase difference between the input and output signals, $\phi_{out} - \phi_{ref}$, for DLL1 in Fig. 5.10 is given by:

$$V_{cntl1} = \frac{K_{PD1}I_{p1}}{2\pi C_p s + K_{PD1}I_{p1}K_{VCDL1}} (\phi_{out1} - \phi_{ref})$$

(14)

Where $I_{p1}$, $K_{PD1}$ and $K_{VCDL1}$ represent the current supplied by the charge pump, the phase detector gain and the VCDL gain respectively. Assuming that the DLLs are matched, the difference between their control voltages is determined from (15):
\[ V_{cntl1} - V_{cntl2} = \frac{K_{PD1}I_{p1}}{2\pi C_p s + \frac{K_{PD1}I_{p1}K_{VCDL1}}{2\pi C_p}} (\phi_{out1} - \phi_{out2}) \] (15)

Where \( V_{cntl2} \) and \( \phi_{out2} \) are the control voltage and the phase difference of the second DLL respectively.

In the steady state where the DLLs are locked and no TSV is connected to the second DLL, \( \phi_{out1} = \phi_{out2} \) and the difference between the control voltages is zero. When a TSV is connected to the system, the phase difference between the input and output of DLL1, \( \phi_{out1} - \phi_{ref} \), increases due to the extra delay added by the TSV. As a result DLL1 loses the lock. To recapture the lock, the charge pump increases the injected current to raise the control voltage.

When DLL2 regains the lock, \( V_{cntl2} \) arrives at the final value which is proportional to the induced TSV delay. The difference between \( V_{cntl1} \) and \( V_{cntl2} \) settles at the final value as predicted by (15) at:

\[ V_{cntl1} - V_{cntl2} = \frac{\phi_{TSV}}{k_{VCDL1}} \] (16)
Where:

\[ \phi_{TSV} = \phi_{out1} - \phi_{out2} \]  

(17)

is the delay induced by the TSV.

Equation (16) shows a linear relationship between the delay induced by a TSV and

\[ \Delta V_{cntl} = V_{cntl1} - V_{cntl2} \]  

(18)

There is also possibility of increasing the number of the tested TSV by increasing the blocks of DLL till number of N (Fig. 5.11). An example of simulation with three DLL in test method also shown on Fig. 5.12. Accordingly, a linear model with N blocks DLL is represented on Fig. 5.13.
Figure 5.11 Block diagram of the proposed TSV tester utilizing \( N \) blocks of DLLs
Figure 5.12 Example of simulation with three blocks of DLL: Vcnt1-no TSV; Vcnt2-micro void defect; Vcnt3-pinhole defect

Figure 5.13 Linear model with N blocks of DLL in test structure
5.2.3 Post-Bond Test Structure

The proposed test method for pre-bond testing can be modified for post-bond TSV testing as it shown in Fig. 5.14. In this method the modules with TSVs are added to the feedback line of Vout. In this case the test structure need switches on the both sides of TSVs which can be implemented with multiplexers. The mathematical approach presented for post-bond TSV is also valid for post-bond TSVs.

Figure 5.14 DLL1 configuration for post-bond TSV tests
5.2.4 Calibration

For accurate measurement the circuit has to be calibrated to eliminate the effects of mismatch on the results. To calibrate the circuit prior to TSV testing, an external clock has to be applied to the DLLs. Once the DLLs are locked, the difference between their control voltages is measured. For an ideal case this difference is expected to be zero. In practice, a deviation from zero is expected which can be considered as an offset error and eliminated from the measurement results later.

5.3 Summary

In this chapter the principles of operation of the proposed test solutions were presented, and discussed. Linear models, schematic diagrams and calibration methods for pre-bond and post-bond testing were also presented.
6.1 Simulations Results for DLL Based Time Amplifier for Testing 2.5D ICs Interposer

The proposed test scheme in Fig. 6.1 was implemented using 65nm CMOS technology. The extracted circuit model for interposer in Fig. 6.2 was also used to conduct simulations with ADS simulation tool from Agilent. The DLL based time amplifier was designed to amplify short-time intervals as low as 1.5ps and the time amplifier gain was chosen to be 10 and the time-to-digital converter was designed to have time resolution of 15ps. Fig. 6.3 shows the input and output of the time amplifier at the locked state when the gain is set to be 10. It can be seen that the input time interval is extended by about ten times as expected.

Figure 6.1 Test setup utilizing a DLL based time amplifier [54]
Figure 6.2 (a) A segment of an interposer with two interconnects implemented in HFSS environment. (b) Low bandwidth circuit model extracted from 3D Full wave simulation
The implemented tester can detect interposer defects affecting the propagation delay by more than 1.5ps. To evaluate the fault coverage the main sources of faults including resistive-open and bridge faults were injected. Fig. 6.4 shows the case where the interconnect experiences the resistive open fault. When the resistance between the ports in the equivalent circuit exceeds 10Ω, the propagation delay rises from about 20ps to more than 200ps. As the resistance between the ports increases the propagation delay grows as expected. The considerable variations of the propagation delay from the nominal value for
a fault-free interposer can readily be detected by the tester. Fig. 6.5 shows the test setup for bridge fault detection in which two interconnect are connected through a resistor. Simulation results in Fig. 6.6 shows that the propagation delay of the interconnect-under-test increases as the bridge resistance decreases. This is an expected result since the

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**Figure 6.4** Variations of the propagation delay with resistive open defects [54]

**Figure 6.5** Test setup for bridge fault detection [54]
effective capacitance of the interconnect-under-test rises due the bridge fault. This will increase the overall propagation delay in return [54].

![Graph showing variations in propagation delay with bridge resistance](image)

**Figure 6.6. Variations of the propagation with the bridge resistance [54].**

### 6.2 Simulations Results for 3D ICs TSV Using a Delay Lock Technique.

The equivalent circuit model of TSV was simulated using ADS Agilent. Two common TSV defects of micro-voids (MV) and pinholes (PH) were considered. For the case of micro-voids, only Rm was changed and for pinholes two parameters of (a) Rp (pinhole) and (b) CTSV were changed. The inductance, L_{TSV}, can be neglected at low frequencies, under 3GHz [27]. As previously stated, a comparative analysis of two signals Vcnt1 and Vcnt2 was used. The Vcnt1 shows the value without connected TSV and Vcnt2 shows the value with connected TSVs. Fig. 6.7 indicate a fragment of one of examples connected implemented electrical model of TSV to VCDL.
Fig. 6.8 shows the input and output signals, $V_{\text{ref}}$ and $V_{\text{out1}}$. It can be seen that the input and output signals are aligned in the locked condition, but a close examination of rising edges represent that there is a difference of 32ps between signals (Fig. 6.9). This result can be explained by the fact the DLL has a feedback and minor error between the input and output signals is estimated. The value of delay differences between those signals may slightly vary during simulations when TSVs will be connected to VCDL.

**Figure 6.7 Equivalent circuit TSV for simulations**
It is clear that $V_{\text{cont}}$ of DLL2 will grow when the delay difference between $V_{\text{ref}}$ and $V_{\text{out}}$ rises. Figure 6.10 shows a linear relationship between $\Delta V_{\text{control}} (V_{\text{cont1}}-V_{\text{cont2}})$, and the number of connected TSVs to DLL2. It is shown that the $\Delta V_{\text{cont1}}$ increases linearly by 5.0 mV for each TSV which connected to DLL2. This relatively linear relationship makes it possible to carry out parallel tests in certain cases as shown in Fig. 5.7 and Fig. 5.11.

Figure 6.8 Input signal. (b) Output signal. (c) Control voltage of DLL1 in the locked state
To examine the robustness of the proposed test methodology against PVT variations, supply voltage, transistor lengths, transistor width, and temperature have been varied separately. When the supply voltage changes by ±5%, the $\Delta V_{cont}$ changes by less than 20µV. The small variations of $\Delta V_{cont}$ doesn’t affect the accuracy of the test results because the variations of $[V_{cont1}-V_{cont2}]$ for common faults is in the range millivolt which is about 1000 times lower. The value of $\Delta V_{cont}$ is more susceptible to process variations, and it changes by about 100µV when the width of transistors changes by 5%.

Figure 6.9 Phase difference between the input and output of DLL1 in the locked state

Figure 6.10 Variations of $\Delta V_{cntl}$ with number of TSVs connected to the tester
Figure 6.11 Variations of ΔVcntl with (a) Supply voltage
(b) Process (c) Temperature
Figure 6.12 Simulations results with micro void defect (a) $V_{\text{cont1}}$ with no TSV (b) $V_{\text{cont2}}$ with tested TSV (c) $\Delta V_{\text{cont}}$
Figures (6.12-16.14) present the simulation results. It shows that the faulty TSV can be detected by the proposed test solution. It is evident from the graphs that the linear and non-linear dependence of Vcont on CTCV, RTSV and GTSV (Rp), depends on the type and
magnitude of the defect. It can be seen from the graphs, the proposed test method can successfully determine the values of variable parameters R, C, and G (Rp) for faulty TSVs.

Figure 6.14 Pinhole defect

(a) ΔV with Rp (b) ΔV with CTSV
For graph with simulations results of micro-void defects (Fig. 6.12), a trade line was used. Fig. 6.12(a) shows the curve of Vcont1 (without TSV). The small size of voids doesn’t affect the electrical performance (RLCG parameters) of TSVs. The skin effect, which is also known as the addiction of alternating carries makes it possible for micro-voids to remain undetected.

For pinhole simulations two different cases were considered by changing the value of Rp and CTSV separately as it shown on Fig. 6.13(a, b). Figures 6.14 (a) and (b) also depict the differences in the two parallel VCDLs: resulting voltage ΔV. As it illustrated, the proposed test structure allows to not only determine if a TSV is faulty but also to determine the depth of the defect.

6.3 Summary

This chapter presented the results of simulations using ADS tool from Agilent for both proposed methodologies in testing 2.5D and 3D ICs integrations. The final graphs for common defects of passive Si IWs and TSVs were presented and analyzed.
A robust test solution for passive Si interposer wires and TSVs in 2.5D and 3D ICs is needed to ensure the success of these new technologies. Two test solutions for TSVs utilizing Delay Locked Loops are proposed in this work.

In the first method, which is presented for testing passive Si interposer in 2.5D ICs, a delay-locked loop is utilized as a time amplifier to first extend short time intervals and then measure them using a conventional Time-to-Digital Converter (TDC). This method relaxes the TDC design requirements for shot-time measurements considerably. CMOS 65nm technology was used to implement the test circuitry. Simulation results using ADS tools indicate that the implemented circuit supports 1.5ps measurement resolution and the time-amplifier can extend the time-intervals by 10 folds. A segment of a typical interposer was implemented and simulated using HFSS tools from Ansys. A circuit model for the implemented interposer was extracted from 3D simulations and the extracted model was used as a reference for the purpose of fault analysis. Simulation results show that the proposed method can successfully detect common structural defects resulting in resistive open and bridge faults.

In the second DLL based test method, which is developed for 3D IC TSVs, the control voltage of a DLL is observed for evaluation of the test results. Two delay-locked Loops are used as a differential pair to implement a differential pair to detect minor TSV structural defects. The proposed method presents a good performance against PVT variations due to the inherent negative feedback of DLLs and the employed differential configuration.
Simulation results using ADS tools from Agilent indicate that the supply voltage fluctuation of ±5% has a minor effect of less than ±0.34% on the output. The proposed test method can be used to detect both pre-bond and post-bond TSV faults.
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