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DESIGN OF MULTI-VALUED LOGIC CELLS USING SINGLE-ELECTRON DEVICES

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DESIGN OF MULTI-VALUED LOGIC CELLS USING SINGLE-ELECTRON DEVICES

By

Lin Li

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DESIGN OF MULTI-VALUED LOGIC CELLS USING SINGLE-ELECTRON DEVICES

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Author‘s Declaration of Originality/Previous Publication

I. Co-Authorship Declaration

I hereby declare that this thesis incorporates material that is result of joint research, as follows:

In all cases, the primary contributions, derivations, experimental setup, data analysis and interpretation were performed by the author through the supervision of Dr. C. Chen. In addition to supervision, Dr. C. Chen provided the author with the project idea, guidance, and financial support.

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This thesis includes 3 original papers that have been previously published/ submitted for publication in peer reviewed journals, as follows:

Thesis	Publication title/full citation	Publication status*

Chapter		
Chapter 3	L. Li and C. Chen, "An analytical model for NDC blocks with single-electron tunneling," in *Proceedings of the IEEE International Conference on Nanotechnology*, July 2015, pp. 448-451.	*"published"*
Chapter 4	L. Li and C. Chen," Modeling and Application for Negative-Differential-Conductance Devices with Single-Electron Technology"	*"Submitted"*
Chapter 5	L. Li and C. Chen, " An Area-Efficient Ternary Full Adder Using Hybrid SET-MOS Technology"	*"Submitted"*

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Abstract

This thesis proposes a new single-electron tunneling based NDC block and develops an analytical model which can be used for related circuit designs and/or their performance optimization. A piece-wise model is used to describe the I-V characteristics of the proposed NDC block. Four applications based on this NDC block are proposed: (1) Multiple-valued logic static memory cell (2) *Schmitt* trigger (3) Three-stage ring oscillator (4) ternary full adder using hybrid single-electron transistor and MOS technology. Simulation was done using Cadence Spectre simulator with 180nnm CMOS model and SET MIB macro mode to estimate the performance.

A Sincere Dedication

To my parents, supervisor and friends

Acknowledgements

I would like to express my gratitude to my supervisor Dr. Chunhong Chen for his useful comments, remarks and engagement through the learning process of this Master thesis. I have learned many thing since I became Dr. Chunhong Chen‘s student. He spends very much time instructing me how to write a paper, how to search literature and how to collect data. My thanks also go to Dr. E. Abdel-Raheem and Dr Y Wang for their constructive comments. Furthermore I would like to thank Ran Xiao for introducing me to the topic as well for the support on the way. Special thanks are given to Department of Electrical and Computer Engineering. Most of my theoretical foundations are built in here. Also, I like to thank the participants in my survey, who have willingly shared their precious time during the process of interviewing. I would like to thank my loved ones, including my parents and brother, who have supported me throughout entire process, both by keeping me harmonious and helping me put pieces together. I will be grateful forever for your love. Without their support, it would have been impossible for me to finish my Master degree.

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List of Abbreviations

CMOS – Complementary Metal Oxide Semiconductor

MOSFET – Metal Oxide Semiconductor Field Effect Transistor

MVL – Multiple-Valued Logic

NDC – Negative Differential Conductance

PVCR – Peak to Valley Current Ratio

CB- *Coulomb* blockade

RTD -- Resonant Tunneling Diode

SED – Single Electron Device

SET -- Single Electron Transistor

TAL- ternary adiabatic logic

TFA-ternary full adder

CNTFETs- carbon nanotube field effect transistors

Chapter 1

Introduction

1.1 Motivation and background

Complementary metal–oxide–semiconductor (CMOS) technology is predicted to confront significant technology limitations, which can slow the development of the integrate circuits, and the CMOS technology will reach to the crisis by the year 2020. Due to these limits, it is probable that CMOS will share its domination on the future integrated circuits (ICs) with the fundamentally new devices that use a few electrons, such as single electron transistors (SETs). In the past few decades, reducing power consumption used to be the primary task in chip designs to meet Moore's law. Figure.1.1 shows a plot of CPU transistor counts against dates of introduction. To deal with this issue, many ultralow-power devices have been explored. The power dissipation of single-electron transistors is ultralow; since it works with only one or a few electrons during switching operations. The drain current of SET is approximately three to four orders of magnitude lower than the traditional CMOS technology, which gets further reduction because of energy quantization effects. Hence, the practical implementation of SETs in modern very large scale integration (VLSI) technology necessitates hybrid CMOS-SET circuit logic. Therefore, we cannot use only single electron transistor with semiconductor technique as in PMOS and NMOS transistors in new technologies [1].

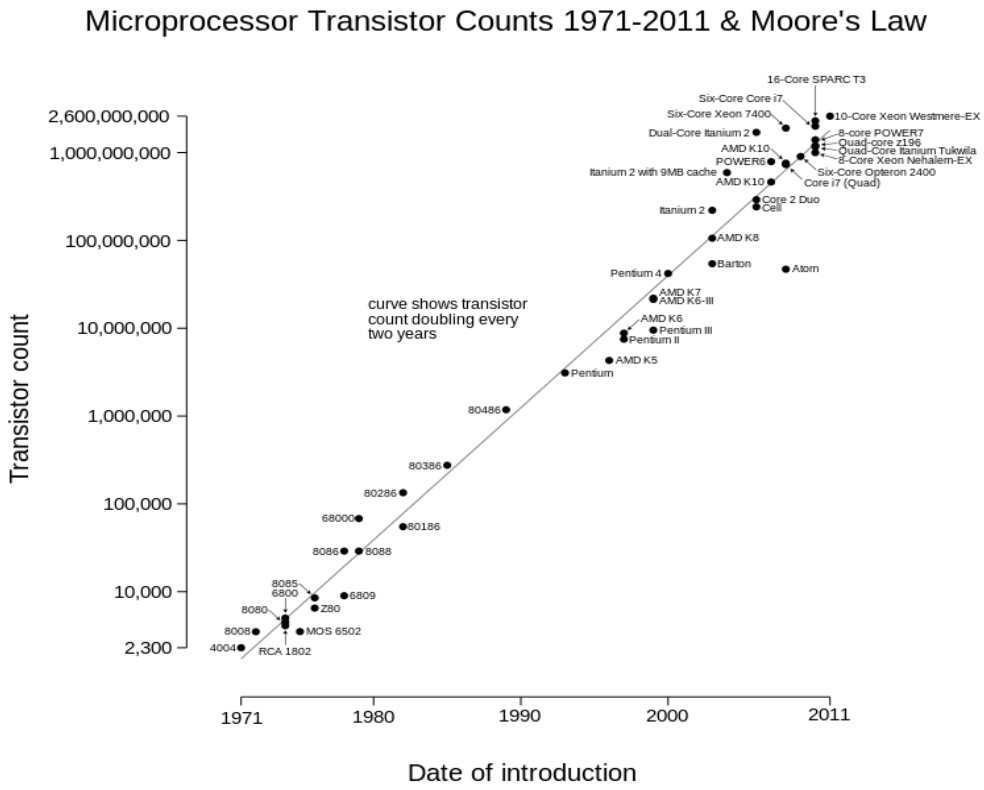


Fig 1.1 a plot of CPU transistor counts [17]

On the other hand, rapid progress in the fabrication technology of Silicon nano devices has pushed the device dimension toward 1-100nm length scale, which renders the basic working principles of the CMOS devices more dependent upon quantum effects and doping fluctuations. When device dimensions are scaled down to a few nanometers, quantum effects such as single electron tunneling and energy quantization lead to interesting new device characteristics that can be exploited to create extremely compact circuits. Figure 1.2 shows the shrinking feature size with every decade.

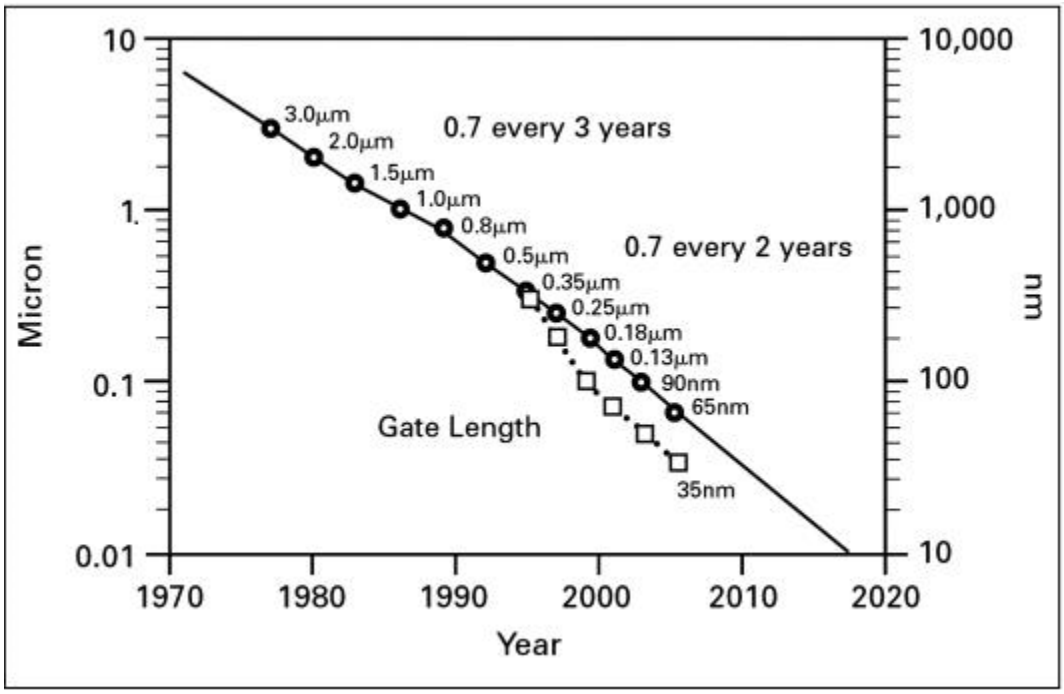


Fig 1.2 a plot of new technology generation introductions (1975–2005) [17]

The SET is one type of nanoscale electronic devices based on quantum tunneling and *coulomb* blockade effect, where one or more *coulomb* islands are sandwiched between two tunnel junctions which connect respectively with the drain electrode and the source electrode, and capacitive coupled with one or more gate electrodes.

Coulomb blockade of SETs is based on the controllable transfer of single electrons through small conducting, which called "islands". By taking advantage of the *Coulomb* blockade effect in controlling the transfer of individual electrons, the SET could lead to single-electron logic devices. Most single electron devices, such as Single-electron transistor models, are based on the orthodox theory of the single-electronics.

From the discussions of above, we can find that the SET has attracted attention as a candidate for future VLSI mainly due to these three reasons: nanoscale size, ultralow power dissipation, and unique *Coulomb* blockade oscillation characteristics. Although the

SET is a promising candidate device to substitute the CMOS, it also has its disadvantages, such as a poor driving capability, poor threshold control due to the involvement of only one or a few electrons in the switching process. Therefore, the conduction mechanism of the conventional CMOS-based logic is not applicable to SETs [1].

Negative differential conductance (NDC) block is a subcircuit that shows both positive and negative differential conductance in its I-V characteristics (Fig.1.3) [2, 3]. NDC blocks have been widely used for applications that essentially require signal amplification, hysteresis and/or memory (such as *Schmitt* triggers, amplifiers, oscillators, and logic memory circuits) [4]. NDC blocks can be implemented using traditional CMOS technology, emerging nano-scale devices such as SET, or hybrid CMOS-SET framework. However, research shows that SET-based implementations are desirable due to their high integration density and/or low power consumption. This is especially true for applications that require multiple-peak NDC characteristics (such as multiple-valued memory cells) as SET devices demonstrate their unique *Coulomb* blockade oscillations. Indeed, recent work reported NDC implementations using three tunnel junctions for binary logic or five junctions for multiple-valued logic [5, 6].

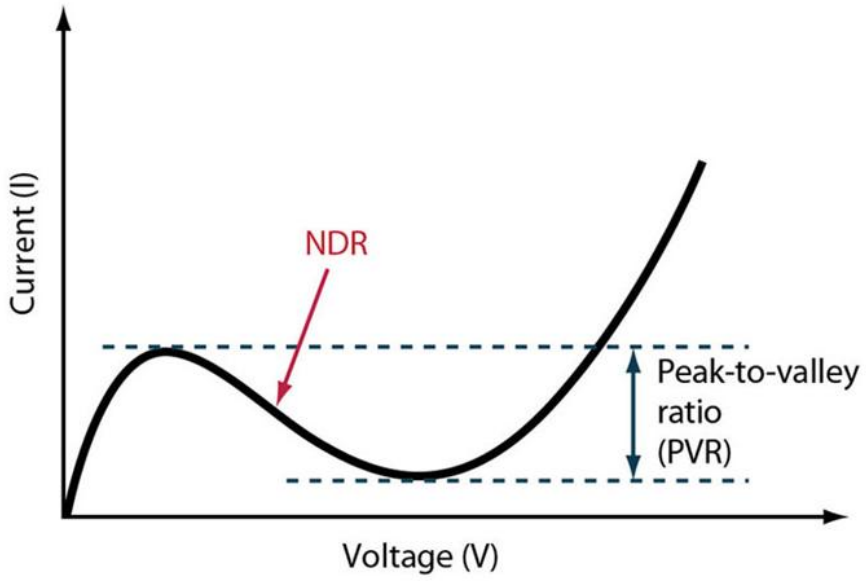


Fig 1.3 Negative Differential resistance characteristic curve

1.2 Organisation of this thesis

This thesis is organized as follows. Chapter 2 provides a background on the Nano electronic design and discusses the key concerns of SET technology. Later some basic information is presented for the *Monte Carlo* simulator for SET.

Chapter 3 presents a new single-electron tunneling based NDC block, and develops an analytical model which can be used for related circuit designs and/or their performance optimization. Simulation results are provided to show the effectiveness of the model with considerations of temperature effects.

Chapter 4 deals with different applications for SET-based NDC devices. A piece-wise model is used to describe the I-V characteristics of the device for efficient performance analysis and optimization with application circuits. Simulation results are

shown to verify the effectiveness of the proposed approach with considerations of temperature effects. In chapter 5, we propose a novel design of ternary full adder (TFA) using hybrid SET and MOS technology. The proposed circuit is evaluated using the Cadence Spectre simulator with 180nm CMOS technology and SET macro models under various test conditions. Results show that the proposed TFA dramatically reduces the number of transistors required with little or no loss in energy efficiency.

Chapter 6 concludes the thesis along with some future research works. The appendix includes the important code for our NDC model using MATLAB and VERILOG.

Chapter 2

Background of Nano electronic Design

2.1 CMOS Scaling Limits

The continuous shrinking of MOSFET device dimensions has been the main catalyst for the stunning growth of the modern microelectronic industry. The minimum feature size is fast approaching 100nm in the next decade with switching charges containing 1000 or less electrons. Moore's law is expected to break down for conventional microelectronics for a variety of reasons [8].

Physical limit:

1) Thermal limit: $E >> k_B T$ or $E \sim 100\ k_B T$

Where E is Energy necessary to write a bit, $k_B T$ is thermal energy.

2) Quantum limit: $\Delta E \Delta t >> h$ *or* $E/f \sim 100\ h$ (h – Planck's constant = 6.6×10-34 J ·S, f – circuit frequency).

Technological limit:

1) Power dissipation limit*:* $E \cdot f \cdot n \sim 100 W/cm2$ (maximum tolerable $\Delta E \Delta t >> h$) where n - device density.

2) Process variations, second-order effects and design complexity.

Economic limit:

The increasing costs of new semiconductor fabrication is making questionable the future of silicon CMOS.

2.2 *Coulomb* blockade effect

The *Coulomb* blockade effect is a phenomenon in which electrons cannot tunnel into the junction when the charging energy of a single electron is much larger than the thermal energy. Figure 2.1 shows the *coulomb* blockade in a single tunnel junction [9].

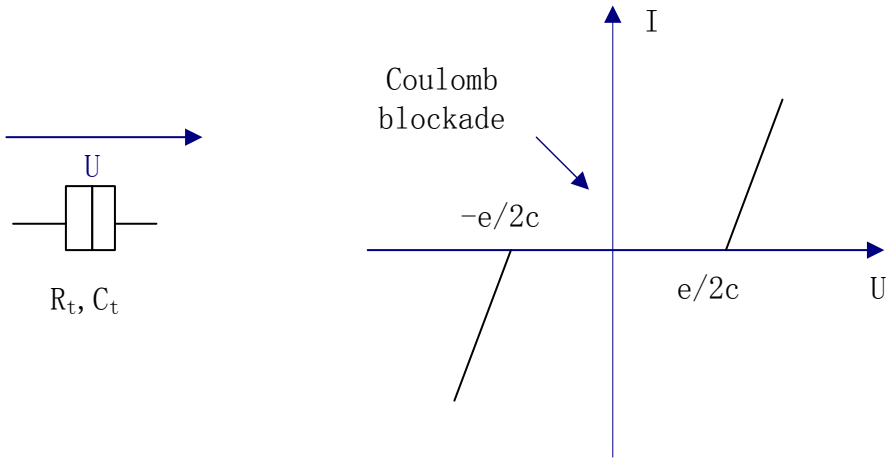


Fig 2.1 *coulomb* blockade in a single tunnel junction

The electron addition energy (E_A—the amount of work that has to be done in order to add one extra electron *e* into it) is measured as

$$E_A = E_c + E_K \approx E_c \approx \frac{e^2}{C} \tag{2.1}$$

Where C is a small spherical electro neutral conductor of capacitance E_C is the charging energy (e^2/C for a spherical conductor) and E_K is the quantum kinetic energy (usually neglected if the feature size is more than 1 nm).

Therefore, in a single-electron system, the electrons need a minimum energy for tunneling through the barrier. If the applied external biases less than this energy, no

electron can tunnel through the junction, which means the device enters into off state; such a situation is the *Coulomb* blockade.

2.3 Orthodox Theory

Throughout the history of single electronics, a unique guiding role has been played by a simple but very effective "orthodox" theory. For a particular case, this theory was developed by *Kulik* and *Shekhter*. The theory makes the following major assumptions.

First of all, the electron energy quantization inside the conductors is ignored. It means that this assumption is valid when $E_k >> k_B T$ or $E_c >> E_k$.

Then, the time τ_t of electron tunneling through the barrier also can be ignored comparing with other time scales (including the interval between neighboring tunneling events).

Coherent quantum processes consisting of several simultaneous tunneling events are ignored. This assumption is valid if the resistance of all the tunnel barriers of the system is much higher than the quantum unit of resistance R_Q

$$R_Q = h/4e2 \approx 6.5\text{K}\Omega \qquad (2.2)$$

2.4 *Monte Carlo* Simulation

The orthodox single-electron theory yields a tunnel rate equation for any junction in a large circuit [11]:

$$\Gamma_n(V) = \frac{\Delta F}{e^2 R_j (1 - e^{-\frac{\Delta F}{k_B T}})} \tag{2.3}$$

Where $k_B T$ is the thermal energy, e is the electron charge, and ΔF is the change in free energy when an electron tunnels through the junction, which can be written as $\Delta F = e\,(V_j - V_c)$, where V_j is the junction voltage and V_c is the critical voltage given by $V_c = e/(2C_{total})$ with C_{total} being the total capacitance seen from the tunnel junction [9].

If this tunnel rate is coupled into a Poisson process the fundamental building blocks for a *Monte Carlo* based simulation are assembled. The Poisson distribution can be rearranged to yield

$$\tau = -\ln(r)/\Gamma \tag{2.4}$$

Where r is an evenly distributed random number from the interval [0, 1] and t is the time at which an electron tunnels through the junction.

The *Monte Carlo* procedure is as follows. Step one, all possible tunnel events with their particular tunnel rates concreting random tunnel times τ_i are computed for all events. Then, the event with the smallest t will happen first and is taken as the winner of the *Monte Carlo* step. At same time, charges and voltages are updated on all circuit nodes. New tunnel rates are calculated and a new winner is determined through stochastic sampling. If this procedure is done many times, the macroscopic behavior of the circuit

can be calculated.

Monte Carlo method is superior to other approaches due to it gives better transient and dynamic characteristics of SET circuits. The master equation deals with average probabilities and transition rates, which paint a more macroscopic picture [8]. In that method, it is not required to find the relevant states before one can start with the actual simulation as in the case of a master equation. *Monte Carlo* method is easy to trade accuracy with simulation time, and therefore, one can quickly achieve approximate results of very large circuits.

Nevertheless, there is one major disadvantage of the *Monte Carlo* method. When it comes to simulating tunneling, a plain *Monte Carlo* approach has its limitations. Tunneling is a very rare process which is difficult to resolve by a *Monte Carlo* method. It demands very long simulation times. We tackled this problem by implementing a new algorithm that combines the *Monte Carlo* and master equation methods.

2.5 SIMON—A Simulator for Single-Electron Tunnel Devices and Circuits

SIMON is a single-electron tunnel device and circuit simulator that is based on a *Monte Carlo* method. Transient and stationary simulation is offered by *SIMON* for arbitrary circuits consisting of tunnel junctions, capacitors, and voltage sources of three kinds: constant, piecewise linearly time dependent, and voltage controlled. Tunneling can be simulated either with a plain *Monte Carlo* method or with a combination of the *Monte Carlo* and master equation approach. Furthermore, as an example of the usage of *SIMON*,

we discuss the essential problem of random background charge and present possible solutions [8].

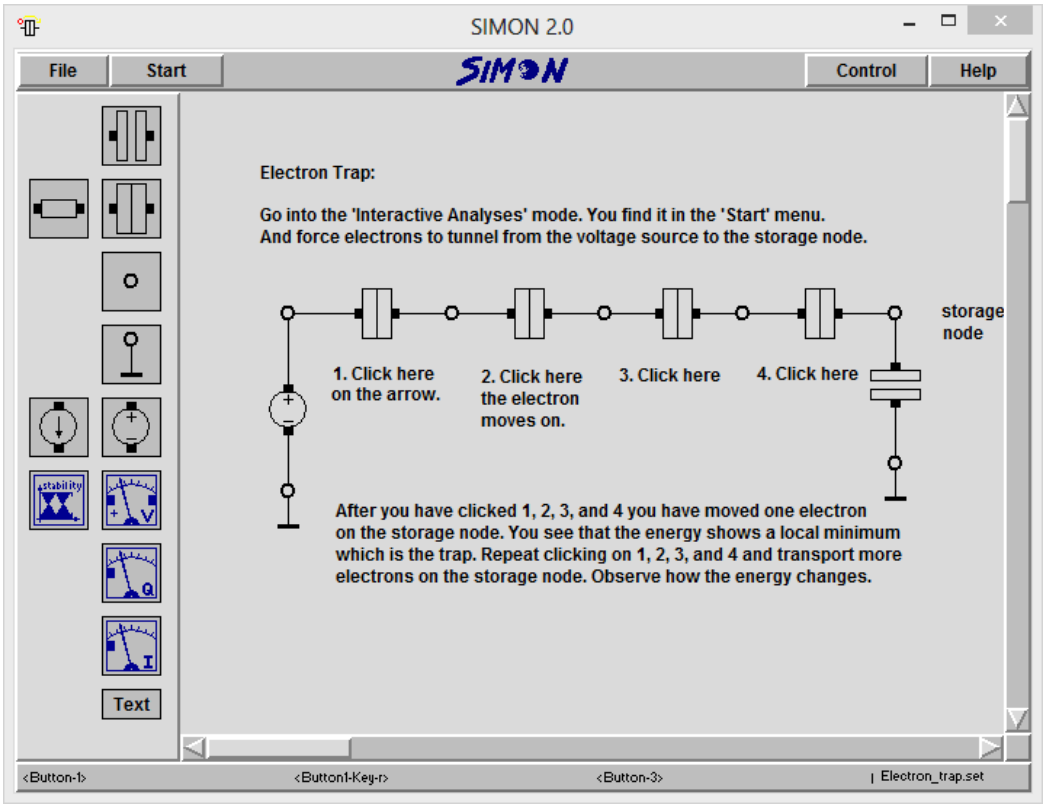


Fig 2.2 Interface of SIMON

Chapter 3

An Analytical Model for NDC Blocks with Single-Electron Tunneling

Negative differential conductance block is a subcircuit that shows both positive and negative differential conductance in its I-V characteristics. NDC blocks have been widely used for applications that essentially require signal amplification, hysteresis and/or memory (such as *Schmitt* triggers, amplifiers, oscillators, and logic memory circuits). NDC blocks can be implemented using traditional CMOS technology, emerging nano-scale devices such as single-electron tunneling, or hybrid CMOS-SET framework. However, research shows that SET based implementations are desirable due to their high integration density and/or low power consumption. This is especially true for applications that require multiple-peak NDC characteristics (such as multiple-valued memory cells) as SET devices demonstrate their unique *Coulomb* blockade oscillations. Indeed, recent work reported NDC implementations using three tunnel junctions for binary logic or five junctions for multiple-valued logic. However, there is a lack of analytical models for NDC blocks so far, making it very difficult to perform circuit analysis and/or optimization.

3.1 Previous Works

3.1.1 Three-junction NDC block

The schematic circuit diagram of the NDC device based on a SET is shown in Fig 3.1. The right island forms a SET, allowing a current to flow between voltage source and ground through the left island, which acts as an electron box. The capacitors C_G are capacitances coupled with islands and C_D, C_N and C_S are the capacitances of tunnel junctions [5].

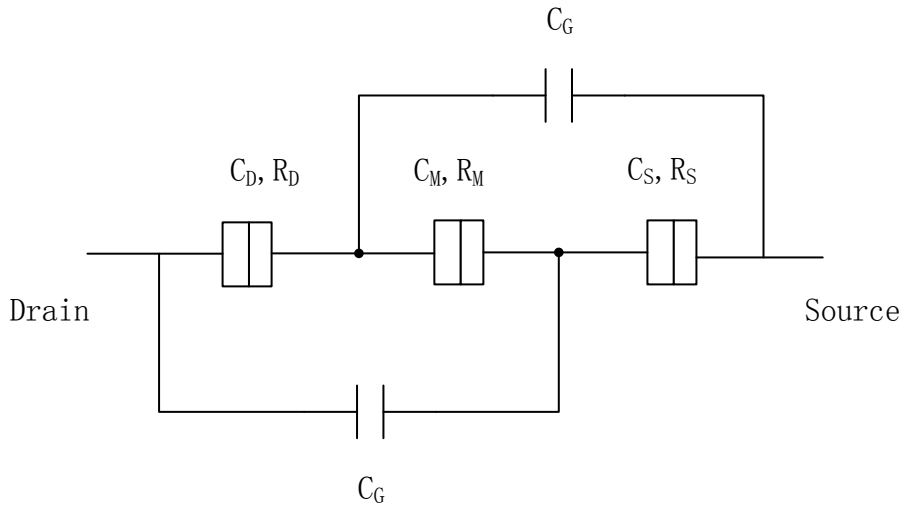


Fig 3.1 the three junctions SET-based NDC block

3.1.2 Three-junction NDC block

Fig 3.2 shows the proposed multiple-peak NDC structure, which consists of four islands. The islands 1 and 3 form two cross-coupled single-electron transistors (SET 1 and SET 2). The capacitors C_g and C_o are capacitances coupled with the islands, and C_d, C_a, C_m, C_b and C_s are the tunnel capacitors [6].

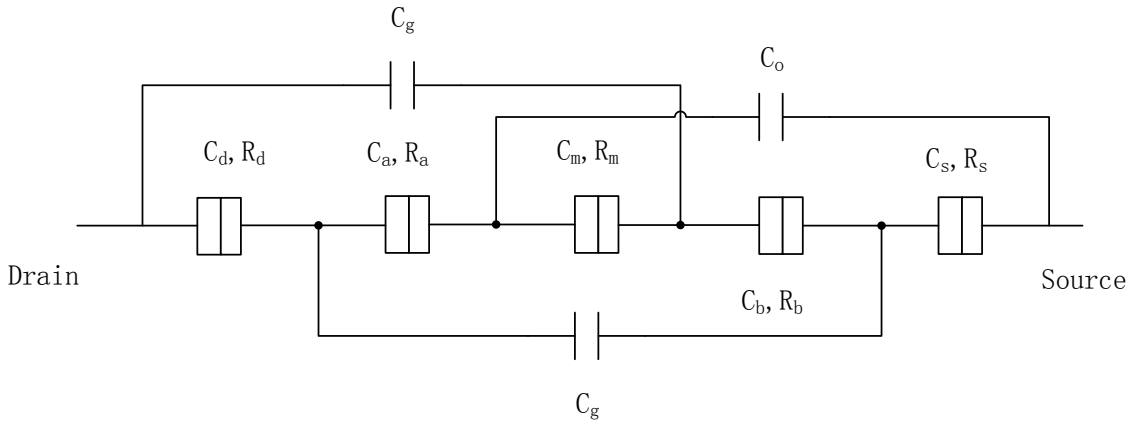


Fig 3.2 the five junctions SET-based NDC block

3.2 The Proposed Model

3.2.1Four-Junction NDC Block

Fig 3.3 shows a four-junction NDC block with symmetric structure, where C_j and R_j are the capacitance and resistance of each tunnel junction, and C_{g1} and C_{g2} can be adjusted to obtain a different number of peaks in the NDC I-V characteristic.

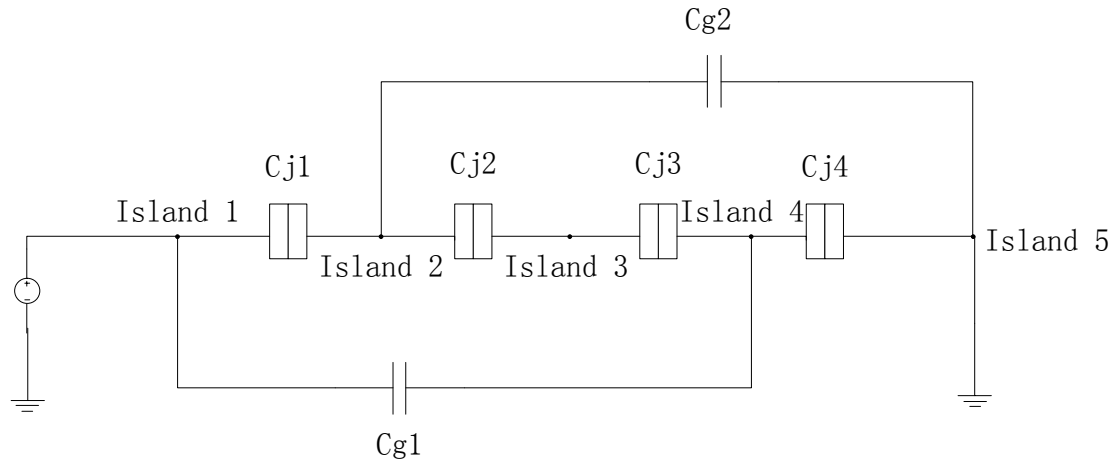


Fig 3.3 The proposed multiple-peak SET-based NDC block

3.2.2 Piece-Wise Model

To calculate the island voltages in Fig 3.3, we first define an island capacitance matrix as follows:

$$C = \begin{bmatrix} C_j + C_{g1} & -C_j & 0 & -C_{g1} \\ -C_j & 2C_j + C_{g2} & -C_j & 0 \\ 0 & -C_j & 2C_j & -C_j \\ -C_{g1} & 0 & -C_j & 2C_j + C_{g1} \end{bmatrix} \tag{3.1}$$

where the diagonal element c_{ii} (i = 1~4) represents the total capacitance of island i, while the c_{ij} (i, j = 1~4 and $i \neq j$) represents the negative value of capacitance between islands i and j. Assume the charges on islands 1 through 4 are q_1, q_2, q_3 and q_4, respectively.

For a given input voltage V_1 at island 1, the voltages on other islands (i.e., V_2, V_3 and V_4) are determined by

$$Q = CV \tag{3.2}$$

Where $\boldsymbol{Q} = [q_1\ q2\ q3\ q4]^{\mathrm{T}}$ and $\boldsymbol{V} = [V_1\ V2\ V3\ V4]^{\mathrm{T}}$.

If we further define a specific charge distribution on islands 2, 3 and 4 (i.e., { q_2 q_3 q_4}) as a state {n}, then the tunnel rate for the tunneling that causes the state transition from state n to the next state is given by [7]

$$\Gamma_n(\mathbf{V}) = \frac{\Delta F}{e^2 R_j (1 - e^{-\frac{\Delta F}{k_B T}})} \tag{3.3}$$

where R_j is the tunnel junction resistance, k_BT is the thermal energy, e is the electron charge, and ΔF is the change in free energy when an electron has tunneled through the tunnel junction, and can be written as $\Delta F = e\ (V_{jun} - V_{cr})$, where V_{jun} is the junction voltage and V_{cr} is the critical voltage given by $V_{cr} = e/\ (2C_{total})$ with C_{total} being the total capacitance seen from the tunnel junction.

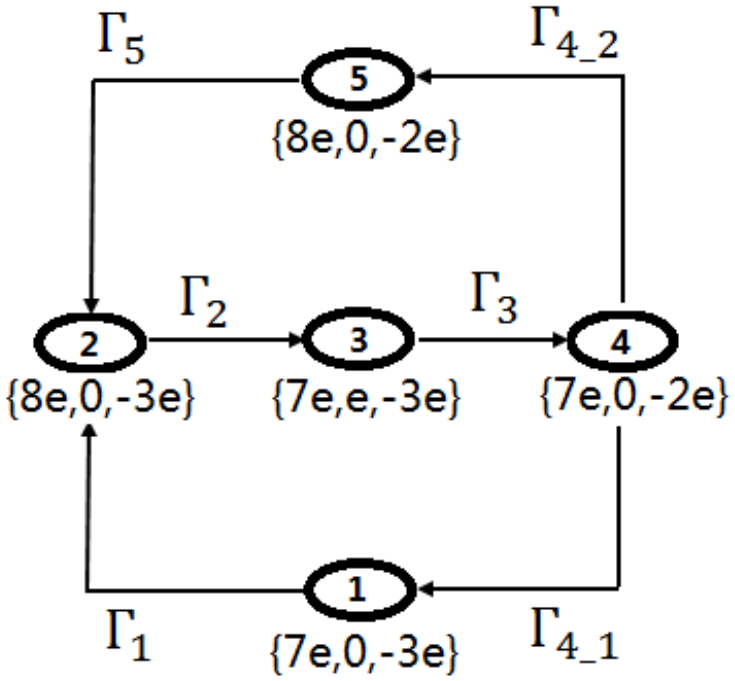


Fig 3.4 the state transition diagram

If a certain voltage V_1 causes a continuous state transition, there will be a static current flowing through the NDC block. Otherwise, the block will enter a *Coulomb blockade* (CB) with no current. It is found that when the continuous state transition occurs, the following state transition cycles will occur: $\{7e, 0, -3e\} \rightarrow \{8e, 0, -3e\} \rightarrow \{7e, e, -3e\} \rightarrow \{7e, 0, -2e\} \rightarrow \{7e, 0, -3e\}$, or $\{7e, 0, -3e\} \rightarrow \{8e, 0, -3e\} \rightarrow \{7e, e, -3e\} \rightarrow \{7e, 0, -2e\} \rightarrow \{8e, 0, -2e\} \rightarrow \{8e, 0, -3e\} \rightarrow \{7e, 0, -3e\}$. This process is described by the state transition diagram shown in Fig 3.4. Using *Markov* chain analysis on Fig 3.4 [11], the state probabilities (denoted by P_1~P_5) can be found using the following equations:

$$\left.\begin{aligned} & P_1 * \Gamma_1 = P_4 * \Gamma_{4\_1} \\ & P_2 * \Gamma_2 = P_1 * \Gamma_1 + P_5 * \Gamma_5 \\ & P_3 * \Gamma_3 = P_2 * \Gamma_2 \\ & P_3 * \Gamma_3 = P_4 * (\Gamma_{4\_1} + \Gamma_{4\_2}) \\ & \sum_{i=1}^{5} P_i = 1 \end{aligned}\right\} \quad (3.4)$$

Then the islands' state probabilities are derived by using Markov chain analysis [8].

$$P_1 = \frac{1}{\Gamma_1 * [\frac{1}{\Gamma_1} + \frac{\Gamma_{4\_2} + \Gamma_{4\_1}}{\Gamma_2 * \Gamma_{4\_1}} + \frac{\Gamma_{4\_2} + \Gamma_{4\_1}}{\Gamma_4 * \Gamma_3} + \frac{1}{\Gamma_{4\_1}} + \frac{\Gamma_{4\_2}}{\Gamma_5 * \Gamma_{4\_1}}]} \quad (3.5)$$

$$P_3 = \frac{(\Gamma_{4\_2} + \Gamma_{4\_1}) * \Gamma_1}{\Gamma_3 * \Gamma_{4\_1} * P1} \quad (3.6)$$

$$P_5 = \frac{\Gamma_{4\_2} * \Gamma_1}{\Gamma_5 * \Gamma_{4\_1} * P1} \quad (3.7)$$

$$P_4 = \frac{\Gamma_1}{\Gamma_{4\_1} * P1} \quad (3.8)$$

$$P_2 = 1 - (P_1 + P_3 + P_4 + P_5) \quad (3.9)$$

The static current can be calculated at any tunnel junction (say, the first junction between islands 1 and 2) by combining the tunnel rate(s) with state probabilities as:

$$I = I_1 = (P_1 * \Gamma_1 + P_4 * \Gamma_{4\_2}) * e \quad (3.10)$$

As V_1 increases, the NDC may go through a number of *CB* areas. The edges of all CB areas are denoted by threshold voltages V_{th1}, V_{th2}, and can be estimated using (3.12 and 3.14) with a specific state and tunnel condition. According to the orthodox theory, threshold voltages will be divided into V_{thi} and V_{thj} which represent odd and even number of threshold voltages due to different tunnel conditions. Equations using to find the V_{thi} are given as follows:

$$\begin{cases} Q = CV \\ Vc1 = Vj1 \\ Vc2 = Vj2 \end{cases} \tag{3.11}$$

$$V_{thi}=\frac{q2+(Cj+Cg2)*Vc1-cj*Vc2}{Cg2} \tag{3.12}$$

Where $q_2 = [7+ (i-1)/2]*e$, and i is an odd integer. Similarly, if i is an even integer, the tunneling conditions are: $V_{c2} = V_{j2}$ and $V_{c3} = V_{j3}$, and $V_{th,i}$ can be expressed as:

$$\begin{cases} Q = CV \\ Vc3 = Vj3 \\ Vc2 = Vj2 \end{cases} \tag{3.13}$$

$$V_{th\,j=}\frac{[q4+ (3*Cj+2*cg1)*Vc2]*(Cj+cg2)-(q2-Cj*Vc2)*(Cj+cg1)}{Cj*(Cj+cg1)-cg1*(Cj+cg2)} \tag{3.14}$$

Where $q_2 = (7+i/2)*e$, $q_4 = -3e$, and i is an even integer. Our simulations show that the static current during either positive or negative conductance portion of the block is almost linearly proportional to the input voltage. This suggests that the current can be expressed as a piece-wise linear function in terms of the peak currents and threshold voltages:

$$I = \begin{cases} 0, & if\ V < V_{th1} \\ k_1(V - V_{th1}), & if\ V_{th1} \le V < (V_{th1} + V_{th2})/2 \\ k_1(V_{th2} - V), & if\ (V_{th1} + V_{th2})/2 \le V < V_{th2} \\ 0, & if\ V_{th2} \le V < V_{th3} \\ k_2(V - V_{th3}), & if\ V_{th3} \le V < (V_{th3} + V_{th4})/2 \\ k_2(V_{th4} - V), & if\ (V_{th3} + V_{th4})/2 \le V < V_{th4} \\ \vdots & \vdots \end{cases} \tag{3.15}$$

where $V = V_1$, $k_1 = 2I_{peak1}/(V_{th2}-V_{th1})$, $k_2 = 2I_{peak2}/(V_{th4}-V_{th3})$, …, and $I_{peak,j}$ (j = 1, 2, …) is the j-th peak current in the NDC I-V characteristic, which is the static current when $V = (V_{th,2j-1}+ V_{th,2j})/2$.

With R_j = 1MΩ, Cj = 0.1aF and T = 0K, simulation results using SIMON, MATLAB, and the above piece-wise model are shown in Fig 3.5 for comparison, where the MATLAB results are obtained with input voltage increments of 1mV. It can be seen from the figure 3.5 that there is a good agreement among these results.

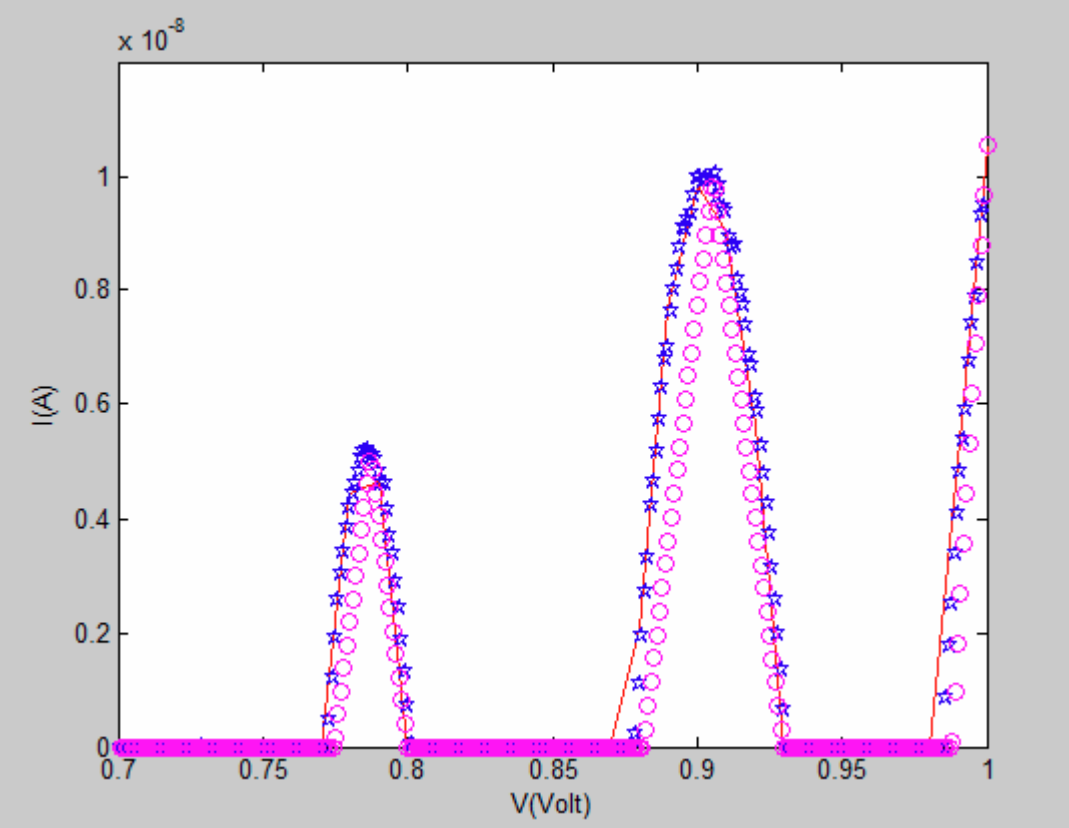


Fig 3.5 Simulation results of Fig 3.3 (T = 0K) where the stars (blue), circles (purple), and solid line (red) correspond to SIMON, piece-wise model and MATLAB, respectively.

3.3 Impacts of Circuit Parameters and Temperature

The previous discussions are based on the parameters (C_{g1} = 5C_j and C_{g2} = *15*C_j). If the NDC block is operated with different parameters, its I-V characteristic will change as well. First of all, both threshold voltages and the static current will decrease as the value of C_j increases. For instance, simulation results with C_j = 0.2aF vs. 0.1aF are shown in Fig 3.7 (a). Secondly, if C_{g2} rises, more peaks can be expected. An example with C_{g2} = 25C_j is shown in Fig 3.7 (b). Third, reducing C_{g1} will lead to a remarkable growth of even-number threshold voltages while keeping the odd-number threshold voltages almost unchanged. Fig 3.7 (c) shows the results with C_{g1} = 4.9C_j. In general, the specific changes in the static current and threshold voltages under different parameters can be found. However, it should be mentioned that the parameter changes are limited by a relatively small range. Otherwise, the negative slopes of the NDC device may disappear.

The above discussions assume the ideal temperature $T = 0K$. As T increases, both the static current and threshold voltages in the device's I-V characteristic will be shifted. As shown in Fig 3.6, with a high temperature, the tunnel rate will not reduce to zero when ΔF is zero. Since P_1 is almost 1 when V_1 equal to $V_{thi,}$ the equation of current can be expressed as:

$$I=\frac{V_{jun}-V_{cr}}{e^{\frac{V_{jun}-V_{cr}}{Vt}}}*\frac{1}{R_j} \tag{3.16}$$

Where V_T is equal to $\frac{K_b*T}{e}$, k_BT is the thermal energy, e is the electron charge.

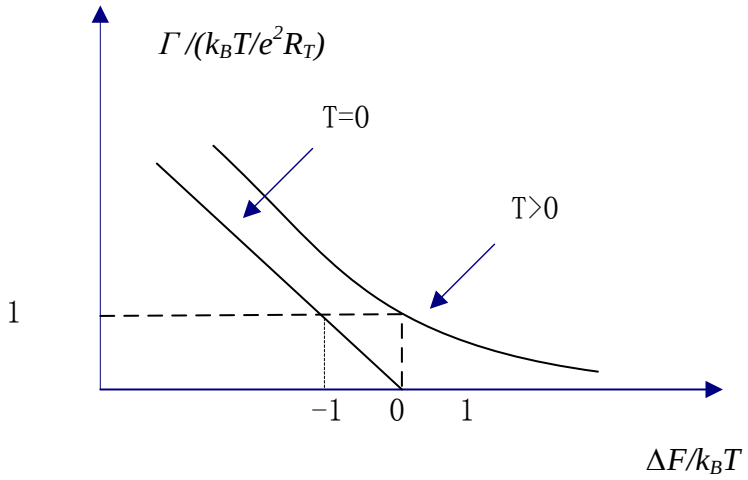
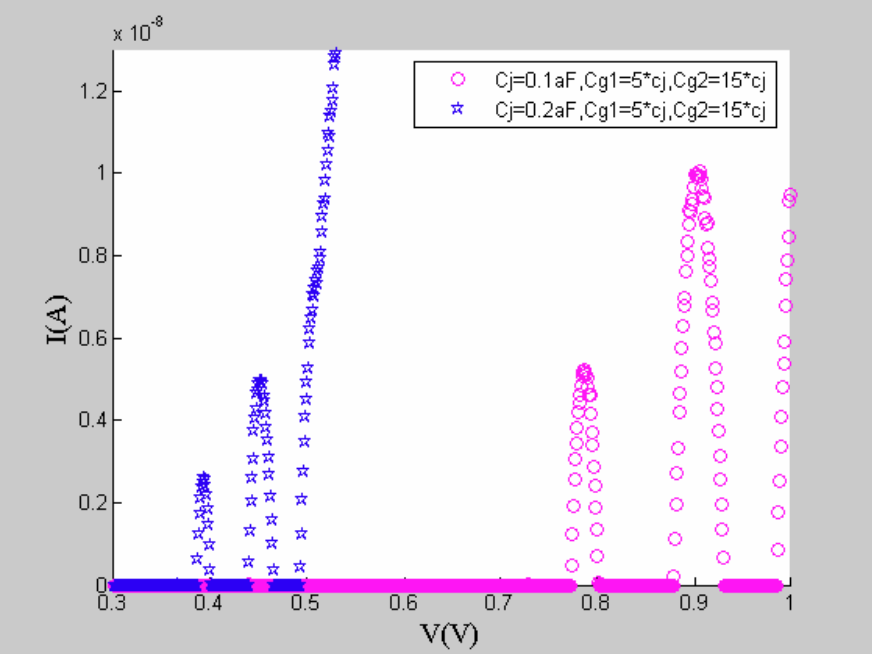


Fig 3.6 curves of tunnel rate when T=0 and T>0

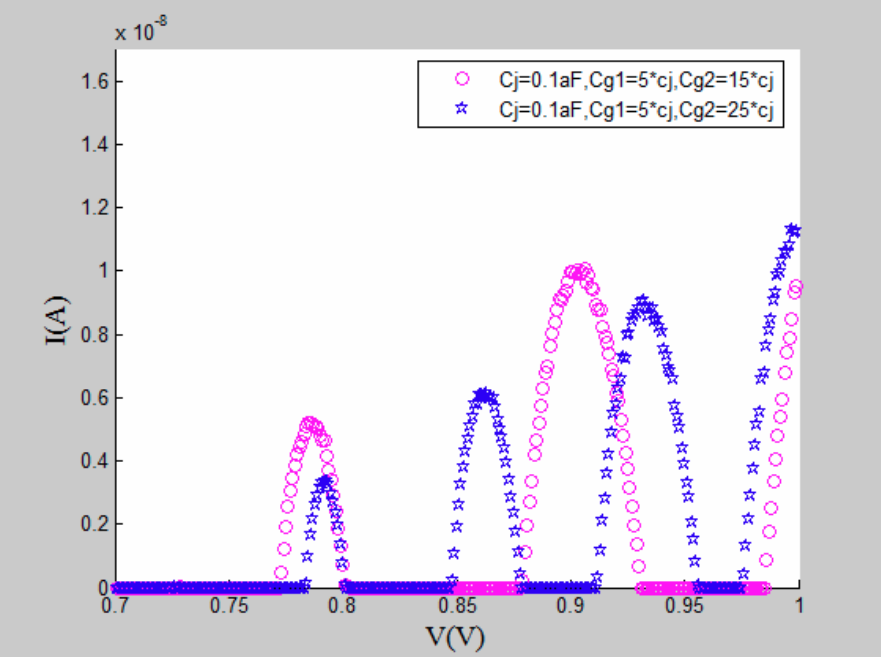
The new threshold voltages Vth,i' under the temperature T can be derived in the same way as is for Vth,i, except with new tunneling conditions: $V_{j1} = V_{c1} - V_T \ln(\beta T)$ and $V_{j2} = V_{c2}$ for i odd, or $V_{j2} = V_{c2} - V_T \ln(\beta T)$ and $V_{j3} = V_{c3} - V_T \ln(\beta T)$ for i even, where $V_T = k_B T/e$, and β is a constant depending on circuit parameters (for the original parameters, $\beta \approx 4$). Thus, the piece-wise model considering temperature effects is expressed as (when $V_{th,i'} \le V_{th,i+1'}$ for $i \ge 2$):

$$\begin{cases} 0, & if\ V < Vth1' \\ K_0 * \left(V - Vth1'\right), & if\ Vth1' < V < \frac{Vth1+Vth2}{2} \\ K_1 * \left(V - Vth2'\right), & if\ \frac{Vth1+Vth2}{2} < V < Vth2' \\ 0, & if\ Vth2' < Vd < Vth3' \\ K_2 * \left(V - Vth3'\right), & if\ Vth3' < V < \frac{Vth3+Vth4}{2} \\ K_3 * \left(V - Vth4'\right), & if\ \frac{Vth3+Vth4}{2} < V < Vth4' \\ \vdots & \vdots \\ \frac{V}{4*R_t}, & if\ V > Vc1 + Vc2 + Vc3 + Vc4 \end{cases} \tag{3.17}$$

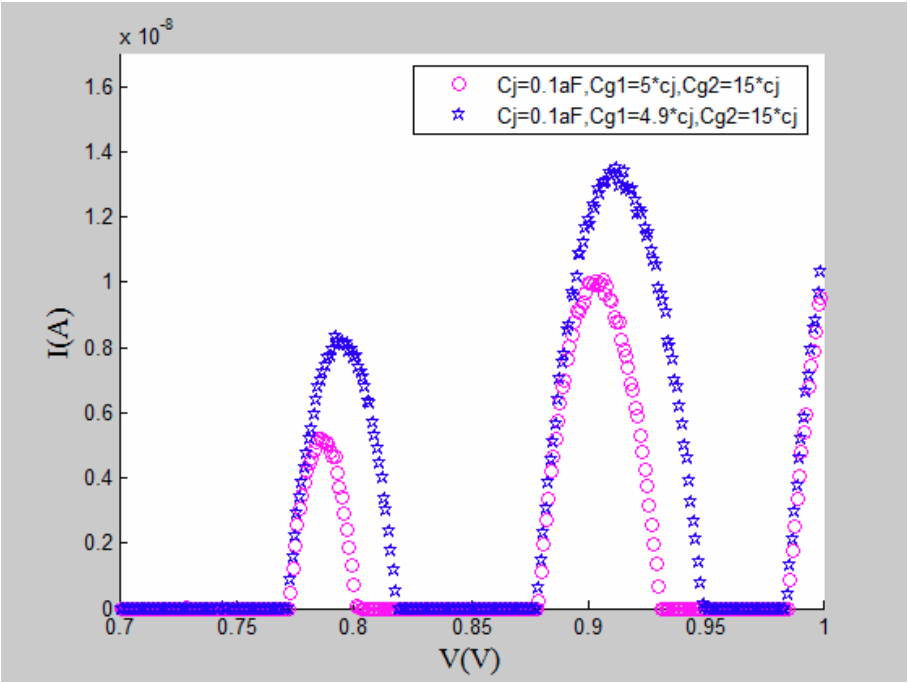
Where $V_{peak,i}=(V_{th,2i-1}+V_{th,2i})/2$ for $i = 1, 2, \ldots$, $k_{0'} = I_{peak1}/(V_{peak1}-V_{th1'})$, $k_{1'}=I_{peak1}/(V_{peak1}-V_{th2'})$, $k2'=I_{peak2}/(V_{peak2}- V_{th3'})$, $k3'=I_{peak2}/(V_{peak2}-V_{th4'})$, …, and I_{peak},i is given by (5) with $V = V_{peak,i}$.



(a)



(b)



(c)

Fig 3.7 Simulation results of Fig 3.3 with (a) Cj = 0.2aF, $Cg1$ = 5Cj and $Cg2$=15Cj, (b) Cj = 0.1aF, $Cg1$ = 5Cj and $Cg2$ = 25Cj, and (c) Cj = 0.1aF, $Cg1$ = 4.9Cj and $Cg2$=15Cj, where the circles (purple) and stars (blue) correspond to original parameters (i.e., Cj = 0.1aF, $Cg1$ = 5Cj and $Cg2$=15Cj) and new parameters, respectively.

As T keeps increasing, the even-number and odd-number threshold voltages may overlap, resulting in $V_{th,i'} > V_{th,i+1'}$ for $i \geq 2$. In this case, (3.17) shall be modified as:

$$\begin{cases} 0, Vd < Vth1' \\ K_0 * (V - Vth1), Vth1 < V < Vpeak1 \\ K_1 * (V - Vvalley1) + I_{valley1}, Vpeak1 < V < Vvalley1 \\ K_2 * (V - Vvalley1) + I_{valley1}, Vvalley1 < V < Vpeak2 \\ K_3 * (V - Vvalley2) + I_{valley2}, Vpeak2 < V < Vvalley2 \\ \vdots \\ \dfrac{V}{4 * R_t}, V > Vc1 + Vc2 + Vc3 + Vc4 \end{cases} \tag{3.18}$$

where $k_{0}'=I_{peak1}/(V_{peak1}-V_{th1'})$, $k1''=(I_{peak1}-I_{valley1})/(V_{peak1}-V_{valley1})$, $k_{2}'=(I_{peak2}-I_{valley1})/(V_{peak2}-V_{valley1})$, $k3''=(I_{peak2}-I_{valley2})/(V_{peak2}-V_{valley2})$, … , and $I_{valley,i}$ is the i-th valley current in the NDC's I-V characteristic, which is the static current when V = $V_{valley,i}$, while $V_{valley,i}$ ($i \geq 1$) is determined by

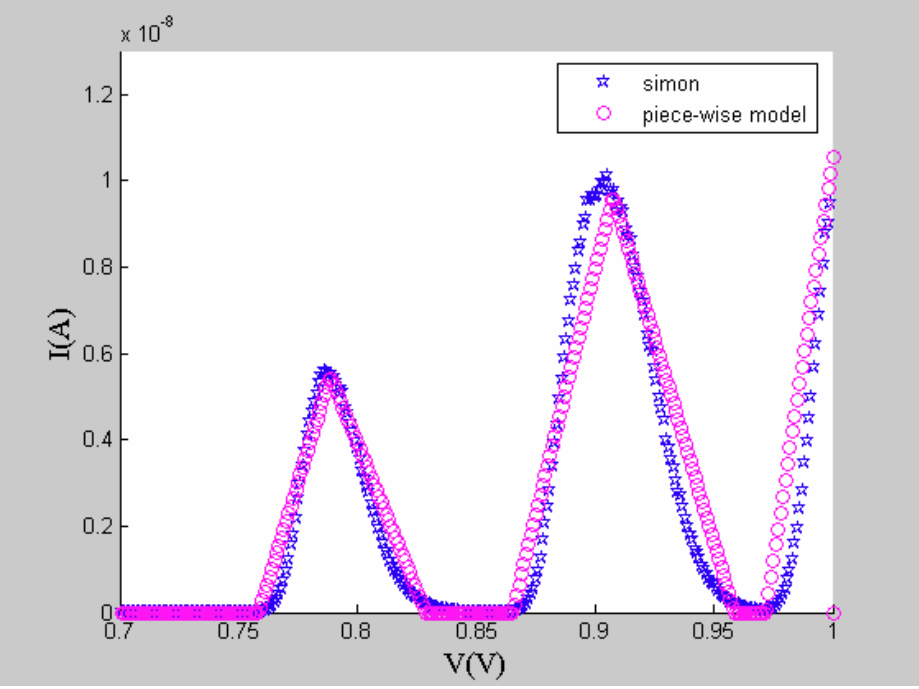
$$K_i * (V_{valley} - V'_{th,i+1}) = K_{i+1} * (V_{valley} - V'_{th,i+2}) \quad (3.19)$$

Or

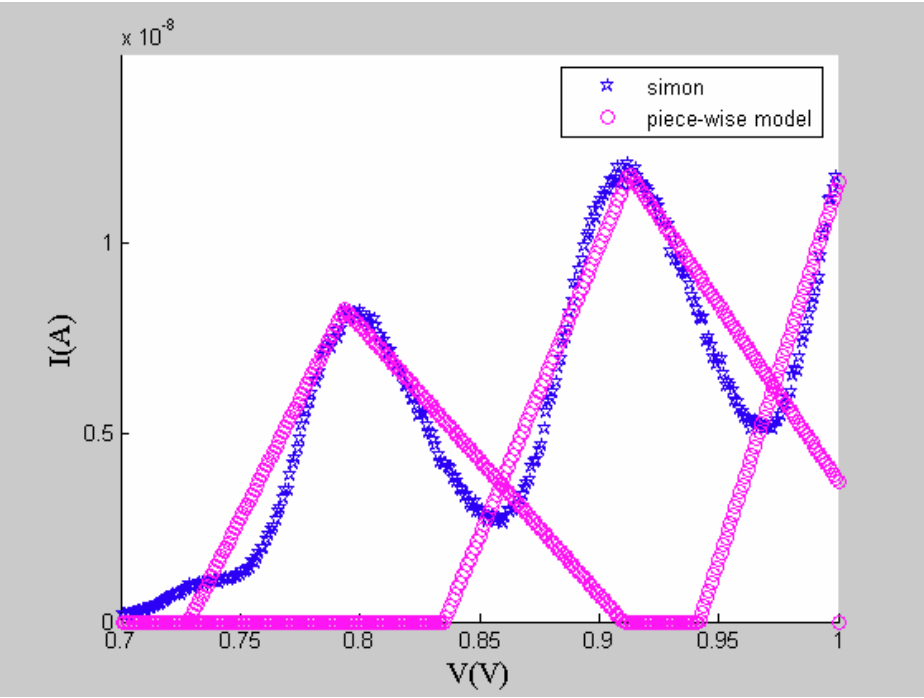
$$V_{valley,i} = \frac{K''_i * V'_{th,i+1} - K''_{i+1} * V'_{th,i+2}}{(K''_{i+1} - K''_i)} \quad (3.20)$$

3.4 Simulation Results and Discussion

Fig 3.8 shows the simulation results of Fig 3.3 under different temperatures. To further verify the impacts of circuit parameters on its I-V characteristic under different temperatures, we also conducted simulations for Fig 3.3 with different parameters and temperatures. Fig 3.9 shows the results when C_j = 0.1aF, C_{g1} = 5Cj, C_{g2} = 35C_j with T = 50K. It can be seen from the figures that the results from the proposed piecewise model match those from SIMON simulations very well.



(a)



(b)

Fig 3.8 Simulation results of Fig 3.3 with Cj = 0.1aF under (a) T = 25K and (b) T = 77K, where the stars (blue) and circles (purple) correspond to SIMON and piece-wise model, respectively.

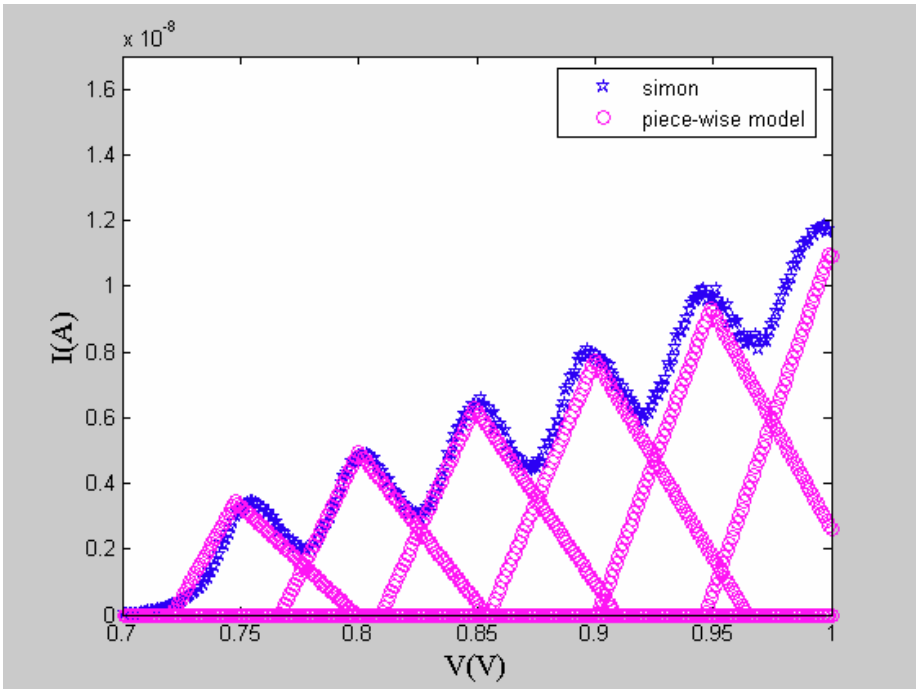


Fig 3.9 Simulation results for Fig 3.3 (Cj = 0.1aF, $Cg1$ = 5Cj, $Cg2$ = 35Cj, and T = 50K), where the stars (blue) and circles (purple) correspond to SIMON and piece-wise model (i.e., (10)), respectively.

Chapter 4

Modeling and Application for Negative-Differential-Conductance Devices with Single-Electron Technology

NDC elements find many applications in both digital and analog circuits, such as memory cells and *Schmitt* triggers. Research shows that single-electron tunneling technology is especially suitable for NDC block implementations due to the unique *Coulomb* oscillations with SET devices.

4.1 Previous Works

4.1.1 G^4-FET Voltage-Controlled NDR Device

The schematic of the conventional, 2-terminal NDR device is shown in Fig 4.1 (a). The G^4-NDR is obtained by replacing the JFETs in Fig 4.1 (a) with complementary G^4-FETs (Fig 4.1 (b)). The resulting structure is a 4-terminal device, the extra 2 terminals being the front-gate (GI) of the n-channel and p-channel G^4-FETs, driven by the voltages V_N and V_p, respectively [4].

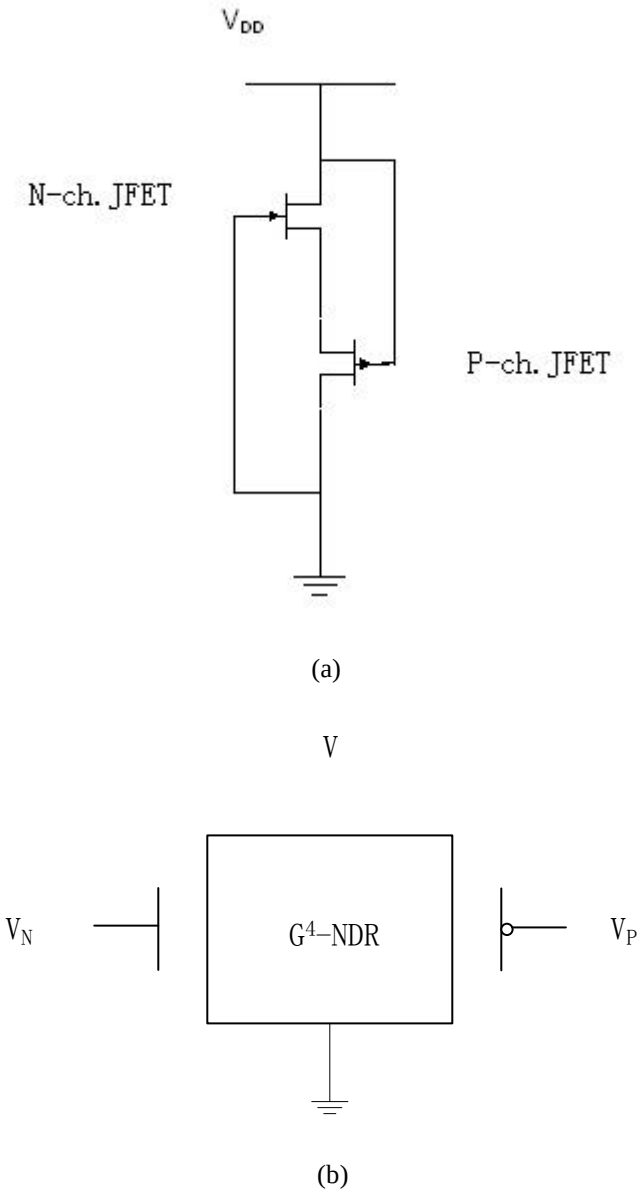


Fig 4.1 (a) Conventional 2-terminal JFET NDR device (b) Symbol of the 4-terminal G^4-NDR

4.1.2 LC Oscillator

As an application example, the G^4-NDR loaded with an LC tank constitutes an LC oscillator (Fig 4.2). The circuit operation is based on the cancellation of the LC circuit resistive losses by the G^4-NDR [4].

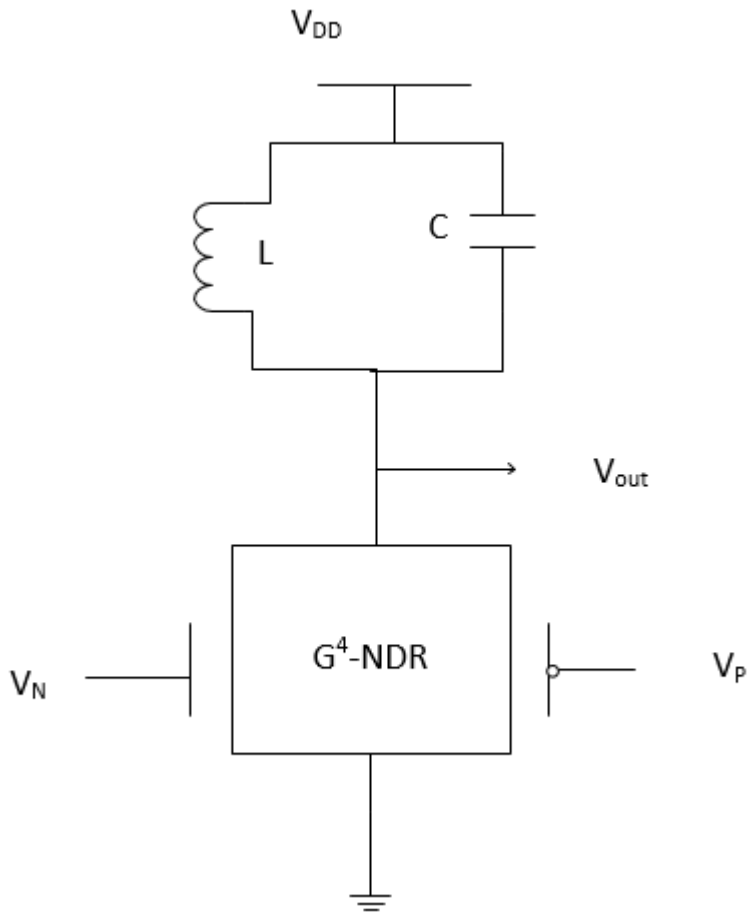


Fig 4.2 schematic of LC oscillator

4.1.3 *Schmitt* Trigger

The *Schmitt* Trigger circuit is obtained by loading the G^4-NDR with a regular inversion-mode PMOS load and connecting the gate of the PMOSFET to the n-type MOS gate input of the G^4-NDR as shown in Fig 4.3.

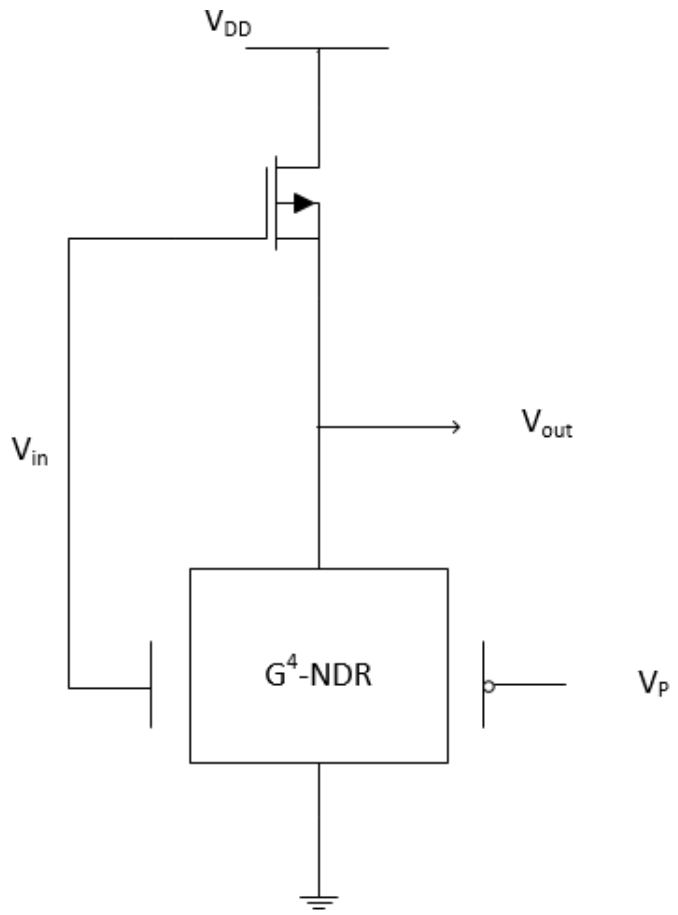


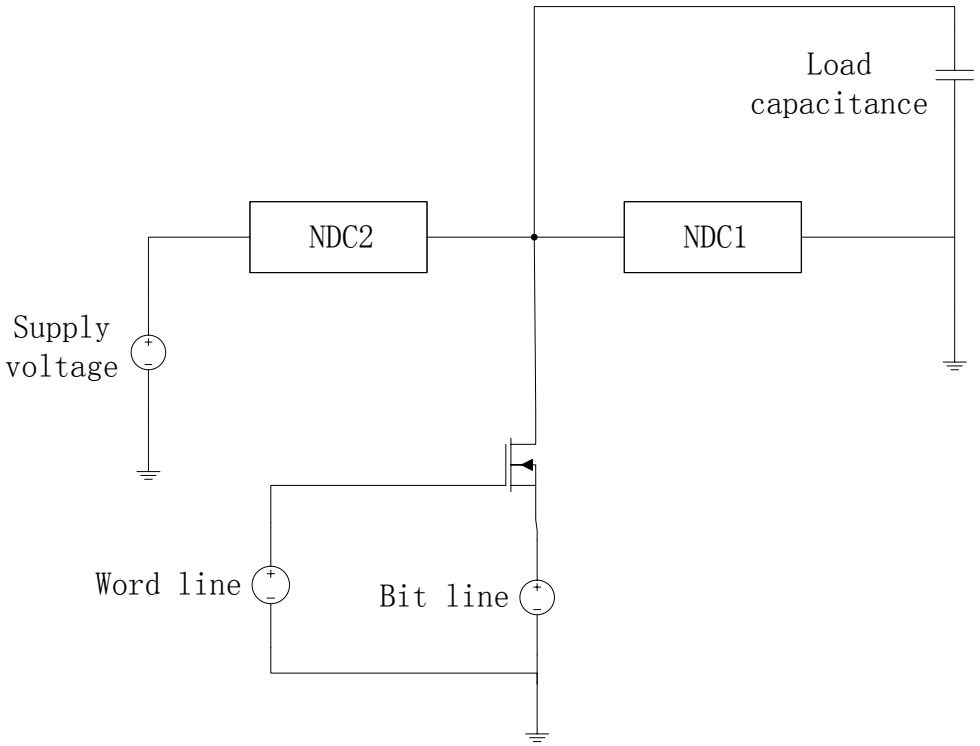
Fig 4.3 schematic of *Schmitt* Trigger

4.2 Multiple-Valued Logic Memory Cells

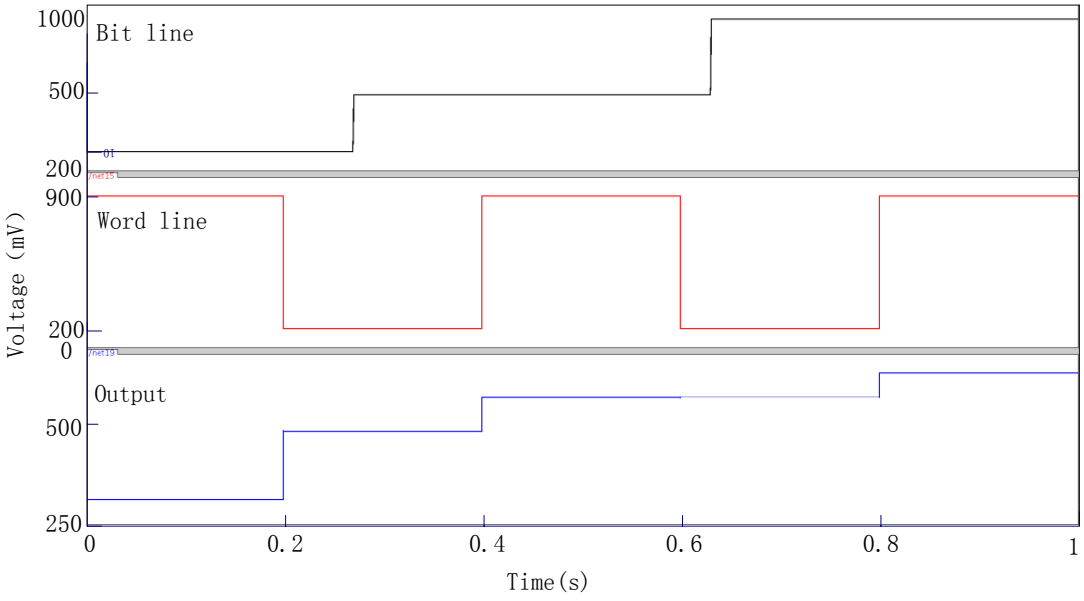
4.2.1 Schematic Circuit

Multiple-valued logic static memory cell can be designed using two NDCs, as shown in Fig 4.4 (a) where an extra NMOS switch is used for cell access. The parameters for both NDCs are: R_j = 1 MΩ, $C_{j1\sim j4} = C_j$ = 0.176aF, C_{g1} = 0.86aF, C_{g2} = 2.64aF. The power supply voltage is biased at 1V. The parameters for the NMOS transistor are: *W/L* = 0.5μm/0.18μm, V_{gs} = 0.9V (for ON state) or 0.2V (for OFF state). The memory cell

operates with three logic states: logic “0”, “1” or “2”. For the supply voltage of 1V, these three logic voltages are approximately 0.44V, 0.5V and 0.56V.



(a)



(b)

Fig 4.4 (a) Schematic for the memory cell, (b) bit-line waveform, word-line waveform, and output

waveform at memory node S

4.2.2 Write Operation for Memory Cell

In Fig 4.4 (a), when both bit line and word line are activated, the input data is written to the memory node. Once the NMOS switch is OFF, the memory node latches to one of three logic voltage levels, depending on the written input. Fig 4.4 (b) shows the simulation results for the write operation. By adjusting parameters and/or supply voltage, each logic state can be designed to take place near the valley of the NDC's I-V characteristics in order to minimize the current required to hold the states. Fig 4.5 shows three logic states when NDC parameters are: $C_{j1\sim j4} = C_j$ =0.176aF, C_{g1} = 0.86aF, and C_{g2} = 2.64aF. It should be mentioned that the two extra intersection points (i.e., *A* and *B*) in Fig 4.5 are unstable, and thus do not correspond to any logic state. This is due to the fact that if the voltage (*V*) at node *S* increases unexpectedly from V_A or V_B, the current in NDC_2 would be greater than that in NDC_1. As a result, the load capacitance C_L would be charged, causing the V_A or V_B to further increase until it reaches a stable logic state ("1" or "2"). Similarly, the operating point would leave the point *A* or *B* as well if there is a voltage reduction/disturbance happening at the node *S*. Therefore, there are only three stable points in the figure.

4.2.3 Impacts of Circuit Parameters

If NDC blocks are operated with different parameters, their I-V characteristics will change and the above NDC-based memory cell can operate with different performance (including the peak-to-valley current ratio, power consumption and noise margin). In Fig 4.5, for example, the average logic margin is approximately 60mV. In order to increase

the logic margin of this memory cell, an alternative set of parameters can be used. For instance, with $C_{j1} = C_{j2} = C_{j4} = C_j = 0.05$aF, $C_{j3} = 0.35$aF, $C_{g1} = 5.6C_j$ and $C_{g2}=15.5C_j$, the operating points of the memory are shown in Fig 4.6, where stars/circles and solid curves represent the I-V characteristics before and after parameter changes, respectively. It can be seen from this figure that the logic margins are improved significantly to around 200mV, on average, at a cost of more static power.

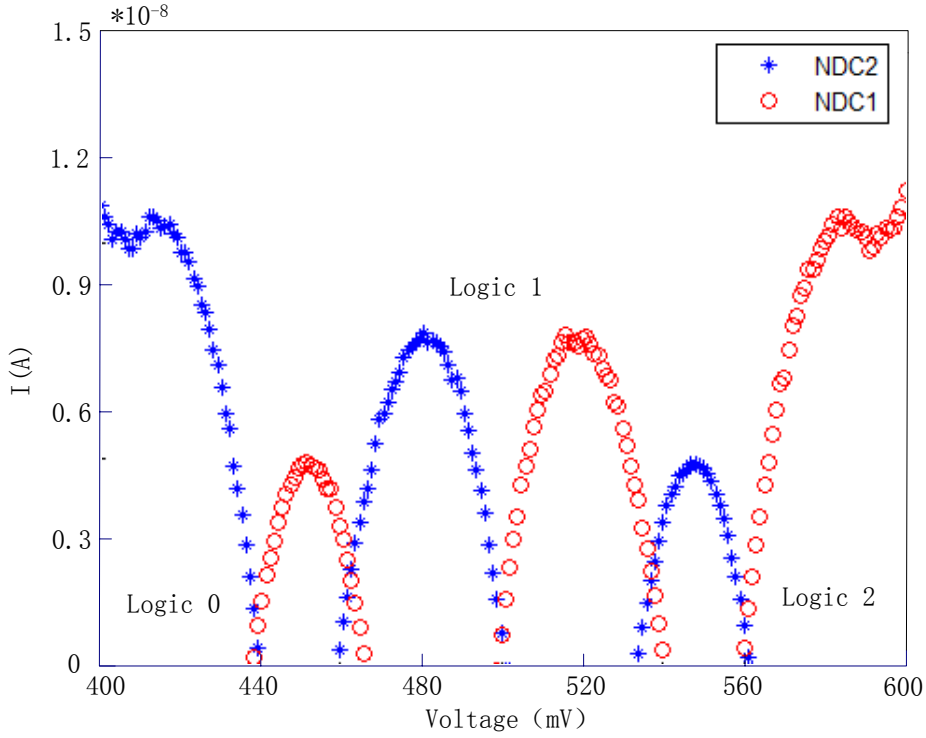


Fig 4.5 Logic voltages for the memory cell using two-peak NDC elements with $C_{j1\sim j4} = C_j = 0.176$aF, $C_{g1} = 0.86$aF, $C_{g2} = 2.64$aF at $T = 0$K, where the circles (blue) and stars (red) correspond to NDC1 and NDC2, respectively.

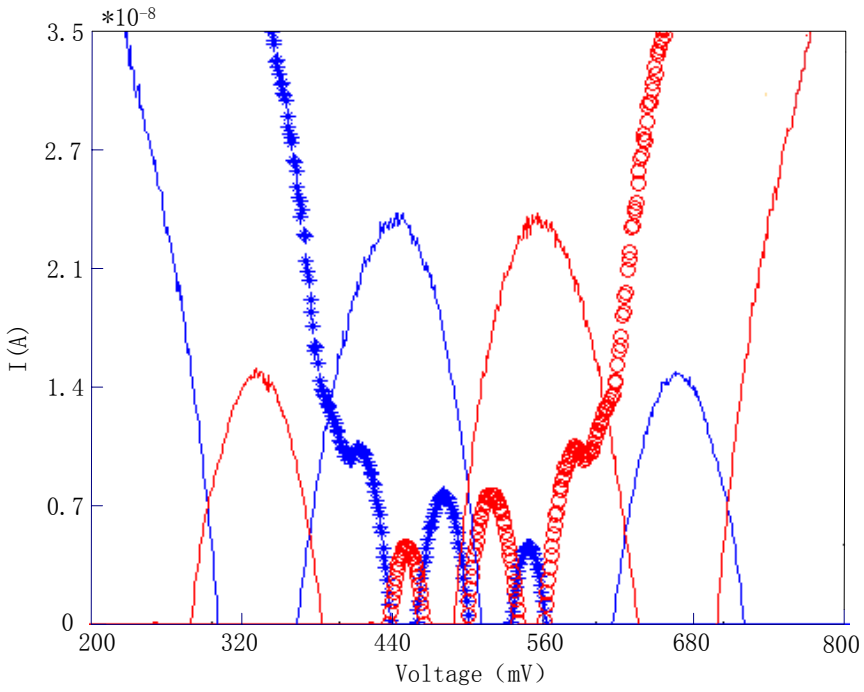


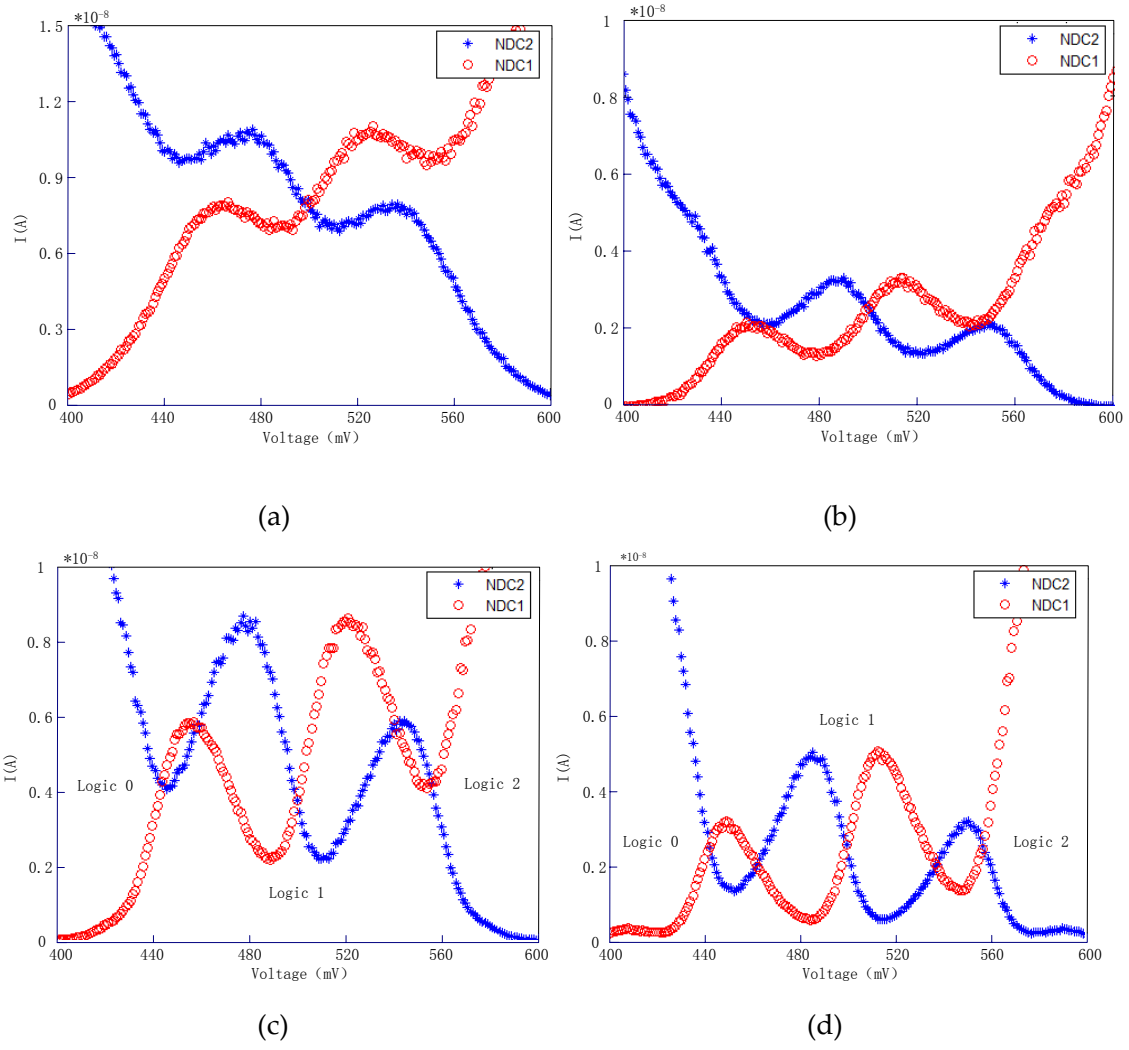
Fig 4.6 Impacts of parameters on the memory's I-V characteristics, where stars/circles correspond to the parameters of $C_{j1\sim j4} = C_j$ =0.176aF, C_{g1} = 0.86aF and C_{g2} = 2.64aF, and solid curves (with improved logic margins) correspond to the parameters of $C_{j1} = C_{j2} = C_{j4} = C_j$ = 0.05aF, C_{j3} = 0.35aF, $C_{g1} = 5.6C_j$ and $C_{g2} = 15.5C_j$.

4.2.4Temperature Effects

The above discussions assume an ideal temperature T = 0K. As T increases, both the static current and threshold voltages in the device's I-V characteristics will be shifted as well. Both simulations and analytical model show that increasing C_j will reduce both threshold voltages and the static current. This property can be used for coarse tuning at high temperatures for a reduced static current. For example, for the parameters in Fig 4.7 (a), there is only one stable point. As C_j increases, two more stable points can be obtained, as is seen in Fig 4.7 (b). On the other hand, changing C_{g1}, which only shifts the curves, will be suitable for fine adjustment, as shown in Fig 4.7 (c) and (d). In addition, for the multiple-valued memory cell, increasing the value of C_{g2} would allow for more stable

logic points.

With an alternative set of parameters, the circuit can also have an improved tolerance to a higher temperature. For instance, by choosing C_{j1} = C_{j2} = C_{j4} = C_j =0.05aF, C_{j3}= 0.35aF, C_{g1} = 5.6C_j, and C_{g2}=15.5C_j, the memory cell demonstrates three stable points at 77K, as shown in Fig 4.7 (e). This group parameter (C_{j1}= C_{j2}= C_{j4}= 0.05aF, C_{j3}=0.28aF) can actually work even at a temperature of up to 220K, as shown in Fig 4.7 (f).



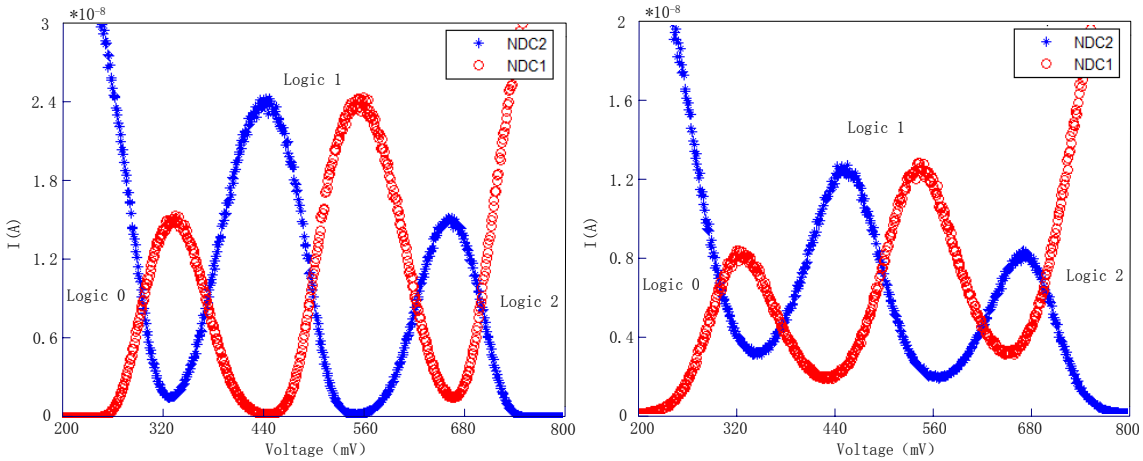


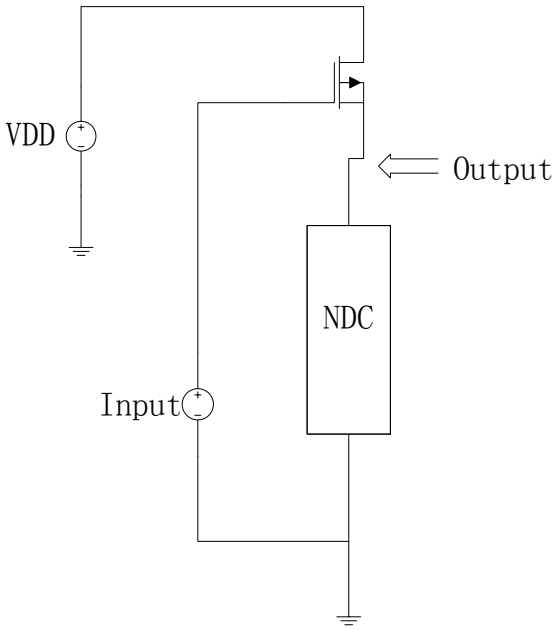
Fig 4.7 Simulation results of memory cells with (a) $C_{j1\sim j4} = C_j = 0.176$aF, $C_{g1} = 0.86$aF, $C_{g2} = 2.64$aF at $T = 77$K, (b) $C_j = 0.16$aF, $C_{g1} = 0.86$aF, $C_{g2} = 2.64$aF at $T = 77$K, (c) $C_j = 0.176$aF, $C_{g1} = 0.86$aF, $C_{g2} = 2.64$aF at $T = 40$K, (d) $C_j = 0.176$aF, $C_{g1} = 0.9$aF, $C_{g2} = 2.64$aF at $T = 40$K, (e) $C_{j1} = C_{j2} = C_{j4} = C_j = 0.05$aF, $C_{j3} = 0.35$aF, $C_{g1} = 5.6C_j$, and $C_{g2} = 15.5C_j$ at $T = 77$K, and (f) $C_{j1} = C_{j2} = C_{j4} = C_j = 0.03$aF, $C_{j3} = 0.28$aF, $C_{g1} = 5.6C_j$ and $C_{g2} = 15.5C_j$ at $T = 220$K.

4.3 *Schmitt* trigger

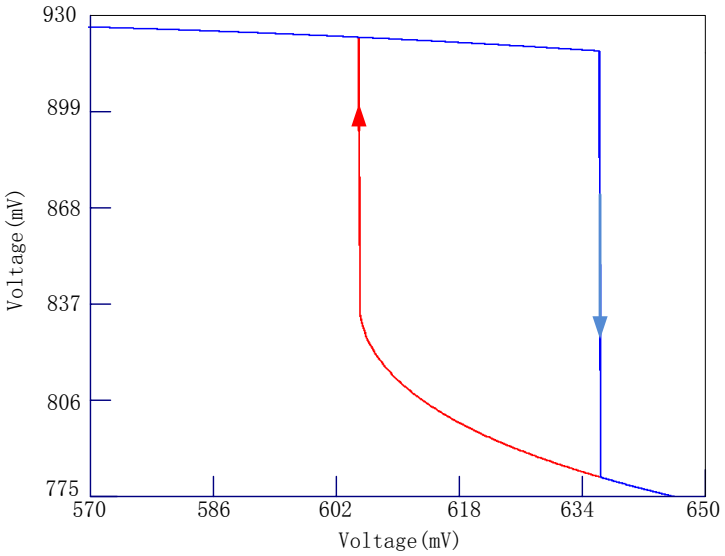
The *Schmitt* trigger circuit is designed by loading a regular PMOS transistor with an NDC, as shown in Fig 4.8 (a). The parameters for the transistor are: $W/L = 0.6\mu m/0.2\mu m$ with $V_{DD} = 1V$. Fig 4.8(b) shows its typical voltage transfer characteristic. An important feature with this NDC-based *Schmitt* trigger is that its hysteresis window can be adjusted by using different circuit parameters. Fig 4.9 (a) and (b) show two specific cases where the window shifts horizontally and vertically, respectively.

In terms of temperature effect, our analytical analysis shows that an ascending temperature will increase the static current and decrease the *Coulomb* blockade area, which makes the hysteresis window smaller and eventually disappear for much higher temperature. Fig 4.9 (c) shows that the hysteresis window is shrunk almost by half as the temperature increases from 40K to 50K, and shows the results with another set of

parameters with temperatures of 50K and 100K.

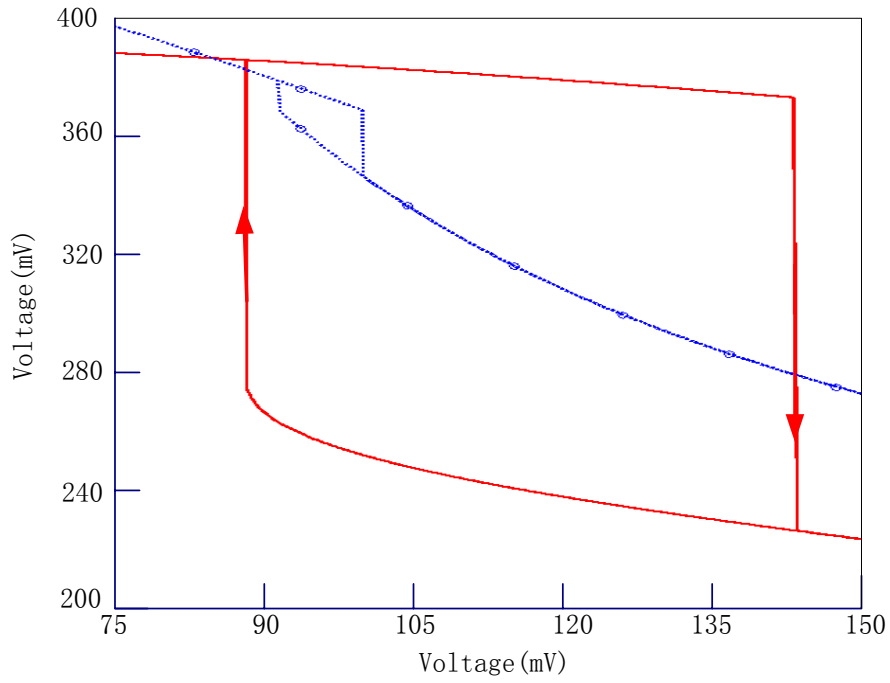


(a)

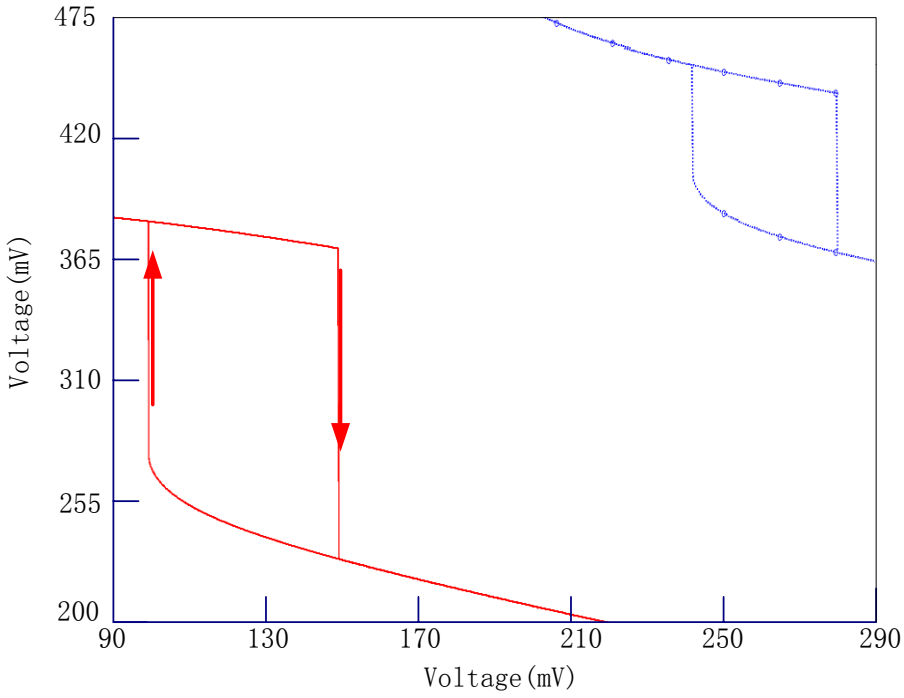


(b)

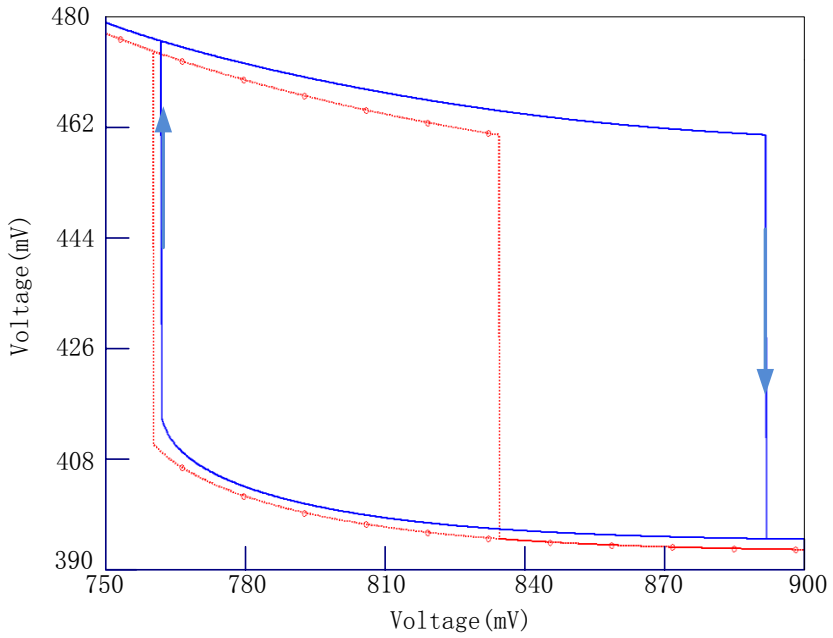
Fig.4.8 (a) Schematic circuit of *Schmitt trigger*, (b) its voltage transfer characteristic


400
360
320
280
240
200
Voltage(mV)
75
90
105
120
135
150
Voltage(mV)

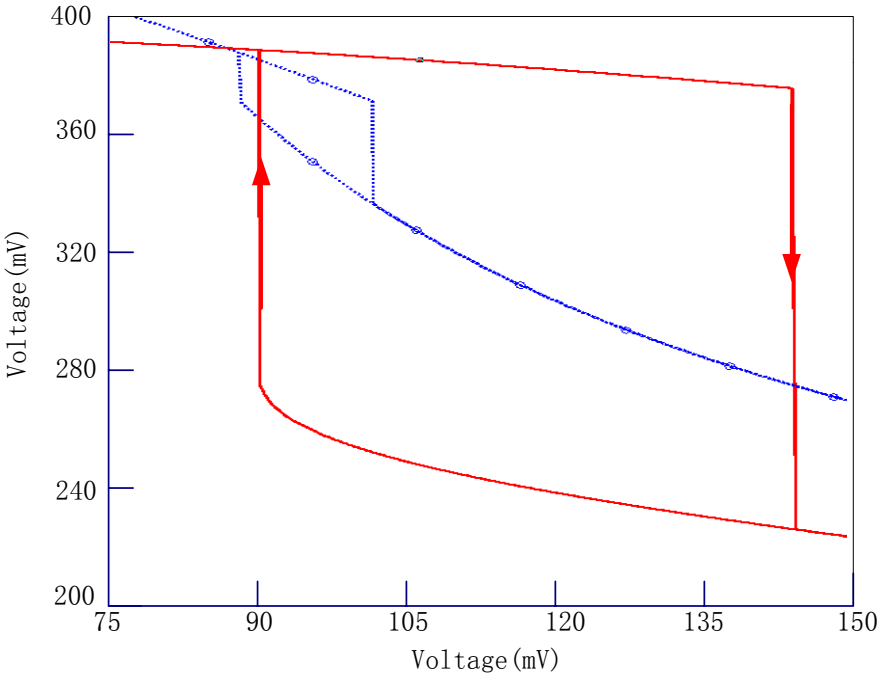
(a)


475
420
365
310
255
200
Voltage(mV)
90
130
170
210
250
290
Voltage(mV)

(b)



(c)



(d)

Fig 4.9 Simulation results of the proposed Schmitt trigger with (a) $C_{j1} = C_{j2} = C_{j4} = 0.1$aF, $C_{j3} = 0.7$aF, $C_{g2} = 0.9$aF, $C_{g1} = 0.5$aF (solid red curve) or 0.9aF (dotted blue curve), (b) $C_{j1} = C_{j2} = C_{j4} = 0.1$aF, $C_{j3} = 0.7$aF, $C_{g1} = 0.55$aF and $C_{g2} = 0.9$aF (solid red curve) or $C_{j3} = 0.2$aF, $C_{g1} = 1.1$aF and $C_{g2} = 1.8$aF (dotted blue curve), (c) $C_{j1\sim j4} = 0.2$aF, $C_{g1} = 1.0$aF, $C_{g2} = 1.8$aF at T = 40K (solid blue curve) and 50K (dotted red one), and (d) $C_{j1} = C_{j2} = C_{j4} = 0.1$aF, $C_{j3} = 0.7$aF $C_{g1} = 0.55$aF $C_{g2} = 0.9$aF at T = 50K (solid red curve) and 100K (dotted blue one)

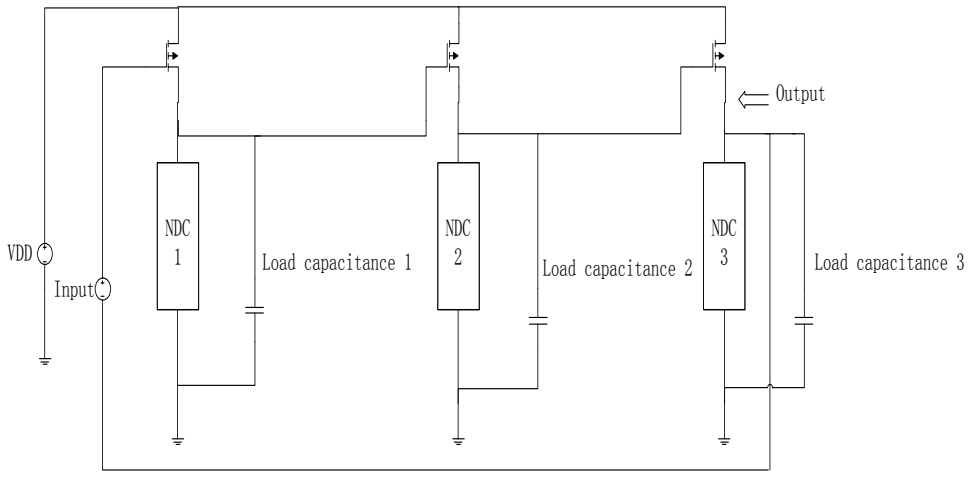
4.4 Oscillator Using NDC Inverter

As a high frequency application, the NDC loaded with a P-MOS constructs a three-stage ring oscillator. The circuit operation is based on the *Schmitt* trigger circuit by the four-junction NDC as an inverter (Fig 4. 10(a)). The parameters for the PMOS are: width =960nm, length =240nm. The supply voltage and load capacitance of each stage are 2V and 1fF, respectively. The output waveform of the ring oscillator shown in Fig 4.10 (b), where the oscillation frequency is given by

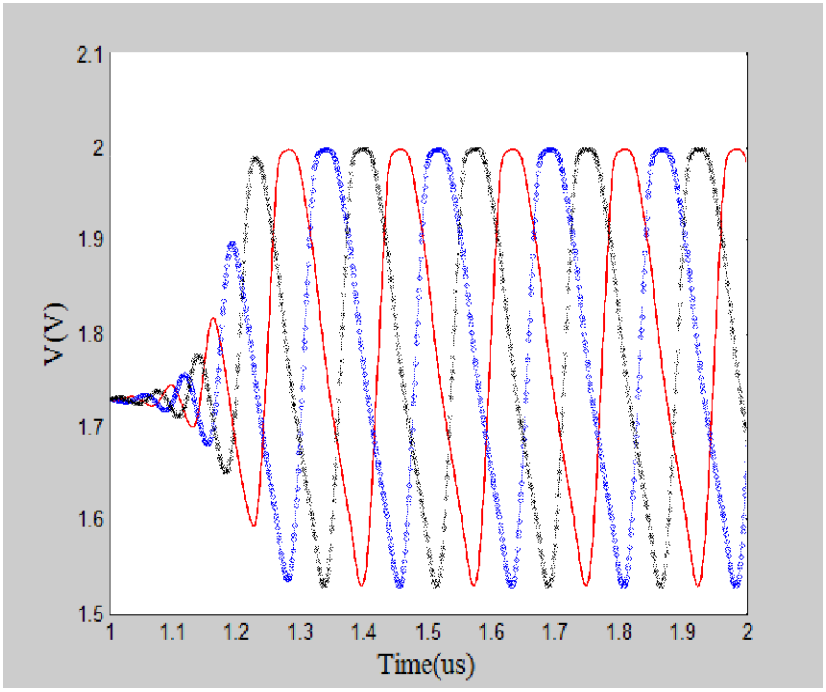
$$f = \frac{1}{2NT_d} \tag{4.1}$$

Where N - Number of stages, T_d - Delay of the design circuit in seconds

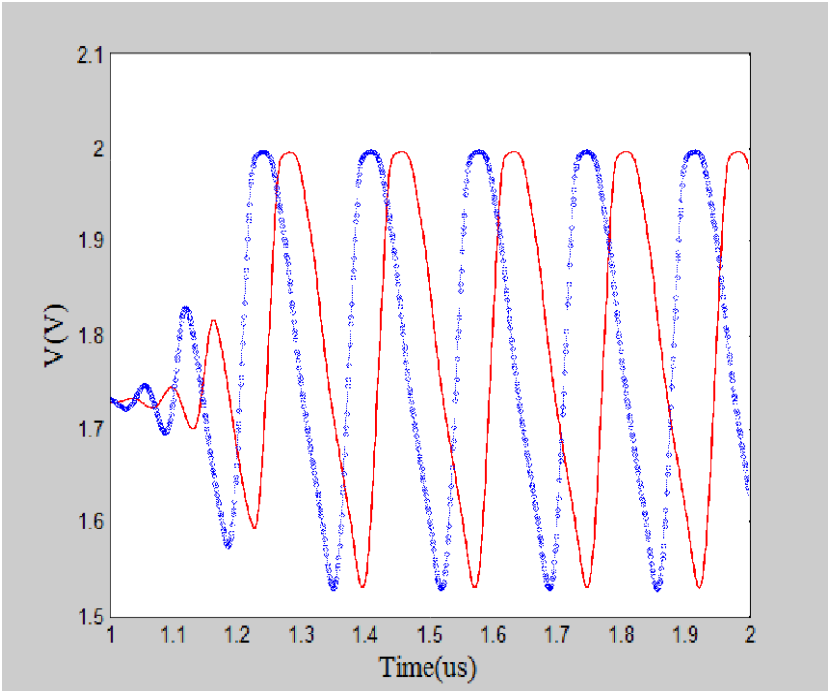
Shifting parameters and increasing temperature will cause change of output waveform's phase showed in Fig 4.10 (c).These changes are not obviously due to the static current of NDC block is operated by various parameters in a narrow range.



(a)



（b）



（c）

Fig 4.10 (a) Schematic circuit of ring oscillator with feedback (b) Output waveform of the proposed oscillator,where the red (solid), blue (circles)and black (stars) correspond to output voltage of first stage, second stage and third stage, respectively (c) phase shifting when temperature is changed.

Chapter 5
An Area-Efficient Ternary Full Adder Using Hybrid SET-MOS Technology

Full adder is one of the most important arithmetic units for many digital applications. A highly efficient and effective design for full adder is crucial for high-performance operation of digital systems. With the single-threshold nature, traditional CMOS devices have been shown to be less area or power-efficient for designing an MVL full adder or ternary full adder in this particular case. With ultra-low power consumption and nanometer size, single-electron transistors with their unique multi-threshold characteristics are instead a promising alternative. The main problems with SET devices are the low current drivability and reliability. Thus, an appropriate and natural solution is to use a hybrid SET-MOS circuit design, having the best of both worlds.

5.1 PREVIOUS WORKS

5.1.1 TFA based on CNTFET

In recent literature, Carbon nanotube field effect transistors (CNTFET) are utilized for the new design methodology which is highly appropriate for MVL logic. Its various properties, such as low-off current, unique 1-D band structure, are the attractive features for circuit designers. And P and N type CNTFET have same size and mobility, different from CMOS, which can simplify the structure for integrated circuit. The

main drawback of this circuit is that it utilizes a larger number of transistors [2] [12] [13] [14]. Figure 5.1 shows schematic diagram of Proposed CNTFET-based TFA cell.

5.1.2 TFA using the Ternary Adiabatic Logic (TAL)

Another logic which can be used for full adder circuit is Adiabatic Logic that attempts to reduce the power consumption of a circuit by operating it both slowly and reversibly. A number of Adiabatic Logic families have been proposed. They are including 2N2P, PAL, CAL, TSEL, and SCAL. The binary logic has been dominated majority of adiabatic logic families, but Ternary Adiabatic Logic can be considered to be the ternary derivative for binary Adiabatic Logic [12].

5.2 SET-MOS Literal Gate

Research shows that literal gates are a fundamental block to build an MVL system. Conventional literal gates are complex and hard to design. However, when implemented using SET-MOS technology, a literal gate can be constructed in a compact structure using an NMOS transistor and a SET transistor. Fig 5.2 shows the basic architecture of a SET-MOS literal gate, where a periodic oscillating of output voltage is realized by applying a drain voltage of the SET transistor to the gate terminal of a current-biased MOSFET. The width and height of the output voltage waveform can be adjusted by the current source, voltage on second gate and its oscillation frequency. By selecting circuit

parameters of Fig 5.2, one can implement some basic ternary logic functions. In particular, a literal gate that produces logic "1" at the output if and only if the input is logic "*i* "(*i* = 0, 1 or 2) is denoted by X^i (refer to Fig 5.2 (b)).

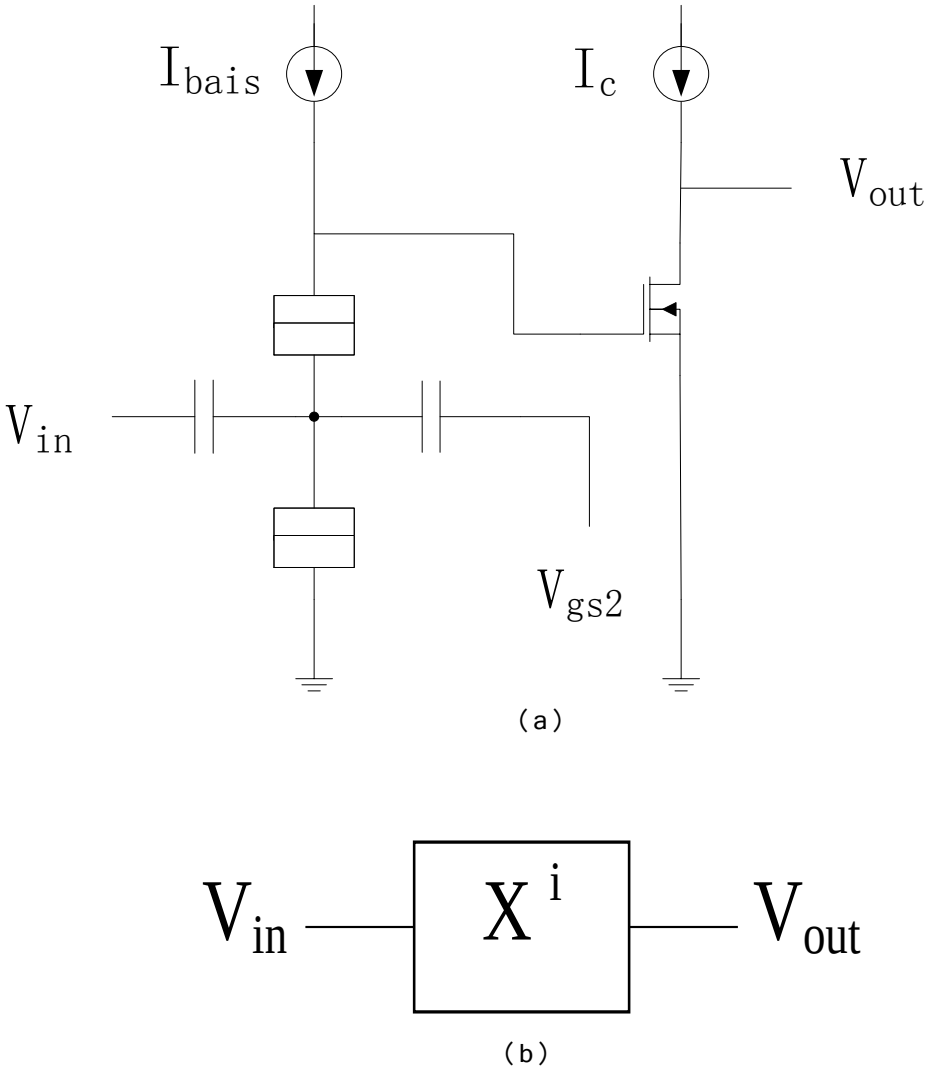
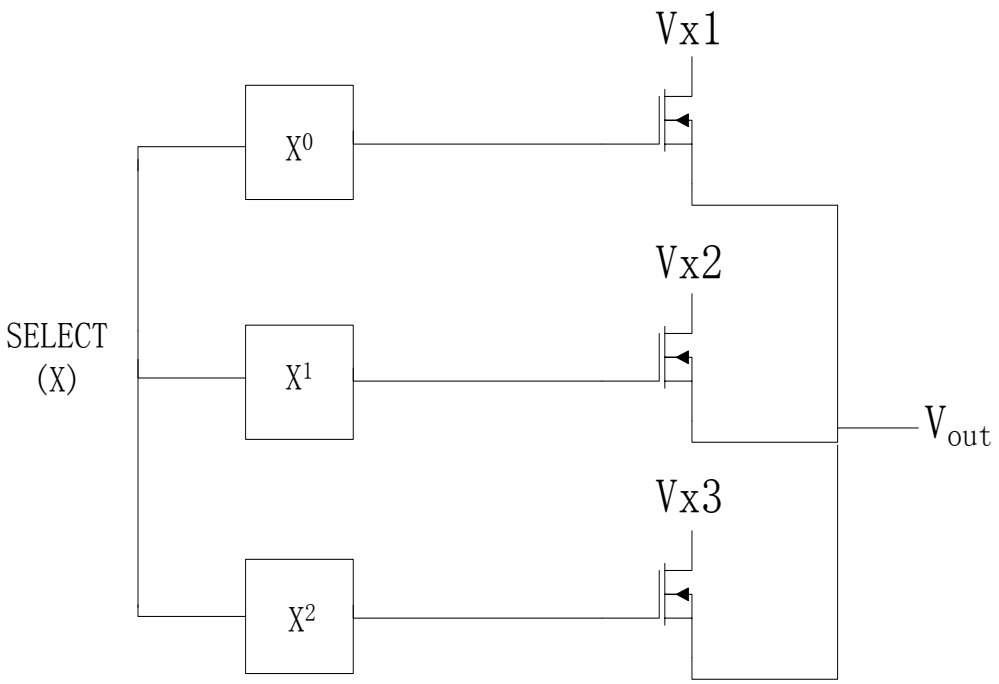


Fig 5.1 (a) A SET-MOS literal gate, and (b) its circuit symbol where V_{out} = "1" if and only if V_{in} = "*i*" (*i* = 0, 1, or 2).

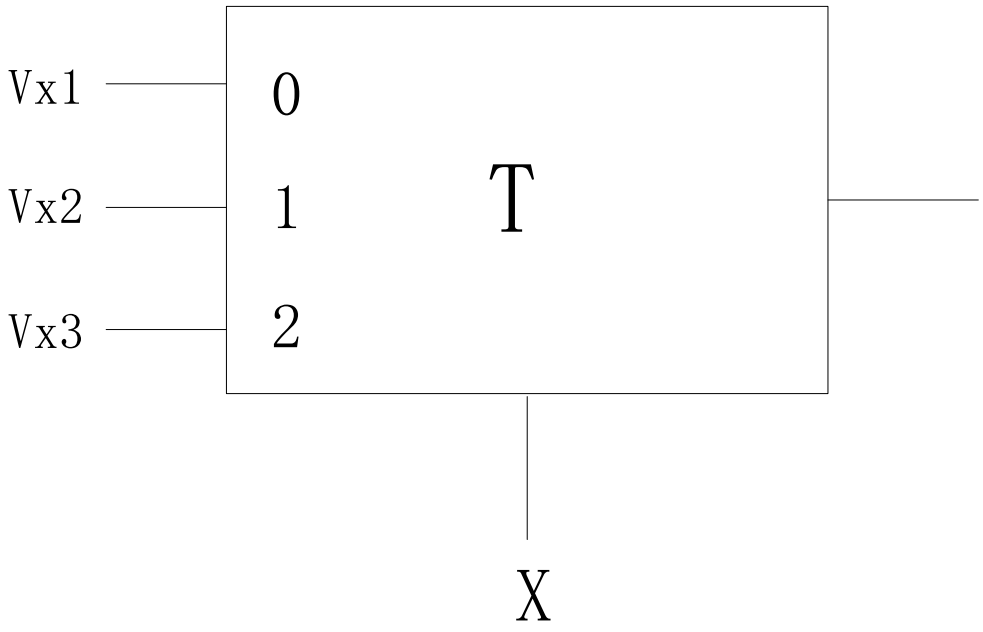
5.3 T-Gate

Similar to multiplexors in binary logic, transmission gate (or T-gate) is another

important building block for MVL design since it can be utilized to implement a variety of logic functions. The schematic of a SET-MOS based T-gate and its circuit symbol are shown in Fig 5.2, where X^i (i = 0, 1, or 2) is a literal gate, X is the input signal, and V_{xi} is a specific ternary logic value depending on the required logic function. Examples of ternary functions that can be implemented by the T-gate are shown in Table 5.1 For instance, the successor function $\vec{x}$ is implemented by choosing V_{x0} = "1', V_{x1} = "2", and V_{x2} = "0" in Fig 5.3.



(a)



(b)

Fig 5.2 (a) Schematic of a SET-MOS ternary T-gate, and (b) its circuit symbol, where $V_{out} = V_{xi}$ if $X =$ "i" (i = 0, 1, or 2)

Function name	**Notation**	**Function output for X = (0, 1, 2)**
identity	X	(0, 1, 2)
complement	$\bar{X}$	(2, 1, 0)
successor	$\vec{X}$	(1, 2, 0)
predecessor	$\overleftarrow{X}$	(2, 0, 1)

Table 5.1 Examples of ternary functions using T-gate

5.4 Proposed TFA

The proposed TFA is shown in Fig 5.3, which takes two ternary inputs *A* and *B* as well as a carry-in signal C_{in}, and generates the sum output *SUM* and carry-out C_{out}. The *SUM* generator contains T-gates that are controlled by *A*, *B* and C_{in}, while the C_{out} generator includes three literal gates plus a binary two-input binary NAND gate and inverter (note: For this ternary logic, both C_{in} and C_{out} have only two possible logic values of 0 and 1). In this work, the supply voltage (V_{dd}) is biased at 0.7 V (unless otherwise specified), and the ternary logic has three voltage levels of 0V (logic "0"), V_{dd} /2 (logic "1"), and V_{dd} (logic "2"). The total number of transistors in Fig 5.3 is 57 only.

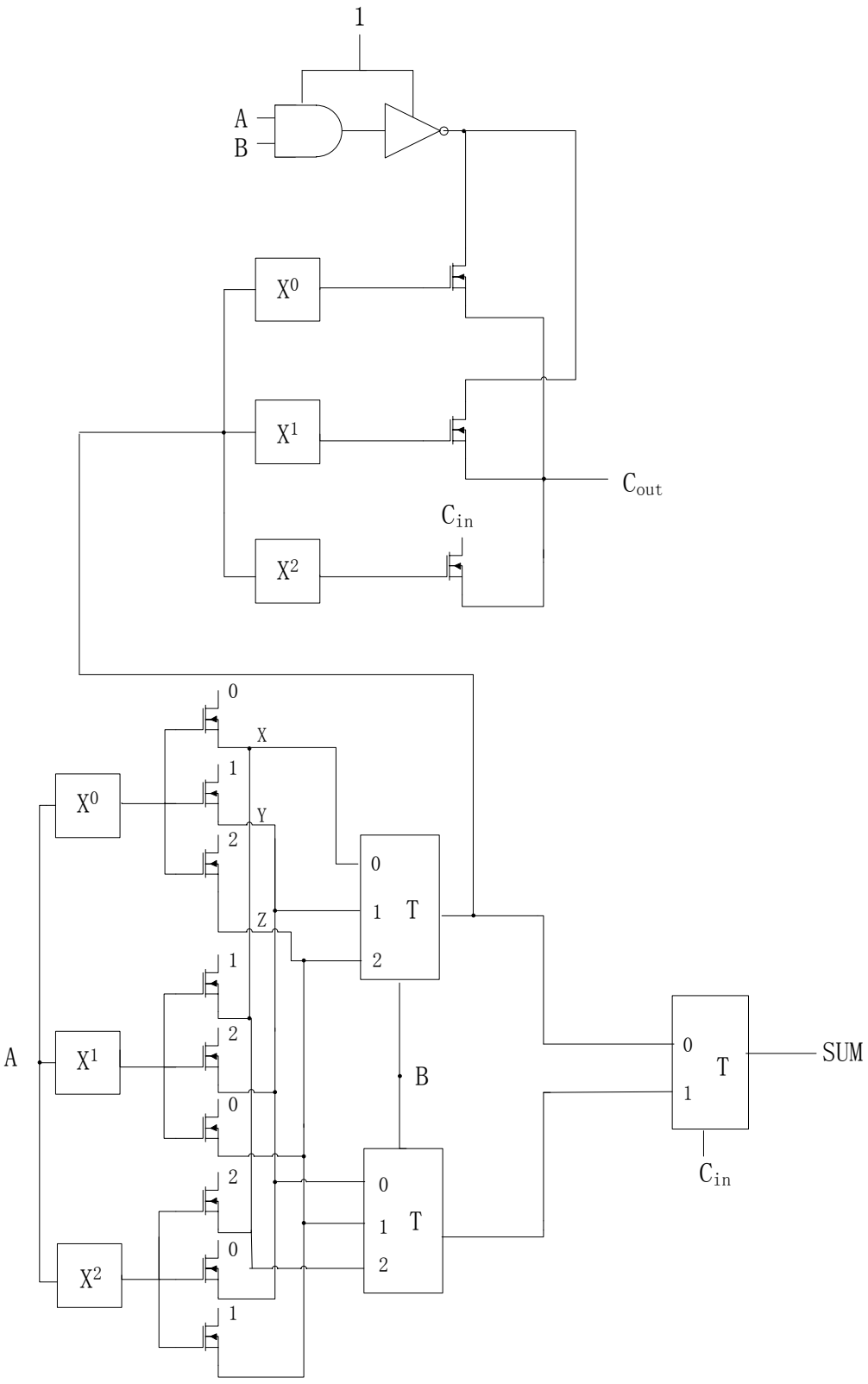


Fig 5.3 Schematic of the proposed ternary full adder

5.5 Simulation Results with Discussions

Simulation was done using Cadence Spectre simulator with 180nnm CMOS model and SET MIB macro mode to estimate the performance of the proposed TFA under various conditions. The results of recently published CNTFET-based TFA cells were also taken for performance comparison. The power supply voltage of 0.7V was used (unless otherwise stated) throughout our simulations which consider different temperatures and operating frequencies.

A complete set of input signals (including all 18 possible input combinations) was applied to the proposed TFA. The performance evaluations were focused on its power, delay and power-delay product (PDP). The average power consumption is measured as

$$P_{average} = \int_0^T V(t) * I(t)dt \quad (5.1)$$

Where *V* is the power supply, *I* (t) is the total current drawn from the power supply, and *T is* the simulation time interval.

The PDP is calculated as

$$PDP = Max\ (Delay) \times P_{average} \quad (5.2)$$

Fig 5.4 shows the simulated results of the proposed TFA, which verifies its correct operation. Our simulation results also show that the proposed TFA has a lower PDP than most CNTFET-based TFA especially when operated at higher frequency, but may still

consume more power than other implementations. Fig 5.5 shows part of these results in comparison with [14] and [16].

The proposed TFA takes advantage of the unique oscillation characteristics of SET transistors, which contribute to an area-efficient design. This can be seen from Table 5.2 where the transistor counts in different TFA are listed. The proposed TFA needs only 57 transistors, a number much less than all those reported in literature so far.

Simulation results on the temperature effect for the proposed TFA are shown in Fig5.6. As expected, the power consumption decreases with the rising temperature due to the performance degradation of MOS transistors. It can also be seen that the delay of TFA improves as the temperature increases. This is mainly due to the fact that the static current of SET transistors goes up with the temperature.

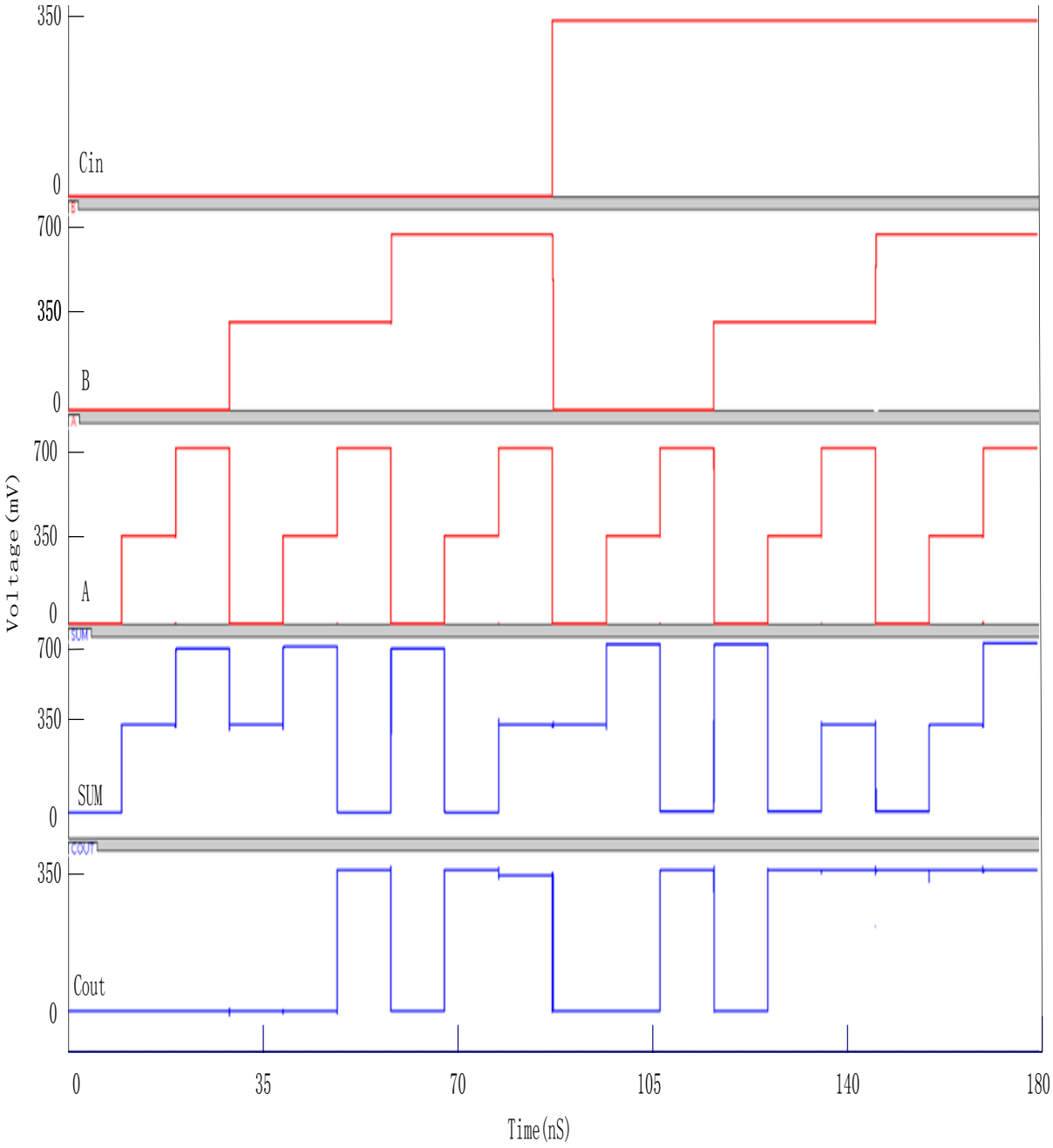
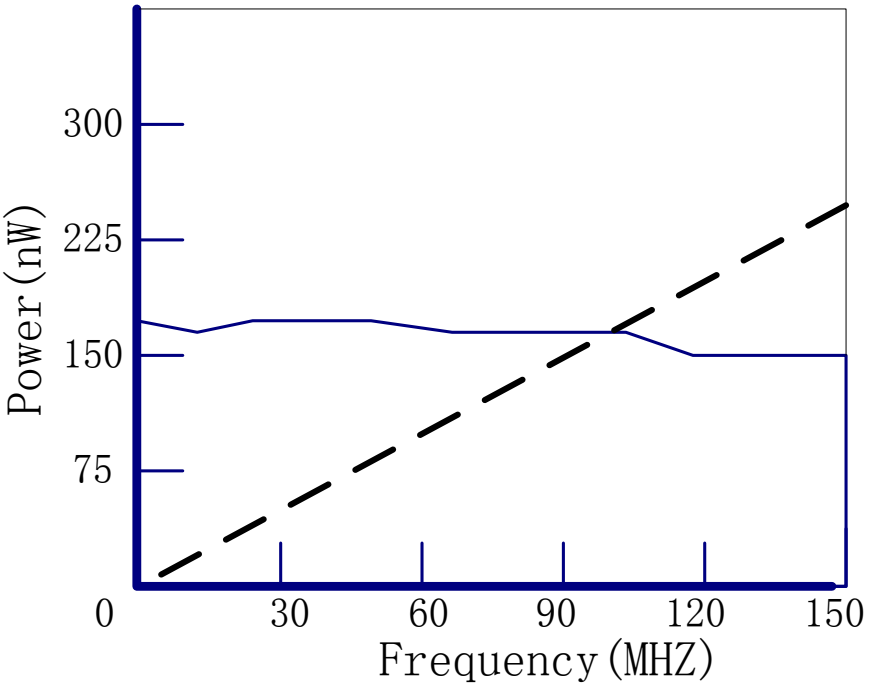
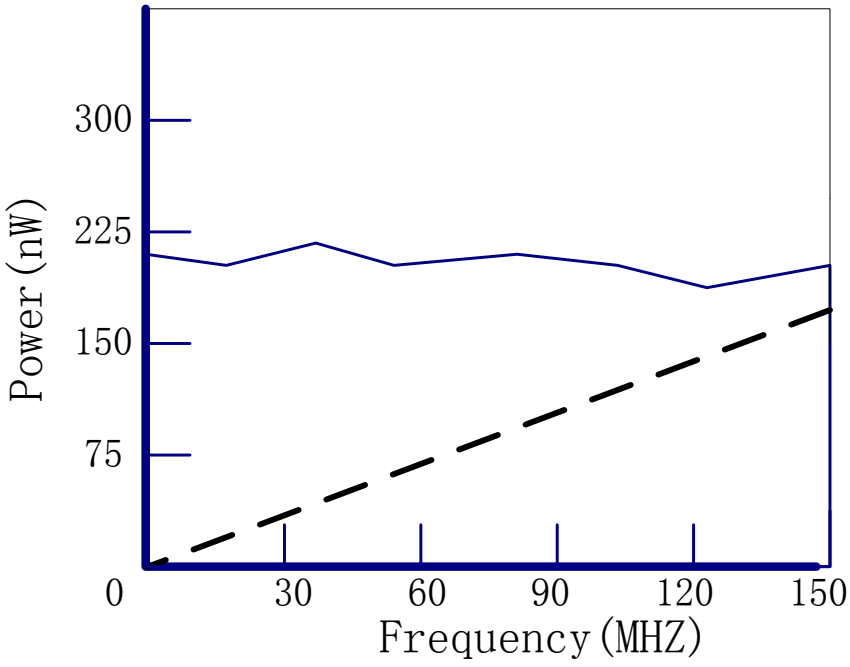


Fig 5.4 Simulation results of the proposed TFA.



(a)

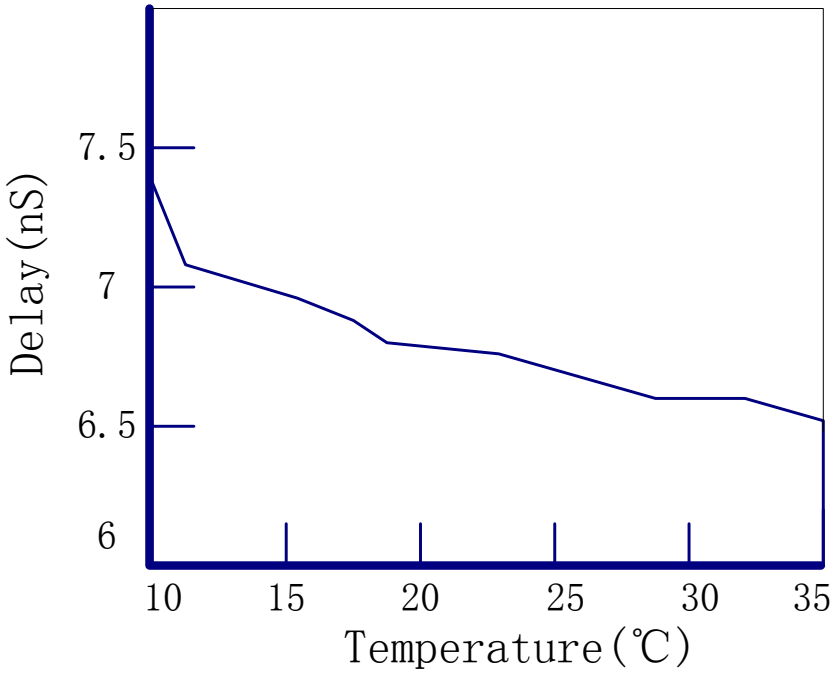


(b)

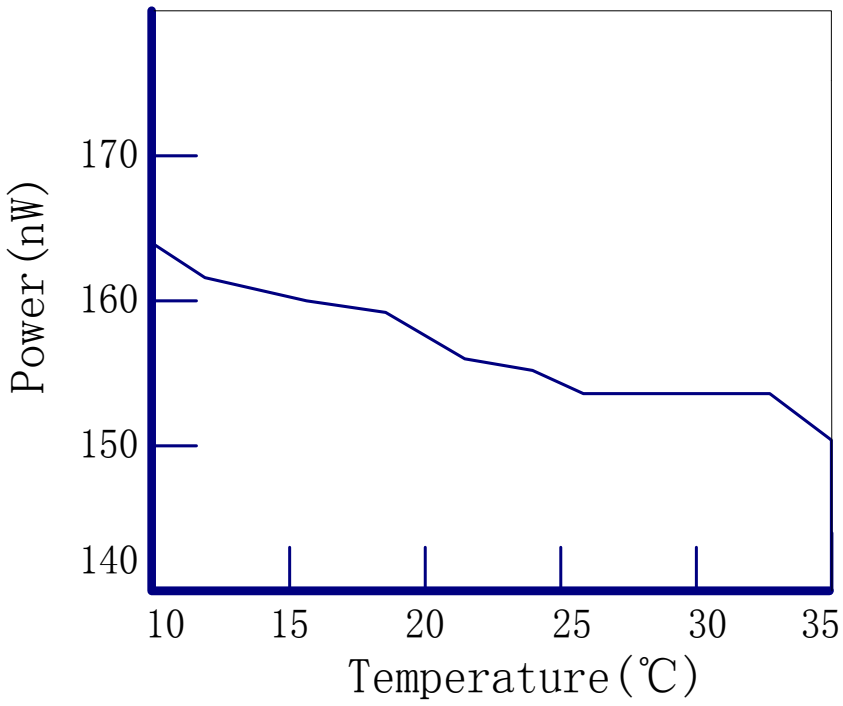
Fig 5.5 the average power vs frequency of (a) the proposed TFA (solid curve with V_{dd} = 0.7V) in comparison with [14] and (b) the proposed TFA (solid curve with V_{dd} = 0.9V) in comparison with [16].

TFA	Type of transistors	# transistors
The proposed	SET and CMOS	57
[18]	CNTFET	106
[19]	CNTFET	142
[20]	CNTFET	214

Table 5.2 Comparison of transistor counts required for TFA



(a)



(b)

Fig 5.6 (a) Delay vs. temperature, (b) power vs. temperature for the proposed TFA

Chapter 6
Conclusion and Future Work

6.1 Conclusion

We have presented a piece-wise model for multiple-peak SET-based NDC blocks with considerations of temperature effects. The model describes the NDC's I-V characteristic in terms of input voltage and circuit parameters, making it very useful for optimization design of NDC application circuits. After the new four-junction NDC block has been modeled, we applied it to implement multiple-valued memory cell and *Schmitt* trigger. With the analytical model, circuit parameters can be adjusted to analyze their impacts on circuit performance for potential optimization design with different applications of NDC blocks. Finally, we have proposed a novel design of ternary full adder based on hybrid SET-MOS technology. By taking advantage of unique *Coulomb* oscillations with SET transistors, the proposed circuit structure promises to be more area- and/or power-efficient than most existing TFA cells. This has been fully supported by extensive simulations with *Cadence* tools.

6.2 Future work

The background charge and temperature effect on SET circuit should be solved in the future. We try to address the reliability issues with the lowest power consumption and delay.

In chapter 5, we present a novel design of ternary full adder using hybrid single-electron transistor and MOS technology. More work should be done in reducing transistor number and optimizing the structure. And a ternary multiplier can be design using this TFA.

References

[1] H. Inokawa, A. Fujiwara, and Y. Takahashi, "A Multiple-Valued Logic and Memory with Combined Single-Electron and Metal-OxideSemiconductor Transistors," IEEE Trans. Electron Devices, vol. 50, February 2003.

[2] C. P. Heij, et al., “Negative differential resistance due to single-electronswitching,” Appl. Phys. Lett., vol. 74, pp. 1042–1044, 1999.

[3] S. Mahapatra and A. M. Ionescu, “A novel single electron SRAM architecture,” Proc. of IEEE-Nano 2004, vol. 3, pp. 287–289.

[4] K. Akarvardar, et al., “Four-gate transistor voltage-controlled negative differential resistance device and related circuit applications,” 2006 IEEE International SOI Conference, pp. 87-88.

[5] B. H. Lee and Y. H. Jeong, “A novel SET/MOSFET hybrid static memory cell design,” IEEE Trans. Nanotechnology, pp. 377-382, 2004.

[6] N. Syed and C. Chen, “Low-power multiple-valued SRAM logic cells using single-electron devices,” IEEE International Conference on Nanotechnology, pp. 1174-1177, 2012.

[7] C. Wasshuber, H. Kosina, and S. Selberherr, “SIMON—A simulator for single-electron tunnel devices and circuits,” IEEE Trans. Computer- Aided Design, vol. 16, pp. 937–944, Sept. 1997.

[8] M. T. Bohr, “Nanotechnology goals and challenges for electronic applications,” IEEE Trans. On Nanotechnology, vol. 1, no. 1, March 2002, pp. 56-62.

[9] K. Likharev, “Single-electron devices and their applications”, Proceedings of the IEEE, vol. 87, no. 4, April 1999, pp. 606-632.

[10] S. M. Goodnick and J. Bird, “Quantum-effect and single-electron devices,” IEEE Trans. on Nanotechnology, vol. 2, no. 4, December 2003, pp. 368-385.

[11] H. Suwa. “Geometrically Constructed Markov Chain Monte Carlo Study of Quantum Spin-Phonon Complex Systems”. 2014, Springer, pp. 11-42.

[12] D. J. Willingham and I. Kale, “A ternary adiabatic logic (TAL) implementation of a four-bit full adder,” NORCHIP, pp.1-4, 2011.

[13] S. Mahapatra and A. M. Ionescu. Hybrid CMOS single-electron-transistor device and circuit design. Artech House, 2006.

[14] K. Navi, M. H. Moaiyeri, R. F. Mirzaee, O. Hashemipour, and B. M. Nezhad, “Two new low-power full adders based on majority-not gates,” Microelectronics Journal of Elsevier, vol. 40, no. 1, pp.126–130, January 2009.

[15] S. L. Murotiya and A. Gupta, “Design of CNTFET based 2-bit ternary ALU for nanoelectronics,” International Journal of Electronics, vol. 101, no. 9, pp. 1244-1257, 2014.

[16] S. A. Ebrahimi, P. Keshavarzian, S. Sorouri, and M. Shahsavari, “Low power CNTFET-based ternary full adder cell for nanoelectronics,” International Journal of Soft Computing and Engineering, vol. 2, no. 2, pp. 291-295, May 2012.

[17] Moore, Gordon (2006). "Chapter 7: Moore's law at 40". In Brock, David. *Understanding Moore's Law: Four Decades of Innovation* (PDF). Chemical

Heritage Foundation. pp. 67–84. *ISBN 0-941901-41-6. Retrieved March 15, 2015*.

[18] S. A. Ebrahimi, P. Keshavarzian, S. Sorouri, and M. Shahsavari, "Low power CNTFET-based ternary full adder cell for nanoelectronics," *International Journal of Soft Computing and Engineering*, vol. 2, no. 2, pp. 291-295, May 2012.

[19] K. Sridharan, S. Gurindagunta, and V. Pudi, "Efficient multiternary digit adder design in CNTFET technology," *IEEE Trans. on Nanotechnology*, vol. 12, no. 3, pp. 283-287,May 2013.

[20] S. L. Murotiya and A. Gupta, "Design of CNTFET based 2-bit ternary ALU for nanoelectronics," *International Journal of Electronics*, vol. 101, no. 9, pp. 1244-1257, 2014.

Appendix A:

Code of four junctions NDC:

MATLAB:

M-file main:

```
VDS=0:0.01:1;
%VJ=0;0.01;1;
ID1=zeros(1,101);
ID2=zeros(1,101);
for j=1:101
       V1=VDS(j);
       Icalculate;
     ID1(j)=I;
     %ID2(102-j)=I
      %VJ(j)=Vj2;
end
%plot(VJ,ID,'g')
%hold on
  plot(VDS,ID1,'r')
  hold on
axis([0.3 1 0 1.5e-8])
```

```
xlabel('V(Volt)')

ylabel('I(A)')


hold on
```

M-file Icalculate:

```
e=1.6e-19;

cj=1e-19;

cp=7e-19;

cg1=5*cj;

cg2=15*cj;

c=[cj+cg1 -cj 0 -cg1 0 -cj 2*cj+cg2 -cj 0 -cg2 0 -cj cp+cj -cp 0 -cg1 0 -cp cj+cp+cg1 -cj 0

-cg2 0 -cj cj+cg2];

C1=reshape(c,5,5);

Ce1=cg2+[(cp*cj)/(cp+cj)]*(cj+cg1)/(cg1+[(cp*cj)/(cp+cj)]+cj);

Ce2=(cg1+cj)*cp/(cg1+cj+cp)+(cg2+cj)*cj/(cg2+cj+cj);

Ce3=Ce2;

Ce4=cg1+[(cp*cj)/(cp+cj)]*(cj+cg2)/(cg2+[(cp*cj)/(cp+cj)]+cj);

Vc1=e/2/(cj+Ce1);

Vc2=e/2/(Ce2);

Vc3=e/2/(Ce3);
```

```
Vc4=e/2/(cj+Ce4);

Vc=[Vc1 Vc2 Vc3 Vc4];

T=0;

kb=1.38e-23;

VT=kb*T/e;

Rt=1e6;

rate1=0;

rate2=0;

rate3=0;

rate4=0;

rate1p=0;

rate4p=0;

q3=0;

q2=ceil((-cj*V1+(2*cj+cg2)*(V1-Vc1)-cj*[(V1-Vc1)-Vc2])/e);

%q2=ceil(((2*[4*cj^2+3*cj*(cg1+cg2)+2*cg1*cg2]-6*cj*(cj+cg1))*V1-Vc1*2*[4*cj^2

+3*cj*(cg1+cg2)+2*cg1*cg2])/2/(3*cj+2*cg1)/e)

q2=q2*e;

V2=V1-Vc1;

%V2=[6*cj*(cj+cg1)*V1+(3*cj+2*cg1)*(2*q2+q3)+cj*(q3)]/2/[4*cj^2+3*cj*(cg1+cg2)

+2*cg1*cg2];

V3=[(V1-Vc1)-Vc2];
```

```
%q3=(-cj*(V1-Vc1)+2*cj*[(V1-Vc1)-Vc2]-cj*(V3-Vc3))

V4=V3-Vc3;

q4=floor((-cg1*V1-cp*V3+(cj+cp+cg1)*V4)/e);

%q4=floor((Vc4*(3*cj+2*cg1)-2*cg1*V1-cj*V2)/2/e)

q4=q4*e;

q=[q2 q3 q4];




i=5;

while(i>0)

[Vj1,Vj2,Vj3,Vj4]=Vcalculate(V1,q2,q3,q4);

VJ=[Vj1,Vj2,Vj3,Vj4]

E=VJ-Vc;

[ma,W]=max(E);

if(T~=0&W==3)

      W=2;

end

if(T==0)

if (ma<=0)
```

```
  I=0;
else;
E=VJ-Vc;
MT=find(E>0);
W=MT(1,1);
end
end
if(W==1)
rate1=(Vj1-Vc1)/(e*Rt*(1-exp(-(Vj1-Vc1)/VT)))
                    q2=q2+e;
[Vj1,Vj2,Vj3,Vj4]=Vcalculate(V1,q2,q3,q4);
VJ =[Vj1,Vj2,Vj3,Vj4]
E=VJ-Vc;
[ma,W]=max(E);
if (ma>=0)
E=VJ-Vc;
MT=find(E>0);
W=MT(1,1);
end
q=[q2/e q3/e q4/e];
end
```

```
if(W==2)
rate2=(Vj2-Vc2)/(e*Rt*(1-exp(-(Vj2-Vc2)/VT)))
q2=q2-e;
q3=q3+e;
[Vj1,Vj2,Vj3,Vj4]=Vcalculate(V1,q2,q3,q4);
VJ =[Vj1,Vj2,Vj3,Vj4]
E=VJ-Vc;
[ma,W]=max(E);
MT=find(E>=ma);
W=MT(1,1);
q=[q2/e q3/e q4/e];
end
  if(W==3)
rate3=(Vj3-Vc3)/(e*Rt*(1-exp(-(Vj3-Vc3)/VT)))
q3=q3-e;
q4=q4+e;
[Vj1,Vj2,Vj3,Vj4]=Vcalculate(V1,q2,q3,q4);
VJ =[Vj1,Vj2,Vj3,Vj4]
E=VJ-Vc;
  [ma,W]=max(E);
    MT=find(E>=ma);
```

```
W=MT(1,1);

q=[q2/e q3/e q4/e];

end

if(W==4)




rate4p=(Vj4-Vc4)/(e*Rt*(1-exp(-(Vj4-Vc4)/VT)))

q3=q3-e;

q4=q4+e;

[Vj1,Vj2,Vj3,Vj4]=Vcalculate(V1,q2,q3,q4);

VJ=[Vj1,Vj2,Vj3,Vj4];

E=VJ-Vc;

[ma,W]=max(E);



q=[q2/e q3/e q4/e];

end

i=i-1;

end
```

```
%rate2=rate2*2;

if(rate4p~=0)

w1=1/rate1/(1/rate1+(rate1p+rate4)/rate2/rate4+(rate1p+rate4)/rate3/rate4+1/rate4+rate1p
/rate4p/rate4);

w1=1/rate1/(1/rate1+(rate1p+rate4)/rate2/rate4+(rate1p+rate4)/rate3/rate4+1/rate4+rate1p
/rate4p/rate4);
else
    w1=1/rate1/(1/rate1+(rate1p+rate4)/rate2/rate4+(rate1p+rate4)/rate3/rate4+1/rate4);
end
w3=(rate1p+rate4)*rate1/rate3/rate4*w1;
w5=rate1p*rate1/rate4p/rate4*w1;
w4=rate1/rate4*w1;
w2=1-(w1+w3+w4+w5);
I2=rate2*w2*e;
I4=(w5*rate4p+w4*rate4)*e;
I3=rate3*w3*e;
```

```
I1=(w1*rate1+w4*rate1p)*e;

I=I2

if(prod([rate1,rate2,rate3,rate4])==0)

    I=0;

end

if(V1>sum([Vc1,Vc2,Vc3,Vc4]))

    I=V1/4/Rt;

end
```

M-file Vcalculate:

```
function [Vj1,Vj2,Vj3,Vj4]=Vcaluate(V1,Cj,Cg1,Cg2,q2,q3,q4)


V2=[6*Cj*(Cj+Cg1)*V1+(3*Cj+2*Cg1)*(2*q2+q3)+Cj*(q3+2*q4)]/2/[4*Cj^2+3*Cj*(
Cg1+Cg2)+2*Cg1*Cg2];

V3=-V1+(2*Cj+Cg2)/Cj*V2-q2/Cj;

V4=(2*Cg1*V1+Cj*V2+q3+2*q4)/(3*Cj+2*Cg1);


Vj1=V1-V2;

Vj2=V2-V3;

Vj3=V3-V4;

Vj4=V4;

End
```

Verilog:

```
// VerilogA model for NDC cell



`include "discipline.h"
`include "constants.h"



module NDC(drain,source);

        inout drain,source;
        electrical drain,source;

////////////////////////////////////////
        analog function real Vj1Cal;
                input V1,Cj,Cg1,Cg2,q2,q3,q4;
                real V1,Cj,Cg1,Cg2,q2,q3,q4,V2;

                        begin

    V2=(6*Cj*(Cj+Cg1)*V1+(3*Cj+2*Cg1)*(2*q2+q3)+Cj*(q3+2*q4))/2/(4*Cj*Cj+3*
```

```
Cj*(Cg1+Cg2)+2*Cg1*Cg2);

        Vj1Cal=V1-V2;

                end

    endfunction

////////////////////////////////////////

    analog function real Vj2Cal;

        input V1,Cj,Cg1,Cg2,q2,q3,q4;

        real V1,Cj,Cg1,Cg2,q2,q3,q4,V2,V3;

                begin

  V2=(6*Cj*(Cj+Cg1)*V1+(3*Cj+2*Cg1)*(2*q2+q3)+Cj*(q3+2*q4))/2/(4*Cj*Cj+3*
Cj*(Cg1+Cg2)+2*Cg1*Cg2);
        V3=-V1+(2*Cj+Cg2)/Cj*V2-q2/Cj;

        Vj2Cal=V2-V3;

                end
```

```
        endfunction

////////////////////////////////////////////

analog function real Vj3Cal;
                input V1,Cj,Cg1,Cg2,q2,q3,q4;
                real V1,Cj,Cg1,Cg2,q2,q3,q4,V2,V3,V4;

                        begin

    V2=(6*Cj*(Cj+Cg1)*V1+(3*Cj+2*Cg1)*(2*q2+q3)+Cj*(q3+2*q4))/2/(4*Cj*Cj+3*
Cj*(Cg1+Cg2)+2*Cg1*Cg2);
                V3=-V1+(2*Cj+Cg2)/Cj*V2-q2/Cj;
                V4=(2*Cg1*V1+Cj*V2+q3+2*q4)/(3*Cj+2*Cg1);

                Vj3Cal=V3-V4;
                        end
        endfunction

////////////////////////////////////////////
```

```
analog function real Vj4Cal;
                input V1,Cj,Cg1,Cg2,q2,q3,q4;
                real V1,Cj,Cg1,Cg2,q2,q3,q4,V2,V3,V4;

                        begin

    V2=(6*Cj*(Cj+Cg1)*V1+(3*Cj+2*Cg1)*(2*q2+q3)+Cj*(q3+2*q4))/2/(4*Cj*Cj+3*
Cj*(Cg1+Cg2)+2*Cg1*Cg2);
                V3=-V1+(2*Cj+Cg2)/Cj*V2-q2/Cj;
                Vj4Cal=(2*Cg1*V1+Cj*V2+q3+2*q4)/(3*Cj+2*Cg1);
                        end
        endfunction

////////////////////////////////////////
////////////////////////////////////////

        parameter real Cj = 1e-19;
        parameter real Cg1 = 5e-18;
        parameter real Cg2 = 15e-19;
        parameter real Rt = 1e6;
        parameter real T = 0;
```

```
        real VT,Vj1,Vj2,Vj3,Vj4,V1,V2;
        real e,q2,q3,q4;
        real rate1,rate1p,rate2,rate3,rate4,rate4p;
        real Vc1,Vc2,Vc3,Vc4;
        real w1,w2,w3,w4,w5;
        real Ids;

////////////////////////////////////////
////////////////////////////////////////
        analog
                begin
e=`P_Q;
VT = T*`P_K/e;
V1 = V(drain,source);

q3=0;
Vc1=e/2/(Cj+Cg2+0.5*Cj*(Cj+Cg1)/(Cg1+1.5*Cj));
Vc2=e/2/(Cj+(Cg1+Cj)*(Cg2+Cj)/(Cg1+Cj+Cg2+Cj)*Cj/(Cj+(Cg1+Cj)*(Cg2+Cj)/(Cg1
```

```
+Cj+Cg2+Cj)));

Vc3=Vc2;

Vc4=e/2/(Cj+Cg1+0.5*Cj*(Cj+Cg2)/(Cg2+1.5*Cj));


//////////////////////////////////////////


q2=ceil(((2*{4*Cj*Cj+3*Cj*(Cg1+Cg2)+2*Cg1*Cg2}-6*Cj*(Cj+Cg1))*V1-Vc1*2*{4*
Cj*Cj+3*Cj*(Cg1+Cg2)+2*Cg1*Cg2})/2/(3*Cj+2*Cg1)/e);

q2=q2*e;


V2={6*Cj*(Cj+Cg1)*V1+(3*Cj+2*Cg1)*(2*q2+q3)+Cj*(q3)}/2/{4*Cj*Cj+3*Cj*(Cg1+
Cg2)+2*Cg1*Cg2};


q4=floor((Vc4*(3*Cj+2*Cg1)-2*Cg1*V1-Cj*V2)/2/e);

q4=q4*e;


//////////////////////////////////////////


rate1=0;

rate2=0;

rate3=0;
```

```
rate4=0;

rate1p=0;

rate4p=0;


////////////////////////////////////////////////////////////////////////////////

/////////{1st}


Vj1=Vj1Cal(V1,Cj,Cg1,Cg2,q2,q3,q4);

Vj2=Vj2Cal(V1,Cj,Cg1,Cg2,q2,q3,q4);

Vj3=Vj3Cal(V1,Cj,Cg1,Cg2,q2,q3,q4);

Vj4=Vj4Cal(V1,Cj,Cg1,Cg2,q2,q3,q4);


if(Vj1-Vc1<0&&Vj2-Vc2<0&&Vj3-Vc3<0&&Vj4-Vc4<0)

Ids=0;


if(Vj1-Vc1>0&&Vj2-Vc2<0&&Vj3-Vc3<0&&Vj4-Vc4<0)

begin

rate1=(Vj1-Vc1)/(e*Rt*(1-exp(-(Vj1-Vc1)/VT)));

q2=q2+e;

if(Vj1-Vc1<0&&Vj2-Vc2<0&&Vj3-Vc3<0&&Vj4-Vc4>0)
```

Permission to Use Previously Published /Submitted Papers

Dr. Chunhong Chen gives permission to Lin Li to include the following papers into his Master‘s thesis.

1) Paper accepted in oral session for ―Proceedings of 2015 IEEE International Conference on Nanotechnology (IEEE-Nano'15), July 2015, Roma, Italy

Entitled:

L. Li and C. Chen, “An analytical model for NDC blocks with single-electron tunneling,” in *Proceedings of the IEEE International Conference on Nanotechnology*, July 2015, pp. 448-451.

2) Paper to be submitted for publication

Entitled:

L. Li and C. Chen,” Modeling and Application for Negative-Differential-Conductance Devices with Single-Electron Technology”

L. Li and C. Chen, ” An Area-Efficient Ternary Full Adder Using Hybrid SET-MOS Technology”

Sincerely,

Dr. Chunhong Chen

Vita Auctoris

Lin Li was born in 1988 in Beijing, China. He completed him Bachelors of Science degree from the Century College, Beijing University of Posts and Telecommunications in 2011. His research interests include multiple-valued cells using single-electron devices. He is currently a candidate for the Master's degree in Electrical and Computer Engineering at the University of Windsor and hopes to graduate in winter 2016.