1-10-2024

DC-Link Capacitor State-of-Health (SOH) Monitoring and Lifetime Extension for EV Applications

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By

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A Thesis
Submitted to the Faculty of Graduate Studies
through the Department of Electrical & Computer Engineering
in Partial Fulfillment of the Requirements for
the Degree of Master of Applied Science
at the University of Windsor

Windsor, Ontario, Canada

2023

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ABSTRACT

Electric vehicles offer the benefit of eliminating tailpipe emissions, which emit greenhouse gases (GHG) into the atmosphere, lead to diminished air quality, and contribute to global warming. Therefore, plenty of research has gone into the development and improvement of EV technologies to create more effective and reliable vehicles in comparison to traditional internal combustion engine (ICE) vehicles. The electric traction drive, or powertrain, is the fundamental system responsible for controlling the output response of the electric motor within an EV.

High efficiency and reliability are extremely desirable traits for the electric drive to extend the range of the EV to reduce driver anxiety, as well as to extend the vehicle's lifetime for a more cost-effective product. Condition monitoring of fragile components allows for the prediction of device failure before it occurs so that catastrophic failure can be avoided, system downtime is reduced, and system reliability can be enhanced. This thesis aims to develop an existing condition monitoring strategy for the most fragile electrical component within the drive, the DC-Link capacitor. The functionality of the DC-Link capacitor is discussed and power loss modelling for the device is presented. A DC-Link capacitor condition monitoring scheme that employs two state-of-health (SOH) determination strategies is presented for improved reliability of the DC-Link capacitor, and overall motor drive system. This scheme features an online degradation calculation method and a quasi-online parameter estimation method for determining the SOH of the device. An analysis of the impact of sensor tolerance, sampling frequency and ambient temperature on parameter estimation accuracy is also performed, and the minimal sampling frequency required for reliable condition monitoring is identified as 50 kHz through simulation and experimental results.

This thesis also proposes a novel LUT based PWM selection strategy with the aim of prolonging the lifetime of the DC-Link capacitor without significantly sacrificing the performance of the permanent magnet synchronous machine (PMSM) drive compared to conventional control methods. The total capacitance degradation over a drive-cycle based analysis is compared under the proposed PWM selection strategy and under conventional space vector PWM control in order to validate the ability of the proposed strategy to extend the lifetime of the DC-Link capacitor. In the simulation study, over a nine load point load profile the degradation of the dc-link capacitor was reduced by 3.994% under the proposed strategy, validating the ability to extend the lifetime of the dc-link capacitor.

DEDICATION

Dedicated to my parents "Doug and Melissa", older brother "Jacob", and younger sister "Makenna".

Thank you so much for your continuous love support and motivation throughout my academic career and life.

I love you all.

ACKNOWLEDGEMENTS

I would like to thank my supervisor, Dr. Narayan Kar, for giving me the opportunity to be a member of the CHARGE Labs and for making me feel like a valued member of the team despite the large size of the lab. Likewise, I would like to thank my co-supervisor Dr. Lakshmi Varaha Iyer for taking me under his wing and encouraging me with his positive, upbeat, and forward-thinking attitude that he brings to the lab every day, and the industry exposure which he presented to me.

I would also like to thoroughly acknowledge my senior work colleagues Philip Korta, Vamsi Krishna Kurramsetty and Dr. Animesh Anik Kundu for providing me with immeasurable amounts of knowledge, skills, support, and guidance. If not for their contributions to my learning experience, I am sure I would not have been able to succeed.

I would like to thank my family, my father Doug, mother Melissa, older brother Jacob and younger sister Makenna for turning me into the person I am today and for always believing in me and supporting my academic and life goals.

I would also like to extend my gratitude to all the valued members of the CHARGE Labs who have come and gone during my time spent here. I would like to thank Eunha Chu for all the behind the scenes work she does to keep the lab running smoothly. I would like to thank the University of Windsor, The Natural Sciences and Engineering Research Council of Canada (NSERC), Canada Research Chair program in Electrified Vehicles, and Magna International among the many other CHARGE Lab sponsors for providing us with the facilities, equipment and funding necessary to carry out meaningful research. I would like to thank Dr. Balasingam and Dr. Biswas for serving on my master's committee and providing meaningful and helpful feedback to allow me to develop a strong thesis.

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LIST OF ABBREVIATIONS

Abbreviation	Explanation
PMSM	: Permanent Magnet Synchronous Motor
MTPA	: Maximum Torque per Ampere
FOC	: Field-Oriented Control
FW	: Flux Weakening
SOH	: State-of-Health
RUL	: Remaining-Useful-Life
EV	: Electric Vehicle
ICE	: Internal Combustion Engine
BEV	: Battery Electric Vehicle
GHG	: Greenhouse Gas
DOE	: Department of Energy
EMF	: Electromotive Force
SPWM	: Sinusoidal Pulse Width Modulation
SVPWM	: Space Vector Pulse Width Modulation
DPWM	: Discontinuous Pulse Width Modulation
VSI	: Voltage Source Inverter
DCC	: DC-Link Capacitor Current
MLC	: Multi-Layer Ceramic
ESR	: Equivalent Series Resistance
ESL	: Equivalent Series Inductance
PET	: Polyethylene Terephthalate
PP	: Polypropylene
PEN	: Polyethylene Naphthalate
IEC	: International Electrotechnical Commission
VEN	: Variable Electrical Network
KVL	: Kirchhoff's Voltage Law
OCV	: Open Circuit Voltage

CAD	: Computer-Aided Design
SOC	: State-of-Charge
BF	: Best Fit
RMS	: Root Mean Squared
RMSE	: Root Mean Squared Error
PV	: Photovoltaic
MC-GDPWM	: Multi-Carrier Generalized Discontinuous PWM
CMV	: Common-Mode Voltage

CHAPTER 1

INTRODUCTION

Electric vehicles (EVs) have shown the potential to reduce the carbon footprint of the transportation sector and create the opportunity for drivers to reduce fuel and regular maintenance costs in comparison to an internal combustion engine (ICE) vehicle [1], [2]. In the past decade, the sales of electric vehicles have steadily increased, and the trend is projected to continue as more government agencies across the world implement incentives to purchase EVs such as rebates and tax benefits [1], [3], [4]. The government of Canada has announced the "Action Plan" to streamline the adoption of EVs by the general public in an attempt to reduce the economy's dependency on non-renewable resources and mitigate tailpipe emissions from the transportation sector. As shown in Fig. 1.1 below, the total greenhouse gas (GHG) emissions from the transportation sector in Canada have been dominated by on-road passenger and on-road freight vehicles for decades [5]. This indicates that there is a significant opportunity to reduce the sector's total GHG through the reduction or elimination of on-road passenger vehicles with conventional ICEs.

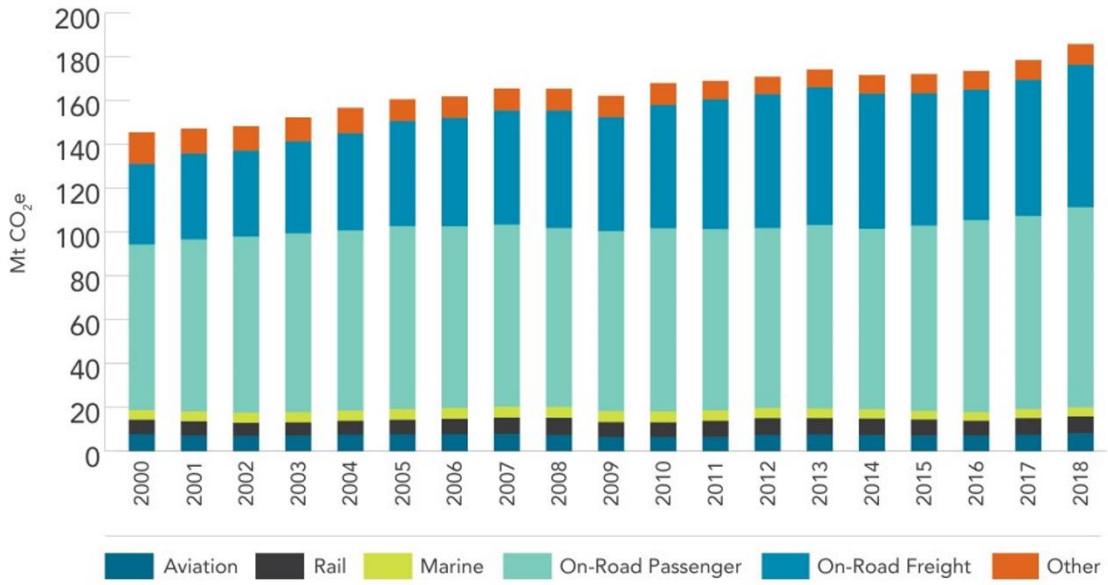

Fig. 1.1. Total GHG emissions from transportation sector in Canada, 2000-2018. (Source: Adapted from [5].)

Additionally, there are several targets set by government agencies such as the US Department of Energy (DOE) for the cost and power capabilities of electric traction drives.

The DOE is looking to produce 33-kW/L power density at $6/kW for a 100-kW drive, and 100 kW/L at $2.7/L for the inverter by 2025 [5]. This requires a significant improvement in power density and a reduction in price compared to current technologies. In order to meet the performance targets and achieve the widespread adoption of EVs, the technology must become more efficient to increase the vehicle range, more reliable to increase user safety, and more cost-effective to bring down the price of the vehicle. In general, there are two ways to increase electric vehicle efficiency and range, through changes to hardware, or to software. Changes in hardware may entail changes to the physical design of the electric motor or inverter, while changes in software would include adjustments and improvements in control strategies and implementation. Physical changes to the motor may include novel winding configuration, stator construction, or utilization of improved materials [7]-[9]. Physical changes to the inverter could entail replacing conventional IGBT or MOSFET switching devices with improved SiC or GaN alternatives or changing the inverter configuration to an alternative architecture such as a three-level or four-leg inverter opposed to a conventional three-phase two-level inverter [10]-[13].

However, hardware changes could require a full redesign of the system, adjustment of controls, refitting of housing, and can lead to a very costly and impractical solution. Meanwhile, adjustment of the control strategy implemented in the system can allow for a much more flexible and cost-effective approach to influencing system performance as opposed to adjustments on the hardware side. Furthermore, it is essential to monitor the present state-of-health (SOH) of the critical components within the motor drive to ensure safe and reliable operation, and to predict when preventative maintenance should occur to avoid catastrophic failure and reduce overall system downtime.

1.1 Research Objectives

The objectives of this thesis are to propose a dependable DC-Link capacitor SOH monitoring scheme designed for EV applications which features two condition monitoring methods: A parameter estimation method, and an analytic degradation accumulation method. In EV applications, it is desirable to utilize strategies that do not require additional hardware to avoid additional costs, redesign of the system housing, and increased system complexity. This thesis aims to utilize strategies that avoid the use of additional hardware

and use simple analytical models to reduce the computational burden on the system to keep these previously mentioned objectives in line with the scope of work. The final objective of this thesis is to propose a PWM selection strategy designed to prolong the lifetime of the traction electric drive by reducing the degradation of the DC-Link capacitor, while also maintaining sufficient inverter performance compared to conventional PWM methods.

1.2 Scope and Contributions of Study

The scope of the work carried out in this thesis includes a simulation based study of the impacts of sensor tolerance, sampling frequency, and external environmental conditions on the accuracy of a capacitance estimation method. An experimental implementation of the previously mentioned capacitance estimation method is carried out in order to validate the simulation study regarding the minimal sampling frequency required to make accurate and reliable estimations. The thesis also includes a proposed framework for modelling degradation accumulation in the DC-Link capacitor over a load profile. Finally, a simulation-based study is complete to quantify the benefit of the proposed PWM selection strategy to prolong the lifetime of the DC-Link capacitor.

The contributions of this thesis include the development of an established highly precise capacitance estimation method [6] toward EV applications through the consideration of ambient temperature, sensor tolerance, and sampling frequency. To experimentally determine the minimum sampling frequency required for adequate estimations of capacitance using a 100-kW electric traction drive and a configurable DC-Link capacitance bank used to emulate a degrading capacitor. Using the history of recorded estimations over time to provide a more accurate real-time estimation of capacitance using a non-linear curve fitting strategy. A PWM selection strategy designed to prolong the lifetime of the DC-Link capacitor in an electric drive without significant sacrifice of performance compared to conventional PWM control to allow for high-performance control with an increased inverter, and vehicle lifetime. A capacitor degradation model is implemented in an electric drive model in PLECS software in order to evaluate the ability of the proposed PWM selection method to reduce capacitor degradation under a drive cycle-based simulation to emulate real-world driving conditions.

1.3 Organization of Thesis

This thesis provides the theoretical knowledge required to understand the operation and control of an electric motor drive within an EV, and the purpose of the DC-Link capacitor within the drive. As well as an effective strategy to monitor the current condition of the DC-Link capacitor, and a novel PWM selection strategy in order to extend the lifetime of the capacitor and motor drive as a whole. The organization and flow of the proceeding chapters are as follows.

Chapter 2 presents the architecture of an electric motor drive and highlights the key components and control strategies utilized to effectively convert electrical power from a battery to controlled AC power used to adjust the speed and torque output of the EV.

Chapter 3 provides a closer look at the purpose of the DC-Link capacitor within the drive and identifies the different types of capacitors typically used in DC-Link applications. The failure mechanisms and failure rate modelling of a typical film capacitor is also presented.

Chapter 4 discusses various methods used to monitor the current condition of the DC-Link capacitor and highlights an effective strategy for condition monitoring in an EV application. Then an in-depth analysis of the impact of sensor tolerance and environmental conditions on the effectiveness of the condition monitoring method is provided. Experimental results are presented to illustrate the feasibility of the highlighted method in a real EV motor drive featuring a permanent magnet synchronous motor (PMSM).

Chapter 5 provides an analysis of the analytical modelling of the lifetime and degradation of the DC-Link capacitor and proposes a combined condition monitoring strategy that utilizes the mentioned degradation model along with the method provided in Chapter 4 for improved reliability.

Chapter 6 proposes a novel PWM selection strategy designed to extend the lifetime of the DC-Link capacitor by reducing the capacitor power losses in certain operating regions. The capacitor degradation model highlighted in Chapter 5 is used to validate the ability of the proposed PWM selection strategy to improve the lifetime of the DC-Link capacitor within an electric drive in a simulation environment.

Chapter 7 concludes the thesis by highlighting the key takeaways from the development of the capacitance estimation strategy from Chapter 4 and emphasizing the

system requirements needed to provide reliable condition monitoring. The conclusion also looks at the effectiveness of the proposed PWM strategy in extending the lifetime of the DC-Link capacitor and discusses future work to further the research presented in this thesis.

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CHAPTER 2

PERMANENT MAGNET SYNCHRONOUS MOTOR DRIVES

A PMSM drive consists of a permanent magnet synchronous machine, a voltage source inverter, current sensors, a position sensor, a controller, a DC-Link capacitor, and a dc voltage source, which is a high voltage battery pack in EV applications. Feedback signals from the current sensors located on each of the three phases of the motor and the position sensor placed on the rotor are used by the controller to generate control signals for the voltage source inverter. The inverter utilizes these control signals to manipulate the magnitude and frequency of power delivered to the motor to control the output torque. The typical configuration for a PMSM drive is illustrated in the Fig. 2.1 below.

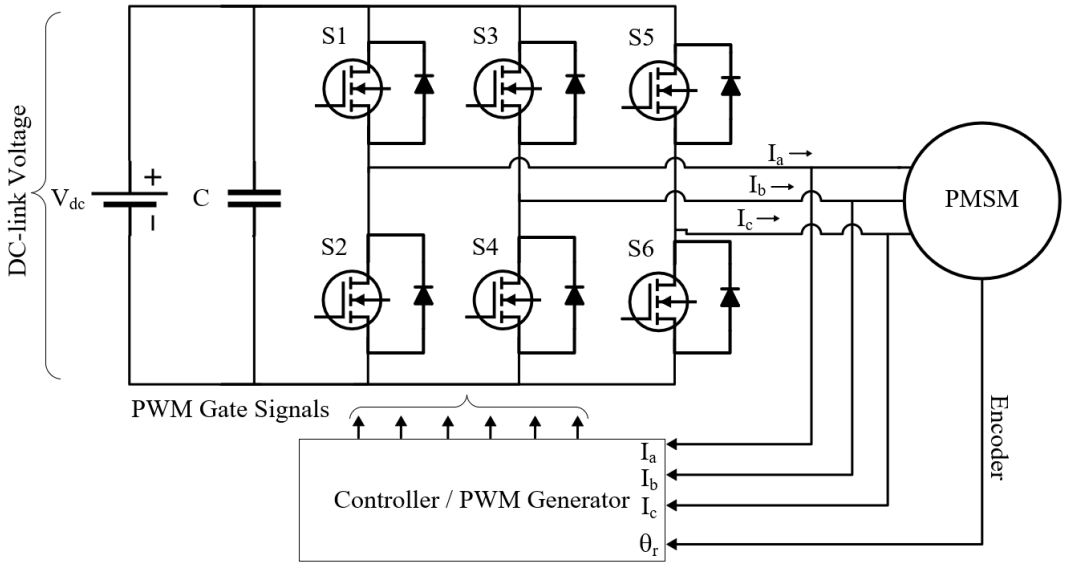


Fig. 2.1. Conventional PMSM drive configuration for EV applications.

The two-level three-phase inverter depicted in Fig. 2.1 utilizes six semiconductors to control the flow of power from the DC side to the AC side of the converter and vice versa [1], [2]. The mathematical conversions required to understand how the control of a PMSM in a traction electric drive is carried out are provided in this chapter. Furthermore, the conventional control strategy that is implemented in EV applications is introduced to provide a clear understanding of the control objectives within the motor drive.

2.1 PMSM Drive Control Theory

PMSMs have been rapidly gaining popularity in propulsion applications due to their high-power density, absence of rotor windings, and their rugged physical structure built for high-speed operation [3]-[6]. A widely employed and effective strategy to control the output torque of the motor is through field-oriented control (FOC), also known as vector control. Thus, FOC requires the transformation of the three phase stator currents, voltages, and flux linkages into a stationary reference frame known as the *dq* reference frame [7]. The *dq* reference frame depicts three-phase ac signals as dc signals with a direct and quadrature axis component, hence *d* and *q*. Since the inductances of a PMSM vary as a function of rotor position and speed, the modelling and control of the machine become extremely complex in the three-phase reference frame. Thus, the *dq* reference frame is utilized to eliminate the machine parameters dependence on rotor position and create a constant parameter equivalent model. The conversion from the *abc* reference frame to the *dq* reference frame is complete through the Park Transformation. The relation for the Park Transformation and the configuration of the *abc* frame in reference to the *dq* axis is given below [7].

$$\begin{bmatrix} d \\ q \\ 0 \end{bmatrix} = \frac{2}{3} \begin{bmatrix} sin\theta & \sin\left(\theta - \frac{2\pi}{3}\right) & sin\left(\theta + \frac{2\pi}{3}\right) \\ cos\theta & cos\left(\theta - \frac{2\pi}{3}\right) & cos\left(\theta + \frac{2\pi}{3}\right) \\ 1/2 & 1/2 & 1/2 \end{bmatrix} \begin{bmatrix} a \\ b \\ c \end{bmatrix} \tag{2.1}$$

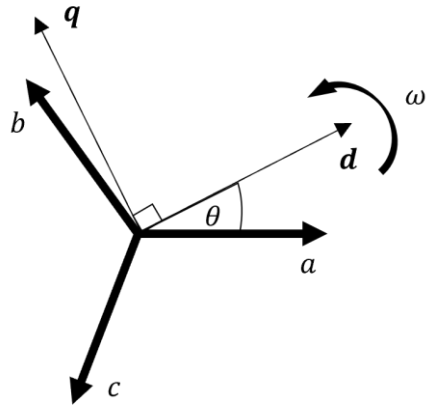
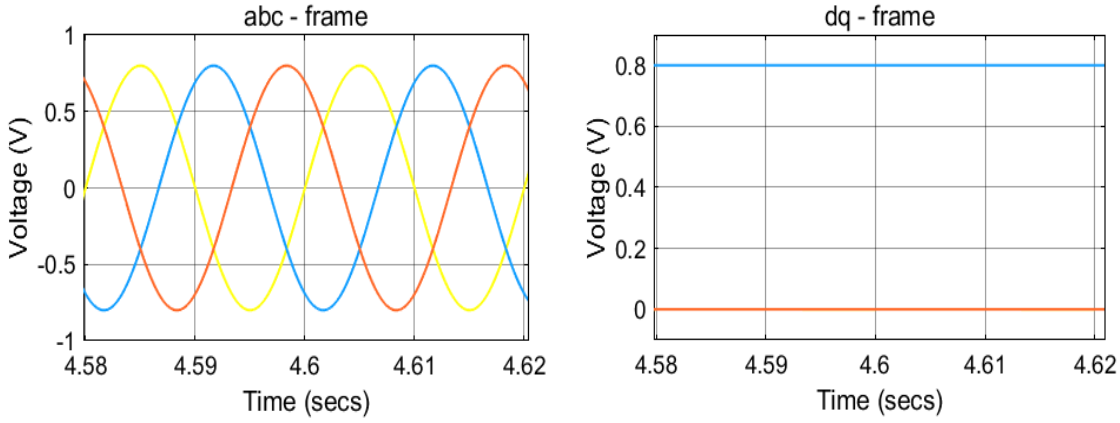


Fig. 2.2. Three-phase vectors in relation to *dq* axis when *d*-axis is aligned to phase *a*.

Converting into a two-phase dc reference frame greatly simplifies the modelling and control of the PMSM under FOC control, allowing for conventional PID controllers to be utilized to eliminate the error between the drive output and the commanded value.



(a) (b)

Fig. 2.3. Balanced three-phase voltage signals. (a) *abc* reference frame. (b) Constant *dq* reference frame.

In the case of an electric vehicle application, there are some performance requirements that must be met by the electric drive in order to achieve adequate performance for the user. One of these requirements is to be able to produce high torque at low vehicle speeds for vehicle starting conditions. Another requirement is to have a high maximum speed in order to meet the specifications of the vehicle maximum speed. Under FOC control, the maximum torque of the machine can be achieved from zero speed up to the rated speed of the machine. At the rated speed of the machine, the maximum available voltage is supplied to the machine, and the back electromotive force (EMF) generated is equal to the supplied voltage. The machine cannot be sped up beyond this point because it will cause the back-EMF generated by the machine to exceed the voltage supplied by the inverter, which eliminated the ability to properly control the current output of the inverter. To get around this issue and increase the speed of the PMSM beyond the base speed, field-weakening (FW) control is utilized [3], [8].

The principle behind FW control is to demagnetize the PM on the rotor by applying a negative d-axis current on the stator and thus reducing the back-EMF. This allows the maximum voltage supplied to the machine to keep properly controlling the output torque. That is why this region of operation is also known as the constant power region, and the region leading up to the base speed in which maximum torque is achievable, is known as

the constant torque region. The typical PMSM torque speed map along with the various operating regions is illustrated below.

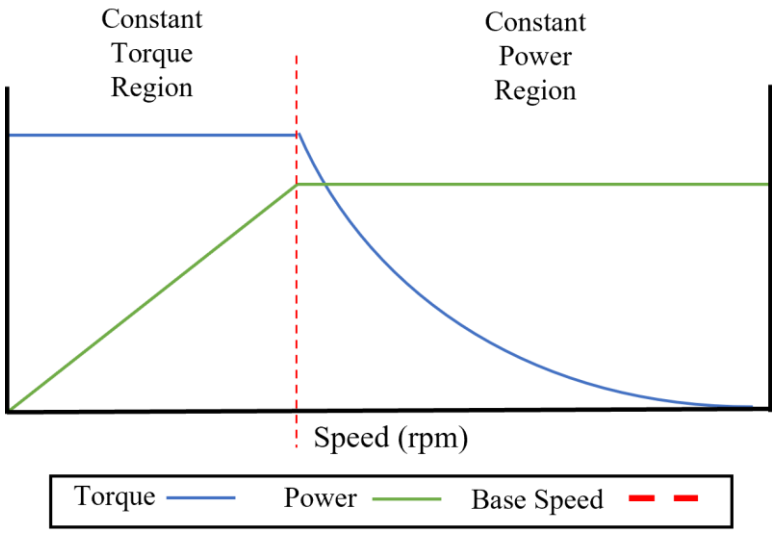


Fig. 2.4. Torque and power versus speed characteristic of PMSM drive under MTPA and FW FOC.

In electric vehicle applications, the area under the blue curve in Fig. 2.4 is known as the torque-speed map of the drive. This plot is essential as it illustrates the achievable operating points with the given inverter and machine parameters of the electric drive. Different driving scenarios and events require operation within different regions of the torque-speed map. For example, when accelerating from zero speed the torque requirement from the drive will be very high even though the speed of the vehicle is low. This would constitute operation in the upper left corner of the torque-speed map. If the vehicle is travelling on the highway at a high speed and the driver wants to slightly increase their speed, a high-speed and low torque operating point in the lower right corner of the torque-speed map may be required. Whereas typical driving procedures such as urban driving would require operation within the lower center of the torque speed map [9]. Understanding the drives operation across the torque speed map in a drive-cycle analysis can allow for improvements in motor control based on the frequency of operation in certain regions or lack thereof. This will be considered further in the PWM selection strategy presented section in Chapter 6 to prolong the lifetime of the DC-Link capacitor.

2.2 Pulse Width Modulation Control of Voltage Source Inverters

Pulse width modulation is an effective and flexible control strategy used to generate high quality sinusoidal currents at the output of a power converter [1], [2]. There is an abundance of PWM methods present in the literature depending on the system architecture and application, some well-established conventional methods and some designed to provide enhancement in performance either in terms of power losses, output current quality, common mode voltage, or DC-Link capacitor current [10]-[18]. This creates an important task in the design of a motor drive system, to select the appropriate PWM strategy to meet the critical performance criteria associated with a given application. The basic principles of the conventional PWM methods typically employed in traction electric drives are highlighted in the proceeding sections.

2.2.1 Sinusoidal PWM (SPWM)

The fundamental PWM strategy used in two-level three-phase inverters is known as sinusoidal pulse width modulation (SPWM). SPWM is a carrier-based modulation strategy which indicates that its gate signals are produced by the comparison of an analog reference signal with a high frequency carrier signal. The intersection of the reference signal and the carrier signal toggles the power switching devices gate signal which causes the device to turn on or off accordingly. An example reference waveform and carrier signal used for SPWM are illustrated in Fig. 2.5.

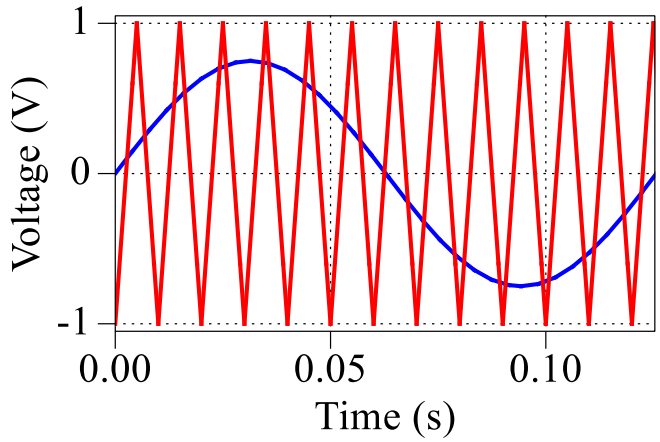


Fig. 2.5. Comparison of high frequency triangle carrier and sinusoidal reference signal used for SPWM.

The frequency of the triangle carrier signal determines the switching frequency of the inverter, which intuitively describes the rate at which the transistors of the inverter are

being switched. A higher carrier switching frequency allows for a more precise output sinusoidal waveform, but also creates enhanced thermal stress on the switching devices and the inverter as a whole. The modulation index is defined as the ratio of the reference signal to the carrier wave and is directly related to the output performance of the inverter. The modulation index can be described according to the following equation [1].

$$m_a = \frac{V_{ref}}{V_{carrier}} = \frac{2V_{ph}}{V_{dc}} \tag{2.2}$$

where V_{ref} is the amplitude of the reference signal, $V_{carrier}$ is the amplitude of the carrier signal, V_{ph} is the fundamental component of the inverter phase voltage, and V_{dc} is the value of DC-Link voltage supplied to the inverter. From (2.2) it is clear that the modulation index can also be used to determine the value of phase voltage expected for a given value of control signal. It also shows that the value of DC-Link voltage directly impacts the modulation index for a given control voltage. There are generally two regions of operation in terms of the modulation index, the linear modulation region, and the overmodulation region [1]. In the overmodulation region, low order harmonics are introduced into the output line voltage, causing a significant increase in phase current THD and deterioration of inverter performance without some sort of specialized control [19], [20]. Therefore, is it desirable to operate in the linear modulation region, which is defined as follows for SPWM,

$$0 \leq m_a \leq 1$$

The dc-bus utilization is a ratio of the output voltage capable by the inverter under the given control strategy. Under SPWM the maximum output voltage possible without entering the overmodulation region is achieved when the modulation index is unity. As shown below, the maximum achievable output phase voltage under SPWM is only half of the DC-Link voltage.

$$V_{ph} = m_a\left(\frac{V_{dc}}{2}\right) = (1)\left(\frac{V_{dc}}{2}\right) = 0.5 * V_{dc} \tag{2.3}$$

2.2.2 Space Vector PWM (SVPWM)

One of the most common and effective PWM strategies employed in traction electric drives is space vector pulse width modulation (SVPWM) due to its improved harmonic performance and improved dc-bus utilization compared to SPWM [11], [21], [22]. SVPWM operates on the principle of using multiple space vectors to formulate a single rotating vector which represents the output voltage of the inverter. For a two-level three-phase inverter, there are eight different configurations that the six switches may take at any given time. The eight configurations consist of six active states, and two zero states in which all the top or bottom switches are shorted to the positive or negative terminal of the dc-bus respectively as shown in Fig. 2.6.

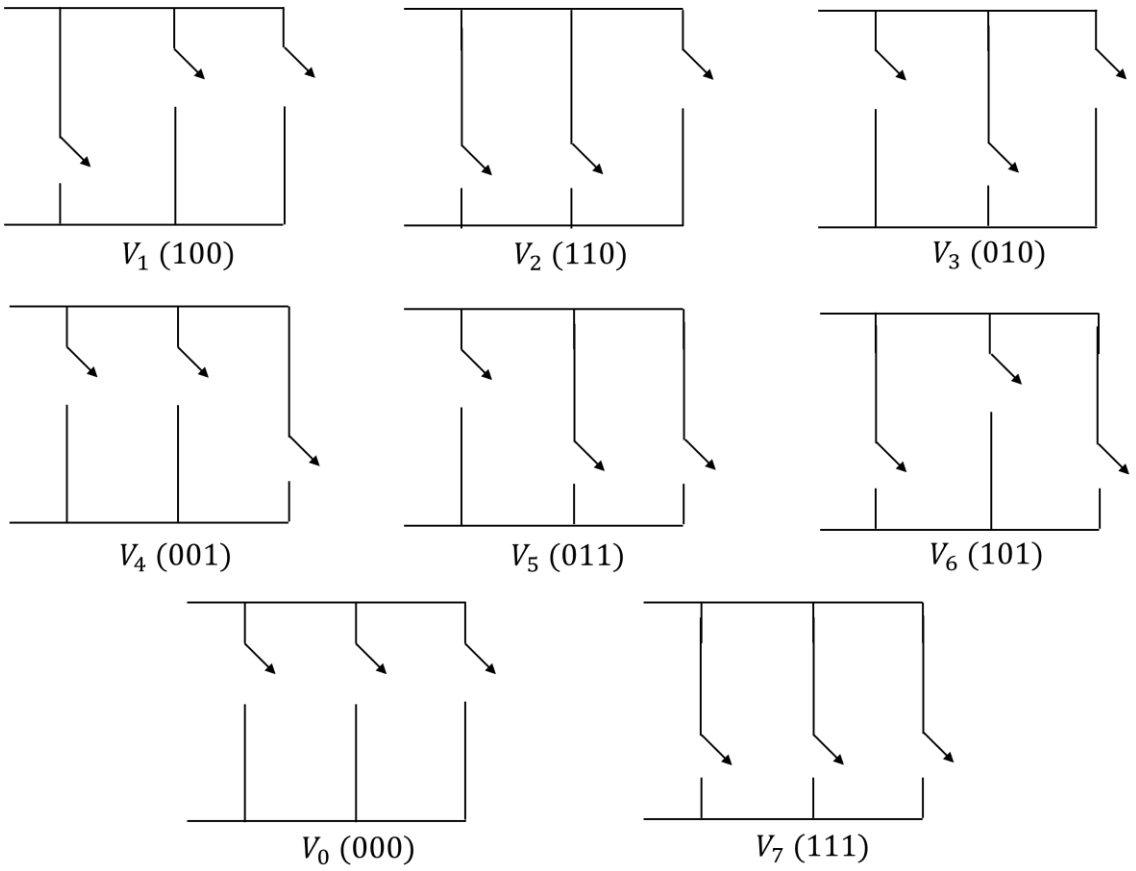


Fig. 2.6. Possible switching configurations of VSI under SVPWM control.

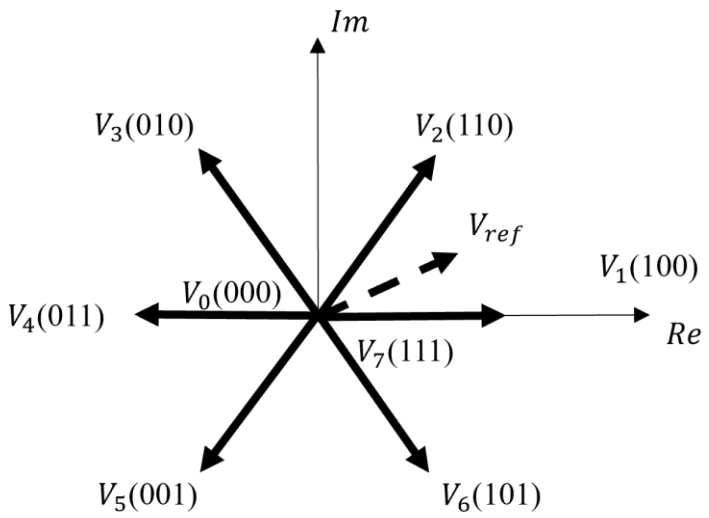


Fig. 2.7. Equivalent space vectors of VSI for the switching states in Fig. 2.6.

Each configuration of inverter switches corresponds to a single space vector in the *dq* reference frame as shown in Fig. 2.7. By actively controlling the switching between two adjacent voltage vectors along with the zero vectors, the reference voltage V_{ref} can be formed into a rotating vector with a frequency related to the rotational frequency of the motor. In the first sector of the space vector plane, the following equations are used to calculate the time spent occupying each active vector in order to achieve proper output control [21],

$$T_1 = T_s * m * \frac{sin(60° - \alpha)}{sin\ (60°)} \tag{2.4}$$

$$T_2 = T_s * m * \frac{sin(\alpha)}{sin\ (60°)} \tag{2.5}$$

and the zero vectors equally share the remaining portion of the fundamental period as follows,

$$T_7 = T_8 = T_s - T_1 - T_2 \tag{2.6}$$

One of the main benefits of using SVPWM is the increased dc-bus voltage utilization. Under SPWM, it was shown that the maximum achievable phase voltage is equal to half of the DC-Link voltage. Meanwhile, SVPWM allows for a 15% increase in output voltage, corresponding to the following maximum phase voltage.

$$V_{ph} = 1.15 * m_a \left(\frac{V_{dc}}{2}\right) = 1.15 * (1) \left(\frac{V_{dc}}{2}\right) = 0.575 * V_{dc} \tag{2.7}$$

2.2.3 Discontinuous PWM (DPWM)

Discontinuous modulation schemes are designed to reduce the switching losses of pulse width modulated inverters [23], [24]. DPWM is a carrier-based modulation technique which has a zero-sequence signal injected into the three-phase modulating waveforms. The zero-sequence signal causes the modulating wave to clamp to the positive or negative rail of the inverter DC-Link voltage for a portion of the fundamental cycle. Therefore, reducing the number of switching events, and in turn, reducing the switching losses. The relation for determining the zero-sequence signal to inject to the modulating waveforms is shown in (2.8) as presented in [23].

$$V_0 = \frac{1}{2} V_{dc}(1 - 2\sigma) - \sigma V_{min} + (1 - \sigma) V_{max} \tag{2.8}$$

where, V_{dc} is the DC-Link voltage, V_{max} and V_{min} are the maximum and minimum of the three-phase modulating waveforms, and σ is given by the following equation.

$$\sigma = 1 - \frac{1}{2}\left[1 + sgn\left(cos3(\omega t + \gamma)\right)\right] \tag{2.9}$$

In (2.9) the value of γ can be varied to produce alternate DPWM methods. DPWM0, DPWM1, DPWM2, and DPWM3 can all be derived from this relation with various values of γ. Each DPWM variant similarly clamps the modulating waveform for 120° of the fundamental cycle, but each method changes the location within the fundamental cycle

which the clamping will occur. The modulating waveforms for each variant of DPWM are illustrated in Fig. 2.8.

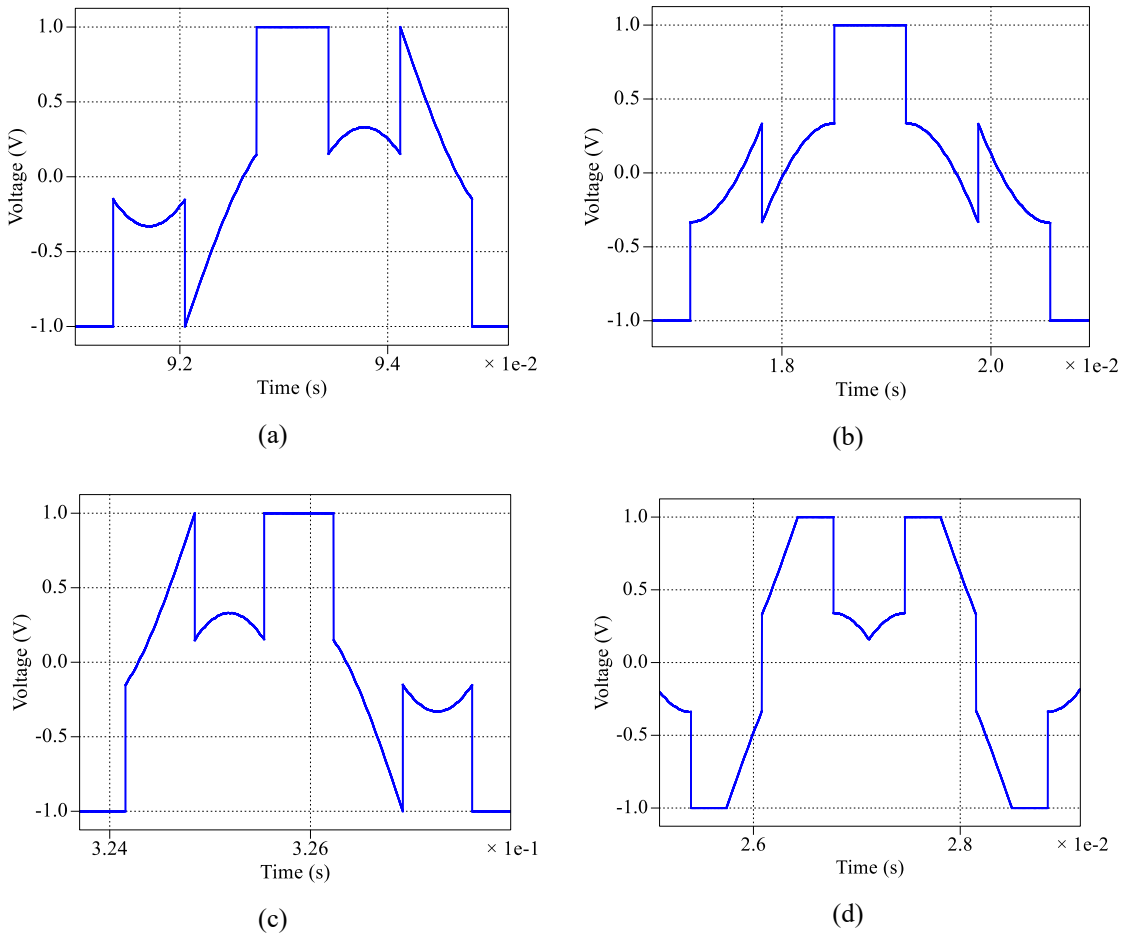


Fig. 2.8. Modulation waveforms (a) DPWM0. (b) DPWM1. (c) DPWM2. (d) DPWM3.

Furthermore, there is an extension of the DPWM known as generalized DPWM (GDPWM) which transitions between each DPWM variant depending on the load conditions to ensure minimal switching losses are always generated [24]. DPWM methods are successful in reducing the switching losses of the inverter but cause a deterioration in the output current waveform quality. The increased THD in the output currents being delivered to the motor causes an increase in torque ripple which has unfavorable outcomes in propulsion applications including increased machine losses, vibrations, and less smooth driving conditions for the driver.

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CHAPTER 3

DC-LINK CAPACITORS FOR EV APPLICATIONS

The reliability of an electric vehicle must always be maintained at a high level in order to ensure user safety and satisfaction at all times. The electric drive is an electrical system which controls the flow of power from the EVs battery bank to the electric motor to realize the desired action commanded from the user. The electric drive is therefore essential to the proper operation of the vehicle and must be monitored to provide a safe user experience. Therefore, it becomes important to identify the main causes of system failure. The DC-Link capacitor is the most delicate component within the voltage source inverter (VSI) as it attributes to 30% of failures in power electronic systems, while the PCB accounts for 26%, semiconductors for 21%, and the remaining are negligible in comparison [1]-[3]. Consequently, ensuring adequate operation and conditions for the DC-Link capacitor can significantly improve the reliability of the VSI and the electric vehicle as a whole.

The DC-Link capacitor is an electrical component that is responsible for maintaining a constant dc voltage at the input of the VSI by filtering the voltage provided from the vehicle's battery pack, and for absorbing high frequency current components generated from the switching behaviour of the inverter [4]-[6]. Thus, the DC-Link capacitor provides a constant DC-Link voltage while also mitigating high frequency harmonics from the drive. Due to the sizing constraints of electric drives previously highlighted in the introduction chapter [7], the components are fitted to be very compact and are placed in an enclosed housing for a physically rigid design and to limit EMI [8]. Additionally, in traction inverter applications, overload conditions of up to 2.5 times rated capacity can last for several minutes [9], thus, the DC-Link capacitor is exposed to harsh operating conditions within the electric drive, experiencing high rms ripple currents and elevated temperatures. These factors contribute to the degradation of the capacitor and directly influence the occurrence of the device's end-of-life as will be discussed further in the coming sections. It is desirable to develop low cost, effective strategies to determine the level of degradation that has occurred in the DC-Link capacitor in order to make predictions of when maintenance should take place to prevent total device failure and maintain the safety of the EV user. In the next subsections of this chapter, the types of capacitors utilized in DC-Link applications

are compared and discussed, then the critical stressors and failure mechanisms of film capacitors are examined, followed by a discussion of failure rate modelling of electronic devices to develop a deeper understanding of the physical characteristics of the capacitor and how the device degrades over time.

3.1 Types of Capacitors Used in DC-Link Applications

When considering an inverter being used for EV applications, there are certain requirements that the DC-Link capacitor must satisfy for safe and reliable operation [9], [10]. First and foremost, the capacitor must have sufficient capacitance to limit the DC-Link voltage ripple below 10% of the rated voltage under all operating conditions [6]. The selected capacitor must also be able to withstand the worst-case scenario magnitude of ripple current estimated or predicted for the system. Finally, the capacitors hot spot temperature should not exceed 105˚C during operation [11], [12]. The three types of capacitors that are typically selected to meet these requirements in DC-Link applications include Aluminum Electrolytic Capacitors, Metallized Polypropylene Film Capacitors, and Multi-Layer Ceramic Capacitors (MLC-Caps) [6], [9], [13].

The materials used and the construction of each capacitor create differences in their cost, nominal ratings and output performance, which creates the opportunity to select the optimal capacitor for a given application. The electrolytic capacitor has the most cost-effective solution and also features the highest energy density compared to film and MLC capacitors. However, the electrolytic capacitor has greater equivalent series resistance (ESR) compared to its counterparts. The high ESR causes increased power losses within the capacitor and in turn, leads to an increase in hot spot temperature. These factors lead to shortened lifetime and decreased reliability for electrolytic capacitors in high current applications such as EV drives [4], [5], [13]. Meanwhile, MLC capacitors have the advantage of reduced volume and an increased maximum capable hot spot temperature. However, the high cost and voltage instability of these capacitors make them inferior to film capacitors for EV applications. Film capacitors have low ESR, high voltage ratings, high ripple current ratings, increased lifetime and improved reliability compared to electrolytic and MLC capacitors. That is why film capacitors are commonly selected for the design of the DC-Link in EV applications, and film capacitors will be considered going forward in this thesis.

3.2 Internal Characteristics of Film Capacitors

Film capacitors can be further divided into various categories based on the type of material used in the dielectric. The main types of dielectrics used are Polypropylene (PP), Polyethylene terephthalate (PET), and Polyethylene naphthalate (PEN) [12]. Each dielectric will result in different internal characteristics and device behaviour in terms of changes in capacitance and internal resistance in relation to external conditions such as temperature, humidity, and operating frequency. Regardless of the dielectric material present in the film capacitor, there are three main components used to model the capacitor. The equivalent series inductance (ESL), equivalent series resistance (ESR), parallel resistance (Rp), and capacitance (C). The equivalent circuit model for film capacitors and the impedance of the capacitor are highlighted below.

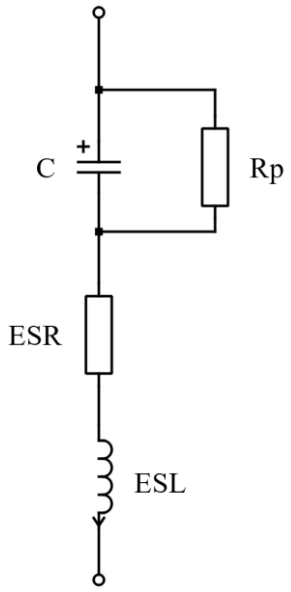

Fig. 3.1. Equivalent circuit model of a capacitor including resistance inductance and capacitance elements.

$$Z_{cap} = \sqrt{R_{ESR}^2 + \left(2\pi f * ESL - \frac{1}{2\pi f * C}\right)} \tag{3.1}$$

From (3.1) it is evident that the impedance of the capacitor is impacted by frequency. In most cases for high voltage film capacitors, the ESL and parallel resistance are negligible and can be ignored when modelling the capacitor [13]. ESR is the main factor contributing

to the device's power losses and is also dependent on frequency. Therefore, the frequency must be taken into account to make accurate power loss calculations for the DC-Link capacitor. The equation used to calculate the capacitor power losses is shown below. The power losses are determined by accumulating the ohmic I^2 R losses at each distinct frequency from 1 to n.

$$P_{cap} = \sum_{i=1}^{n} \left[ESR(f_i) * {I_{cap}}^2_{RMS}(f_i) \right] \tag{3.2}$$

3.3 Critical Stressors of Film Capacitors

The critical stressors of an electrical component are the key factors which cause the degradation of the device and lead to the end of the component's useful life. For film capacitors, three of the major critical stressors include ambient temperature, voltage stress, and ripple current stress [14], [15]. Humidity is often considered as a critical stressor for film capacitors as well, but in the case of EV drives the capacitor is commonly in an air-sealed housing according to the international electrotechnical commission (IEC) standards which drastically reduces the effects of humidity [16]. In the case of film capacitors, one of the most prominent degradation mechanisms is the self-healing process [17], [18]. The self-healing process occurs when there is a defect in the capacitor's electrode due to over-voltage. This causes the current density in this region of the electrode to increase significantly, causing an increase in temperature until the effected portion of the electrode evaporates [19]. This allows the capacitor to continue regular operation with a small increase in ESR and a decrease in capacitance. Additionally, due to the water vapor in the air gap between the aluminum film and polypropylene film, oxidation-reduction reactions occur. These electrochemical reactions also lead to the reduction of capacitance. The final mechanism through which the capacitor degrades is through partial discharge. Partial discharge is related to a small amount of discharge that occurs within the insulator of the capacitor. Air, water vapor, and other impurities present within the capacitor, partial discharge is unavoidable. Eventually, the self-healing, electrochemical reaction, and partial discharge processes lead to the end of life of the capacitor. The end-of-life criteria for film

capacitors is characterized by a 5% reduction in capacitance from its initial value [5], [13], [20].

Generally, the failure of a film capacitor can be classified as either sudden failure or aging failure [21]. Sudden failure is caused by a single over stress event, while aging failure is due to the degradation of the capacitor's materials over time. In the case of sudden failures, the capacitor may either enter an open-circuit state or a short-circuit state [22], [23]. In either case, system maintenance is required as the DC-Link capacitor is essential to the proper operation of the electric drive. However, one case poses a more serious threat to the system and a hazard to the user. In the open-circuit state, the capacitor is disconnected from the DC-Link and therefore the failure has no path to propagate further to damage additional components, and there is minimal threat posed to the user. Meanwhile, in the case of a short-circuit failure, the capacitor enters a resistive state which creates a low impedance path across the input of the DC-Link voltage through the film capacitor. This can potentially be extremely hazardous as high currents will pass through the device, causing melting of the dielectric material within the capacitor. This may lead to the release of hydrocarbon-based gases within the traction drive, which could be ignited and cause an explosion [22], [23]. In the case of aging failure, the capacitor experiences a reduction in capacitance and an increase in ESR over time due to the degradation mechanisms previously mentioned, which eventually lead to the end-of-useful life of the device when the capacitance drops 5 % from its initial value [5], [13], [20].

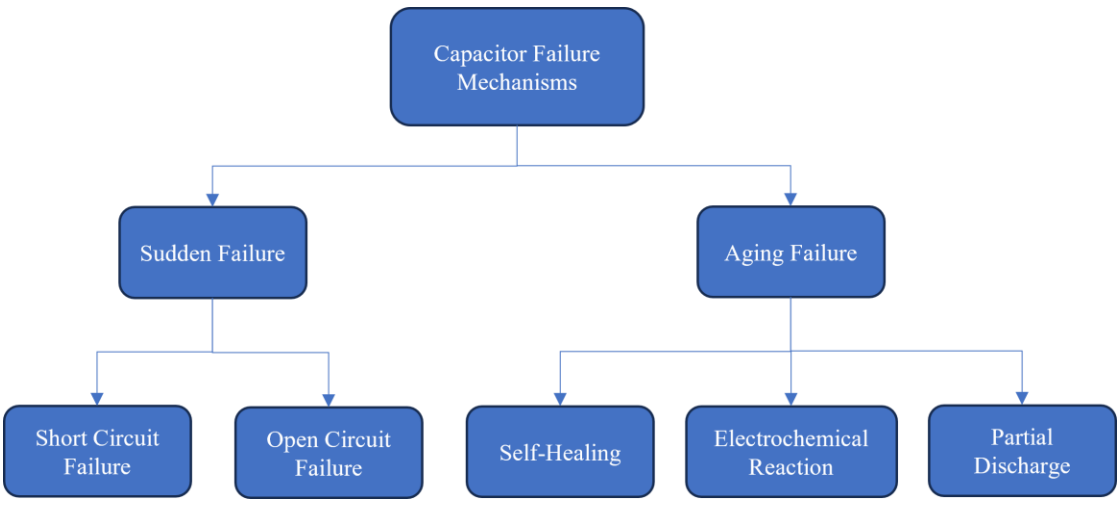

Fig. 3.2. Failure mechanisms of film capacitors in DC-Link applications.

3.4 Understanding Failure Rate Modelling of Electronic Components

Traditionally, the failure rate of DC-Link capacitors and other electronic components could be described as a function of time according to a bathtub curve as shown in Fig. 3.3. [22], [24]-[26]. This indicates that there is an increased chance of failure occurring in the early stage of life, or in the final stages of its lifetime. The early lifetime period is known as the early failure period. Failures during this period are usually attributed to defects occurring due to faulty materials or poor manufacturing processes. Meanwhile, in the later stages of the device's lifetime in the region known as the "wear-out failure period", the device is expected to fail as the device has served its purpose for a time close to its rated lifetime, and wear-out of the dielectric material occurs. Between the early failure period and the wear-out failure period, there is the random failure period. This region indicates the portion of time which the capacitor is operated at or below rated conditions as intended in the original system design. In this region, the capacitor has already shown adequate performance past the early failure period, thus indicating there are no manufacturing defects, but has not yet reached the predicted end of life of the device. In this region, the capacitor has the lowest chances of failure, and there is no specific type of fault that is most likely to occur, thus the name random failure period.

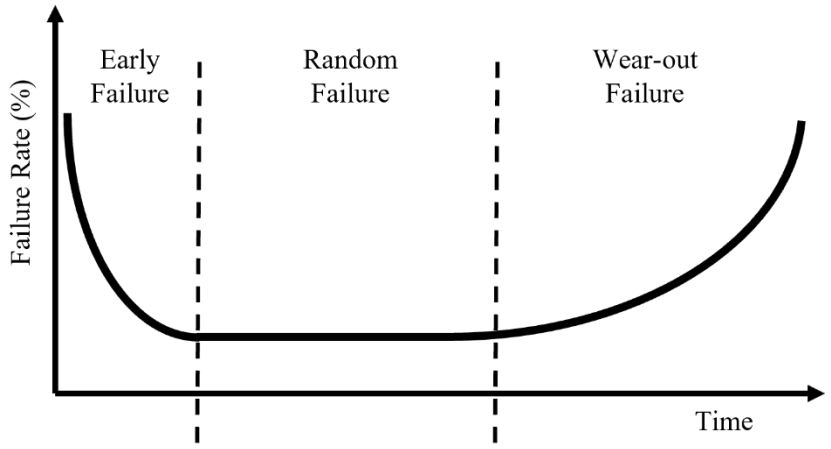

Fig. 3.3. Bathtub curve conventionally used to model the failure rate of electronic components over time.

However, more recently it has been shown that this widely accepted bathtub model is unsuitable for reliable failure prediction and modelling for electronic components [27]. Due to the constant enhancement of the manufacturing processes, product screening, burn-in testing, and quality control procedures associated with electronics manufacturing, it has

been shown that the early failure period is not present. Several case studies were performed to prove that the early failure period is not present in modern capacitors [28]-[30]. Additionally, the previously constant failure region in the random failure period has been shown to be non-constant. The failure rate of DC-Link capacitors increases over its lifetime from the moment it is put into operation due to the aging mechanisms of the device which leads to time dependent degradation of the device, leading to an increased chance of failure over the course of its lifetime. The degradation of the capacitor is dependent on the materials, construction, application, and loading conditions of the device, which makes it difficult to create a single model that can be used for modelling the failure rate of any capacitor. [27] concluded that the failure rate should be determined using failure data rather than assuming a failure rate model. Thus, it is crucial to monitor the SOH of the DC-Link capacitor during its entire operational lifetime to ensure that the device is still suitable for operation as device failure could occur at any time and not only during some predefined regions.

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CHAPTER 4

DC-LINK CAPACITANCE ESTIMATION FOR EV APPLICATIONS

As mentioned in Chapter 3, DC-Link capacitors undergo inevitable degradation over the course of the EVs operational lifetime, eventually leading to the devices end-of-life, which is defined as a 5% reduction in initial capacitance for film capacitors [1], [2]. Therefore, it becomes imperative to monitor the level of degradation that has occurred in the capacitor in order to know when to perform preventative maintenance before failure occurs and poses harm to the user. The capacitance of a capacitor provides a very clear indication of the device's current health condition and is most commonly used as the condition monitoring parameter in condition monitoring methods [3]. Several efforts have been made over the years to develop effective strategies to perform condition monitoring of DC-Link capacitors in a variety of applications [4]-[13]. [4] provides a comprehensive overview of the condition monitoring methods available for DC-Link capacitors and categorizes the methods based on the principles used to determine the device characteristics.

The first principle used is periodic small-signal ripple for capacitance estimation, the second principle uses non-periodic large signal charging or discharging to estimate capacitance, and the final principle uses a black-box model and training data to make estimations of capacitance based on capacitor voltage and currents. Furthermore, the condition monitoring methods are categorized based on the time when the estimation is performed. Some methods must be performed with the capacitor removed from the motor drive structure; this is known as an offline method for obvious reasons. Offline methods can be highly accurate but cannot be performed during regular operation and require removing the device from the system and are therefore not desirable for continuous condition monitoring over the lifetime of the vehicle. On the other hand, online methods are performed during regular operation and allow for continuous condition monitoring without having to alter the motor drive. The final category is known as Quasi-online methods. These are methods which can be executed without removing the device from the system but can only be performed during certain operating conditions such as during startup or shutdown. Either online or quasi-online methods are effective for the application

of EV DC-Link capacitors to avoid additional system downtime and to provide real-time vehicle information to the user.

In [5], an external variable electrical network (VEN) is used to discharge the DC-Link voltage of a grid-tied VSI to make an estimation of capacitance and ESR for electrolytic capacitors. [6] uses a constant duty cycle to discharge the DC-Link through the windings of an electric machine in an adjustable speed drive and makes an estimation of capacitance and ESR based on the ripple voltage of the capacitor. This method also makes an estimation of capacitor temperature by relating it to the stator windings temperature. The DC-Link voltage is discharged through the motor windings similarly in [7], and the capacitance is estimated using the integration of the discharge current divided by the voltage drop across the DC-Link. An alternative method is proposed in [8] which utilizes high bandwidth current and voltage sensors to acquire the capacitor voltage and current to make an estimation of the capacitor's impedance, ESR, and capacitance. Furthermore, this method also makes an estimation of capacitor core temperature based on the estimated parameters. [9] calculates the DC-Link capacitance using the power losses of the device. The capacitor power loss is expressed as the difference between the grid and inverter in a grid-tied VSI application, and capacitance is calculated as the power losses divided by the product of the DC-Link voltage and the first derivative of the DC-Link voltage. A capacitance estimation method for aerospace drives is proposed in [10] which makes use of DC-Link voltage and input inverter current measurements to calculate the DC-Link capacitor current, and like [7] makes the calculation of the integration of capacitor current divided by the capacitor voltage to estimate capacitance with relatively high accuracy. However, this method involves the use of high-performance current sensors on the input of the inverter which are not typically available in conventional motor drives for EV applications. In [11], a stochastic approach is used to estimate the capacitance, ESR, as well as ESL for an electrolytic capacitor using an adjustable transfer function in order to minimize the error seen between the predicted value and true value of DC-Link voltage and current. The predicted voltage and current are utilized to estimate the capacitor parameters using the least mean squares algorithm with less than 1% error. A novel method is proposed in [12] which allows for estimation to be performed during regular operation of a grid-tied motor drive. During the periodic fluctuation of the 3-phase voltage supplied from the grid, the

DC-Link transitions from being supplied by the grid to supplying the load intermittently. The constant charge and discharge of the capacitor is used to determine the DC-Link capacitance using the integration of current over the drop in DC-Link voltage. However, this method is performed during regular operation which may pose unnecessary risk to the user, and this method also considers a grid-tied drive as opposed to battery-fed VSI as we would be expecting in an EV application.

The previously mentioned capacitance estimation methods for condition monitoring show sufficient accuracy in simulated and experimental results. However, these methods involve either the use of additional sensors or hardware, upgrading of existing sensors, injection of current or voltage signals into the motor drive, considering alternative system architecture and types of capacitors compared to EV's, are performed offline or during regular operation, or some combination of each of these issues. This makes the methods unsuitable for EV condition monitoring applications. Additionally, several capacitor condition monitoring methods rely on the estimation of ESR in the case of electrolytic capacitors. However, as mentioned previously, for EV applications film capacitors are more commonly selected due to their high current and temperature capabilities and extended rated lifetime. The ESR of film capacitors is extremely small compared to electrolytic capacitors [13], which makes it extremely difficult to accurately determine, making it impractical to consider any methods which estimate ESR for condition monitoring purposes when film capacitors are used.

A method for capacitance estimation is proposed in [13] that allows for an effective and practical solution for EV applications. This method introduces LC resonance into the system by discharging the DC-Link capacitor through the stator windings of the electric machine in an electric motor drive. The preexisting phase current sensors are utilized to measure the large signal discharge current to avoid the use of any additional hardware or any changes to the motor drive architecture. The measured current signal is fit to a known relation for the current response in an under-damped RLC circuit that is dependent on the circuit parameters, allowing for an estimation of capacitance using only the discharge current signal. This method has shown very high accuracy with an estimation error of less than 1% in experimental tests for both electrolytic and film capacitors. The SOH monitoring method proposed in this thesis utilizes the capacitance estimation method

proposed in [13] due to the simple implementation, low cost, and effectiveness in estimating the DC-Link capacitance without the use of additional hardware. This thesis looks to expand upon the work presented in [13] to further adapt the method towards EV applications by taking into account several factors associated with implementation within a real motor drive including sensor tolerance or signal noise, sampling frequency, motor parameters of a modern PMSM drive, and ambient temperature. Additionally, the consideration of parallel capacitors on the dc-bus is addressed, as well as the ability to improve estimation accuracy by using the history of recorded estimations in a curve fitting algorithm.

4.1 Capacitance Estimation Using LC Resonance

The method used for capacitance estimation in [13] uses the principles of a fundamental RLC circuit to estimate the capacitance of the DC-Link capacitor. Whenever the motor drive is being shut down, the DC-Link can be disconnected from the dc power supply, and by toggling certain switches in the VSI, the equivalent circuit of the motor drive simplifies as shown in Fig. 4.1. Here the resistance and inductance represent the equivalent resistance and inductance of the machine stator windings. The DC-Link capacitor is represented by a capacitance and equivalent series resistance (ESR), while the inverter switching devices are represented by the forward voltage drop and blocking diode.

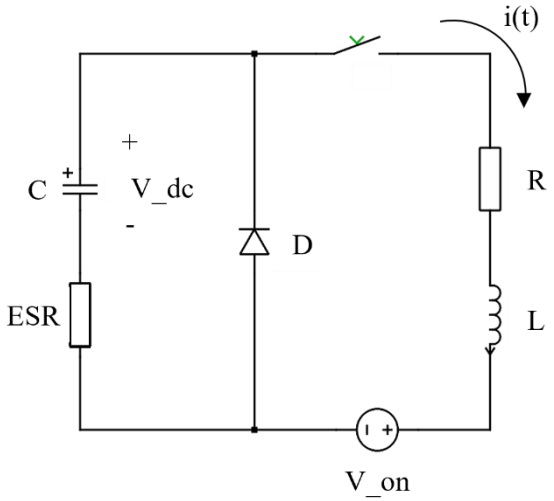


Fig. 4.1. Equivalent circuit of motor drive under proposed LC resonant capacitance estimation method [13].

For the circuit in Fig. 4.1, the following voltage relation can be derived based on Kirchhoff's voltage law (KVL),

$$V_{on} = V_c - (ESR + R) * i(t) - L * \frac{d}{dt} i(t) \tag{4.1}$$

$$i(t) = -C * \frac{dV_c}{dt} \tag{4.2}$$

where V_{on} is the on-state voltage of the switching devices of the VSI, V_c is the voltage across the DC-Link capacitor, C is the DC-Link capacitance, R and L are the phase resistance and inductance of the machine under consideration, ESR is the capacitor equivalent series resistance, and $i(t)$ is the resonant current. So (4.1) now becomes,

$$V_{on} = V_c + (ESR + R) * C \frac{dV_c}{dt} + LC * \frac{d^2 V_c}{dt^2} \tag{4.3}$$

In the case of an RLC circuit, depending on the circuit parameters there will either be an over-damped, under-damped, or critically damped response [13], [14]. Due to the inherently low inductance and capacitance values in real EV motor drive applications, the value of $(ESR + R)/L < \sqrt{1/LC}$ is typically true, which results in the under-damped response occurring. Then the capacitor voltage over time $V_c(t)$ can be solved from (4.3) under the consideration of damped oscillation [13]

$$V_c(t) = \frac{\omega_0}{\omega} V_0 e^{-\delta t} \sin(\omega t + \alpha) \tag{4.4}$$

where,

$$\omega = \sqrt{\frac{1}{LC} - \left(\frac{ESR + R}{2L}\right)^2} \tag{4.5}$$

$$\delta = \frac{ESR + R}{2L} \tag{4.6}$$

$$\alpha = \sin^{-1}\left(\frac{\omega}{\omega_0}\right) \tag{4.7}$$

by substituting (4.4) back into (4.2) the result is shown below

$$i(t) = \frac{V_0}{\omega L} e^{-\delta t} \sin(\omega t) \tag{4.8}$$

therefore, by measuring the current $i(t)$ that flows through the motor phase windings, a multivariate non-linear least squares algorithm can be used to estimate the parameters β1 = $\frac{U_0}{\omega L}$, β2 = -δ, β3 = ω to estimate the capacitance according to the following relation

$$C = \frac{\beta_1 * \beta_3}{V_0(\beta_2^2 + \beta_3^2)} \tag{4.9}$$

4.2 Consideration of Controller Sampling Frequency and Sensor Tolerance

This capacitance estimation method is highly reliant on the ability to attain accurate measurements of the resonant current, which occurs in a very short period as will be shown in this section. Therefore, to account for signal noise as well as sensor tolerance, it is important to analyze the impact that adding noise to the current signal has on the capacitance estimation accuracy. In [13], measurement and noise interference are both taken into account to validate the ability of the capacitance estimation method to perform accurate estimation in spite of undesirable conditions. However, the noise considered on the current signal was not significant with an amplitude of 1 A, and no comprehensive analysis of estimation accuracy versus sensor noise is provided. Additionally, the sampling frequency of the microcontroller has a strong impact on the estimation accuracy as it directly influences the number of current samples available for curve fitting. In motor drive applications the sampling frequency is determined by the switching frequency of the inverter, which is typically between 8-12 kHz [15]. [13] indicates that a 100 kHz sampling frequency can be used for estimation since the inverter is not in regular operation during the test. However, this elevated sampling frequency may not always be achievable in real

motor drive applications, and it may be beneficial to a system designer to understand what the minimum sampling frequency is required to provide reliable estimations. Therefore, this section aims to provide an in-depth analysis of the estimation accuracy of the LC resonance method under various levels of sensor noise and sampling frequencies to identify the system requirements in terms of current noise and sampling frequency to provide reliable estimations of capacitance. The greatest accuracy achieved from the state-of -the-art capacitance estimation methods highlighted in [4] is an estimation error of 1% or less. Therefore 1% estimation error is considered accurate enough for reliable SOH monitoring for film capacitors in this thesis.

A final consideration to take into account when adapting this estimation method to EV applications is that of the motor parameters, more specifically the motor phase resistance and inductance. These parameters of the drive under consideration have a direct impact on the duration and magnitude of the discharge current used for estimation. Modern PMSM drives are designed with very low phase resistance and inductance in order to help reduce stator copper losses as well as to limit voltage and current fluctuations due to high switching frequencies. Phase resistance can be in the milliohm range and inductance can be in the range of hundreds of microhenries [16], [17]. The impact this has on capacitance estimation is evident in Fig 4.2. In this figure, the same initial voltage and DC-Link capacitance are used. However, the phase resistance and inductance are changed to show the impact on the current waveform time duration and magnitude. The red curves represent a drive with a low power induction machine with RL values highlighted in [13]. The blue curves represent a generic low inductance PMSM. The peak magnitude of the current waveform in the case of the induction machine is only 12.1 A while it is 65.7 A for the PMSM drive in this simulation. Meanwhile, the duration of the current waveform is reduced from 6.367 ms in the case of the induction machine to only 0.816 ms for the PMSM. This large reduction in time makes it more difficult to make accurate estimations because less samples can be collected for curve fitting. If considering a 10 kHz sampling frequency, only 8 samples can be collected for the PMSM drive while 63 samples can be collected for the induction drive. Less samples make noise present on the signal more significant as well, therefore this work aims to analyze the noise and sampling influence

on the estimation abilities in a low inductance PMSM drive in order to determine the feasibility in a real EV application.

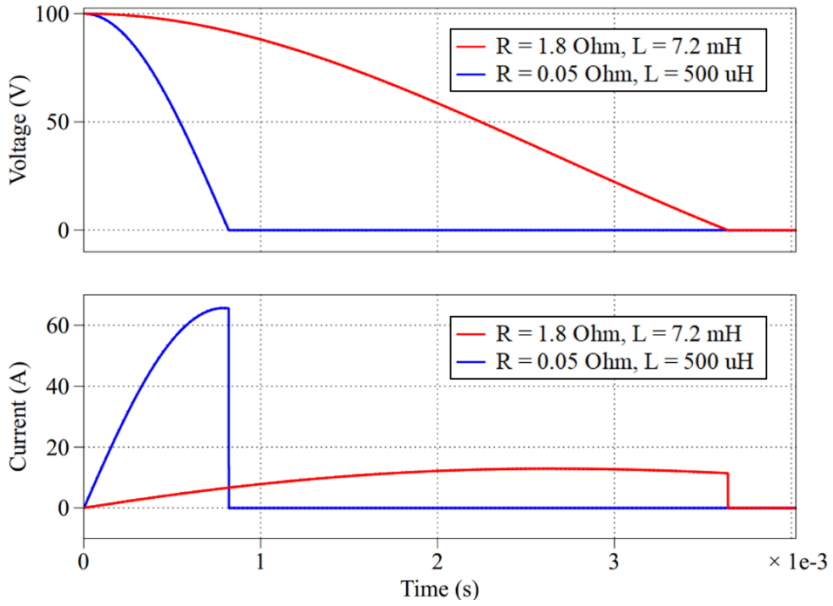


Fig. 4.2. Impact of drive parameters on duration and magnitude of current waveform used for estimation.

The simulation waveforms of current sampled at 100 kHz with 2 A of peak-to-peak noise in the low inductance PMSM drive, and the result of the exponential fit using the non-linear least squares algorithm are shown below.

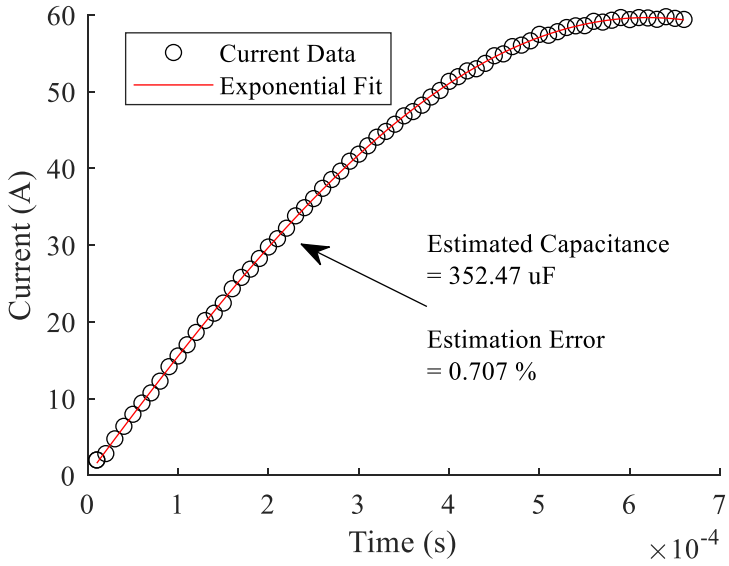


Fig. 4.3. Simulated current waveform and resulting estimation from exponential fit at 75 V initial DC voltage.

TABLE 4.1. IMPACT OF SENSOR NOISE ON ESTIMATION ACCURACY AT 100 KHZ

Current Sensor Peak-to-Peak Noise (A)	Mean Estimation (uF) 5000 Estimates	Absolute Error (%)
0	350.000	0
1.6	350.145	0.042
3	350.356	0.102
4	350.864	0.247
6	351.039	0.297
8	352.626	0.7502

TABLE 4.2. IMPACT OF SAMPLING FREQUENCY ON ESTIMATION ACCURACY WITH 8 A OF PEAK-TO-PEAK CURRENT SENSOR NOISE

MCU Sampling Frequency (kHz)	Mean Estimation (uF) 5000 Estimates	Absolute Error (%)
5	664.441	89.83
10	380.307	8.659
25	361.135	3.181
50	355.567	1.59
75	353.575	1.021
100	352.63	0.7502

TABLE 4.3. MAXIMUM ESTIMATION ERROR WITH 3 A OF PEAK-TO-PEAK SIGNAL NOISE

MCU Sampling Frequency (kHz)	Maximum Error (%)
5	755.65
10	62.33
25	27.58
50	23.62
75	24.69
100	14.06

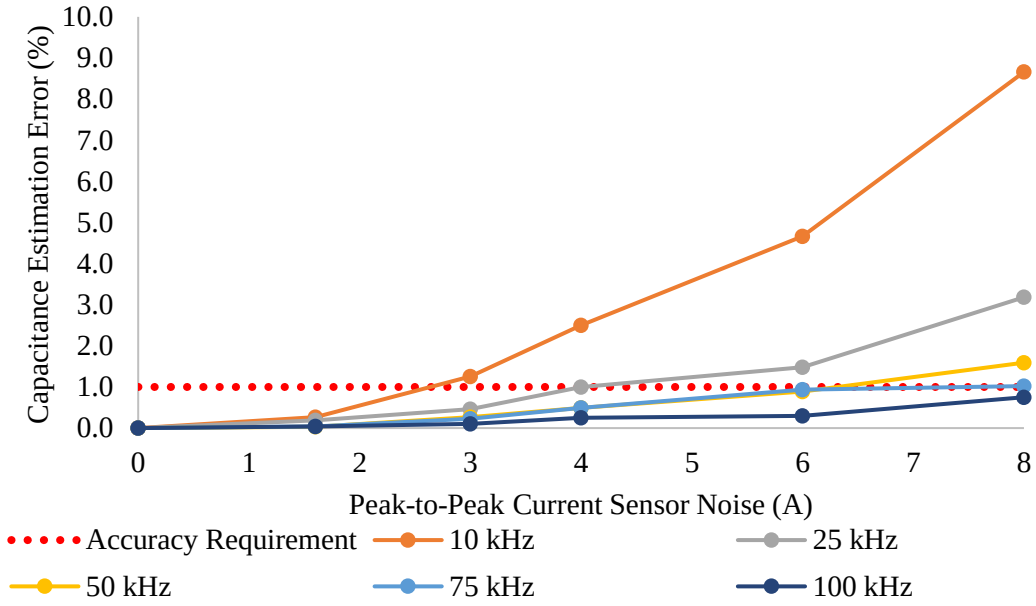


Fig. 4.4. Mean capacitance estimation error at various levels of sensor noise with different controller sampling frequencies.

Fig. 4.4 highlights the impact of signal noise on estimation accuracy in a PMSM drive by showing the mean estimation of capacitance over 5,000 estimates to remove the random bias of the white noise added to the current signal. By analyzing the simulated data in Fig. 4.4, it is clear to see that there is a clear trend between the estimation error and the level of sensor noise, as well as sampling frequency. With 8 A peak-to-peak of noise on the current signal, the mean estimation with a 100 kHz sampling frequency is 352.62 uF, which corresponds to 0.75% estimation error. As mentioned previously, the desired accuracy for reliable estimation for the film capacitor is 1%, thus with 100 kHz sampling frequency, based on the simulation results featuring these specific drive parameters, reliable estimations can still be made with up to 8 A peak-to-peak of noise present on the current signal if sufficient estimations are available. Meanwhile, with the same level of signal noise present, when the sampling frequency is reduced to 10 kHz, the estimation error shoots up to 8.66% corresponding to an estimation of 380.37 uF when the true value is 350 uF. This does not provide an accurate representation of the current SOH of the DC-Link capacitor and may lead to unsafe operating conditions or faults. With a sampling frequency of 10 kHz, and a signal noise level of only 1.6 A peak-to-peak will allow the estimation to meet the accuracy requirement of 1% according to the simulated results. As the sampling

frequency is increased to 25 kHz, the allowable noise level to maintain accuracy requirements is increased to 4 A peak-to-peak. While up to 6 A of signal noise peak-to-peak can be tolerated if the system sampling frequency is set to 50-75 kHz. From the data available in Table 4.2 and Table 4.3, it can be drawn that a minimum sampling frequency of approximately 50 kHz is required for adequate capacitance estimation as this allows for a mean estimation error of only 1.59% with 8 A of peak-to-peak noise present, and the maximum error in 5,000 estimations drops from 62% at 10 kHz to only 23.62% at 50 kHz. Therefore 50 kHz appears to provide good performance in terms of maximum deviation of estimations and mean value. However, it must be kept in mind that these error values are based on an average of 5,000 estimations in order to capture the trend of the relation between sampling frequency, sensor noise, and estimation accuracy. Table 4.3 shows the maximum error that occurred at each sampling frequency when 3 A of signal noise is present. This shows that single estimations are not reliable for accurately estimating the capacitance in a low inductance PMSM drive with signal noise even at a sampling frequency of 100 kHz. Multiple samples must be utilized to mitigate the effects of sensor noise and other external conditions which may impact the estimation. The ability to use the history of recorded estimations to make a more reliable estimation is resented in the coming sections of this chapter. Another important metric to consider is the maximum error in individual estimations that occurs at each level of signal noise and sampling frequency. Fig. 4.5 below illustrates the trend in maximum error against sampling frequency and signal noise. It is easy to see that the maximum error also increases with lower sampling and with higher signal noise. In some cases, a good mean estimation can still be made with individual estimations deviating largely from one another due to large sample sizes. However, it creates more uncertainty and less reliability in the capability of the method to accurately estimate capacitance. The simulation study shows that for a sampling frequency of 50 kHz and peak-to-peak current sensor noise of 3 A, the expected maximum error in individual estimations is approximately 24%. However, with this level of maximum error, a mean estimation error of less than 1% can still be achieved as shown previously in Fig. 4.4.

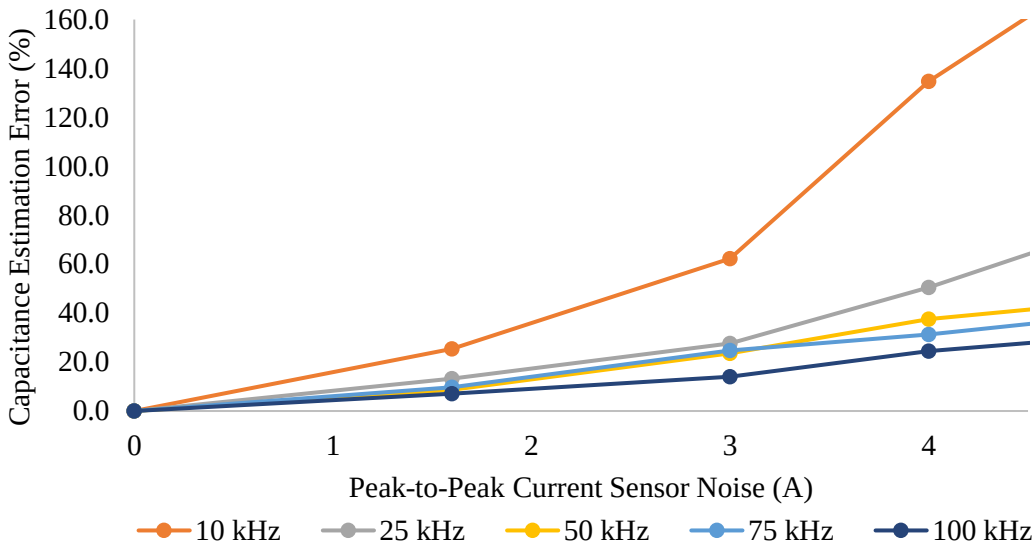


Fig. 4.5. Maximum capacitance estimation error at various levels of sensor noise with different controller sampling frequencies

This analysis provides a clear indication to system designers on the sampling frequency requirements for the capacitance estimation method to meet the accuracy requirements based on the level of signal noise they are expecting, either based on sensor tolerance indicated by datasheet information or by accurately determining the level of ripple expected on the measured signal. The capacitor discharge and capacitance estimation are performed in the experimental lab on a 100 kW IGBT based PMSM drive with a DC-Link capacitance of 350 uF to realize the estimation in a true EV drive. The estimation is performed at several sampling frequencies in order to validate the capability to perform reliable estimation at reduced sampling frequencies.

4.3 Simulation Results of Temperature Consideration

Li *et al*, [13] also mention the consideration of temperature in the estimation of capacitance, as film capacitors capacitance is dependent on ambient temperature. Although, the paper goes on to say that this test doesn't need to consider temperature because the test can be conducted at the same temperature each time since the system is in shutdown and has time to cool down first. This may not always be true, however, since in practical EV applications it is not uncommon for users to leave their vehicle parked outside during the day as well as overnight. Therefore, when the system is shut down, it will not always cool to the same temperature, but rather will cool to the current ambient temperature

in that region. Customers living in northern Alberta in the Winter surely will not experience the same ambient temperatures as someone living in southern Florida during the Summer. Changes in capacitance due to temperature may create misleading results as it may show that the capacitance has been reduced when no degradation has yet occurred. Or vice versa, the capacitance may increase due to temperature meanwhile the capacitor has truly almost reached its end-of-life, leading to failure to perform preventative maintenance before catastrophic failure occurs. Therefore, for consistent and reliable estimations the capacitance should always be estimated at a reference temperature to ensure the true level of degradation that has occurred can be identified.

As mentioned in Chapter 3, there are different materials that can be used to construct the dielectric of film capacitors, and the internal behaviours of the device are determined by the type of material. For example, film capacitors utilizing PP as the dielectric material typically see a reduction in capacitance as temperature increases, while PET and PEN capacitors typically see an increase in capacitance as temperatures increase [18]. Therefore, it is important to know the type of capacitor being used in the motor drive, as well as to know the specific behaviour of the device parameters with respect to external disturbances. The more information that is available on the DC-Link capacitor, the more accurate and reliable the capacitance estimation can become. However, in situations where there is limited information available on the DC-Link capacitor or system parameters, a generic model can still be used and provide satisfactory results.

A simple an effective strategy that can be implemented to take the impacts of ambient temperature into consideration is to use a look-up-table based approach to characterize the capacitance change in terms of temperature based on manufacturers datasheets or through experimental results. Therefore, the expected change in capacitance at any given temperature can be obtained and used to recalculate the estimated capacitance at a reference temperature. The process for the previously mentioned method is highlighted below.

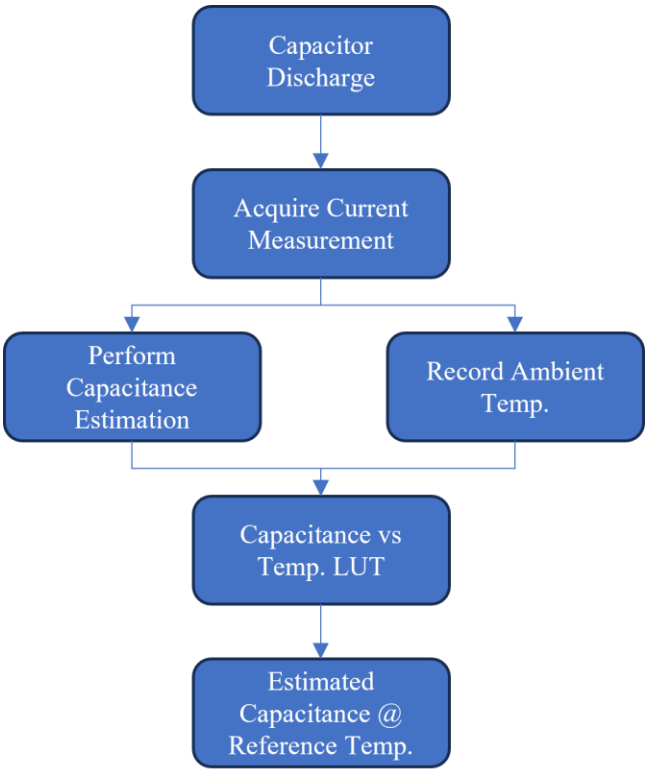


Fig. 4.6. Procedure for consideration of ambient temperature in estimating capacitance.

4.4 Simulation Results of Temperature Consideration

By inputting a changing ambient temperature into the simulation environment, and also adding some parameter dependence on temperature based on typical device behaviour, manufacturer datasheets, or from experimental results, the influence of temperature can be represented in the simulation. I have input a sinusoidally fluctuating temperature profile in order to model daily and weekly temperature changes. The influence of temperature on capacitance in the simulation study is determined by the typical capacitance change vs temperature curve given by TDK and Visay [18], [19] for PP film capacitors. This corresponds to a 1% increase in capacitance at -30˚C, and a 1% decrease in capacitance at 60˚C. The relationship between capacitance changes and temperature is illustrated in the plot below.

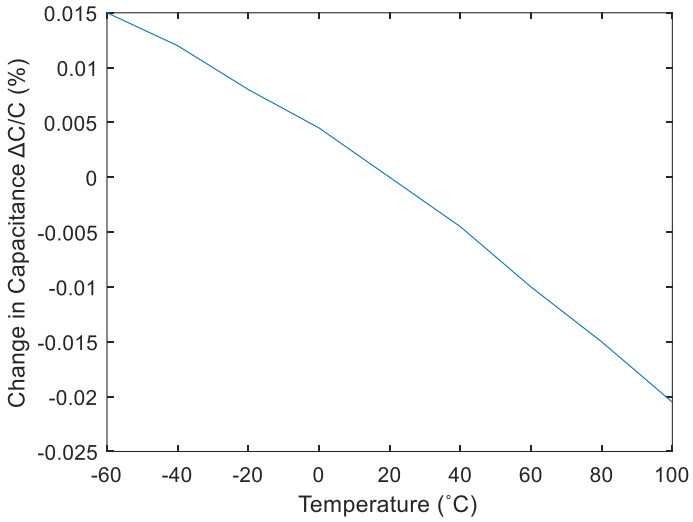


Fig. 4.7. Change in capacitance vs ambient temperature for PP film capacitor considered in the simulation.

Therefore, when considering the influence of temperature, the true capacitance value is adjusted based on the current ambient temperature. The discharge of the capacitor is performed, and the estimation of capacitance is carried out as conventionally done. However, this estimation result will correspond to the altered capacitance value due to the ambient temperature. Therefore, after the estimation is performed, the capacitance change at the measured current temperature is determined. This value of capacitance change can then be factored into the previously executed estimation in order to perform the estimation at a reference temperature of 20˚C. The improvement in estimation reliability with the consideration of temperature is highlighted below.

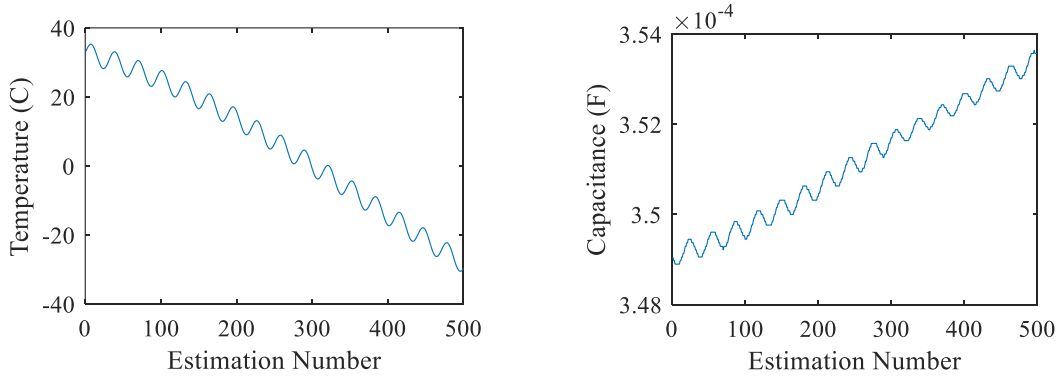


Fig. 4.8. Simulation conditions (a) Temperature profile considered in simulation. (b) Resulting change in capacitance.

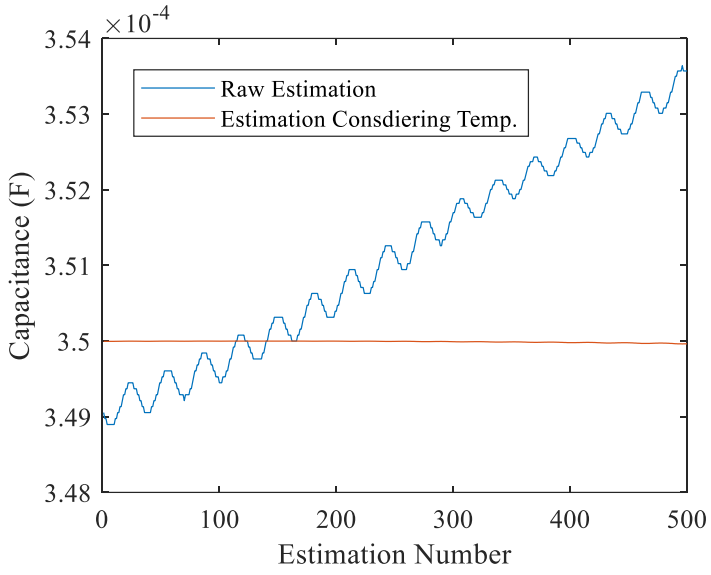


Fig. 4.9. Estimated capacitance with and without temperature consideration with no signal noise present.

When no signal noise is present on the current waveform, the estimated capacitance with and without temperature considerations is shown in Fig. 4.9. The result is that the estimations follow the changes in capacitance due to temperature which do not describe the true degradation in capacitance, and lead to a skewed mean estimation. Table 4.4 shows the mean estimation of 500 estimates with and without temperature consideration and it is clear that by considering the ambient temperature, the accuracy can be greatly improved. Although the error without temperature consideration is still below 1%, this would increase if any signal noise is present, or if more fluctuations in temperature occur.

TABLE 4.4: IMPACT OF TEMPERATURE ON ESTIMATION ACCURACY

Considering Temperature	Mean Estimation (uF) 500 Estimates	Absolute Error (%)
No	351.13	0.3324
Yes	350.08	0.0079

4.5 Curve Fitting History of Recorded Estimations

In an effort to improve the reliability of the capacitance estimation method and effectively utilize the history of recorded estimation data, instead of performing a single estimation and blindly taking that value as the true value of capacitance, the history of

estimations recorded over time can be utilized to make an improved estimation of the current capacitance and also accurately track the degradation of the capacitance over time. In [13], it is stated that the mean value of recorded estimations can be used in order to average out the error and provide an accurate estimation. However, a simple mean calculation may impact the estimation accuracy depending on the number of samples used in the calculation and depending on how much the capacitance has truly reduced over that period. For example, if the capacitance was constant for the first years of operation, but begins to degrade over the previous months, the mean calculation will not equally consider this recent degradation and will lead to inaccurate results as shown in Fig. 4.10.

Fig. 4.10 shows the individual estimations of capacitance, the yellow line represents the mean calculation of the recorded estimations, and the red line represents the true value of capacitance attempting to be estimated. It is clear that towards the end of the plot, around the 800th measurement, the true capacitance begins to decrease more rapidly. However, the mean calculation is heavily influenced by the initial 800 estimations which leads to a mean estimation far greater than the true value. The mean leads to a delayed indication of a reduction in capacitance that would lead to unreliable SOH monitoring as the system would be indicating to the user that the system is still in suitable operating condition even though this may no longer be the case.

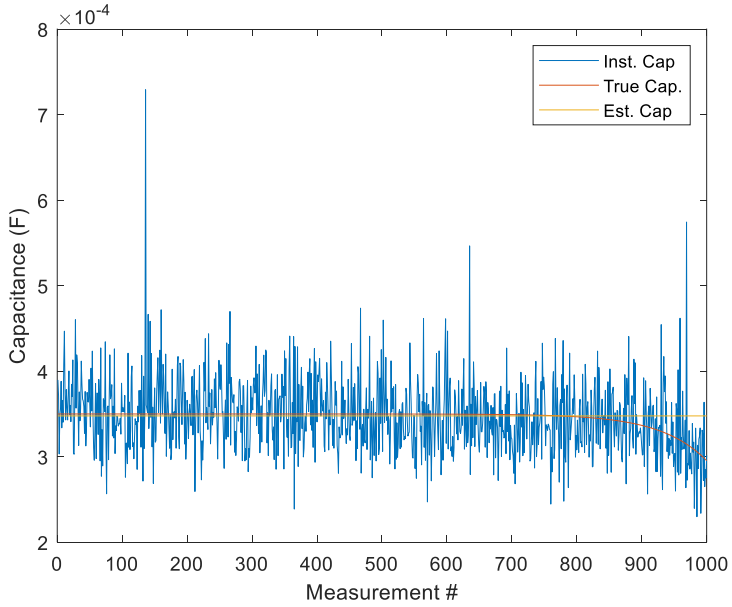


Fig. 4.10. Divergence of mean estimation from true value due to capacitor degradation.

In battery applications, it is desirable to accurately model the highly non-linear relation between the open circuit voltage (OCV) of the battery and the device state-of-charge (SOC). However, due to the complex internal chemistry within modern batteries, it is very difficult to directly model this relation. The OCV-SOC relationship can instead be mathematically modelled using various non-linear functions that are selected to well represent the nature of the OCV-SOC curve [21]. A similar approach is employed in this application to model the non-linear relationship of the capacitor's capacitance over time. Least squares estimation and non-linear mathematical functions are utilized to fit the recorded estimations to a curve resembling the degradation of a film capacitor [22]-[24]. For a system in the following vector form

$$z = Ax + n \tag{4.10}$$

where z is the output response, A is the system function, x is the parameters to be estimated, and n is system noise. If the system is in the form,

$$z = \begin{bmatrix} z(1) \\ z(2) \\ . \\ . \\ . \\ z(n) \end{bmatrix} \quad A = \begin{bmatrix} A(1) \\ A(2) \\ . \\ . \\ . \\ A(n) \end{bmatrix} \quad x = x \quad n = \begin{bmatrix} n(1) \\ n(2) \\ . \\ . \\ . \\ n(n) \end{bmatrix} \tag{4.11}$$

then, as long as the mean of the system noise is zero, the least squares estimation of the parameter x can be solved using the following relation [21].

$$x_{LS} = (A^T A)^{-1} A^T z \tag{4.12}$$

In this application, A is an array of non-linear functions selected to fit the recorded estimations of capacitance, z is the recorded estimations of capacitance, and x is the output estimation of capacitance used for SOH monitoring. The following non-linear exponential functions were used in an attempt to model the non-linear nature of film capacitors degradation.

$$A(s)^T = [1,\ e^s,\ e^{-s},\ e^{s^2},\ e^{-s^2}] \tag{4.13}$$

Using the least-squares method previously highlighted, and the non-linear functions shown in the model above, the following fit was achieved from capacitance estimation data when 3 A of peak-to-peak noise was present on the current signals.

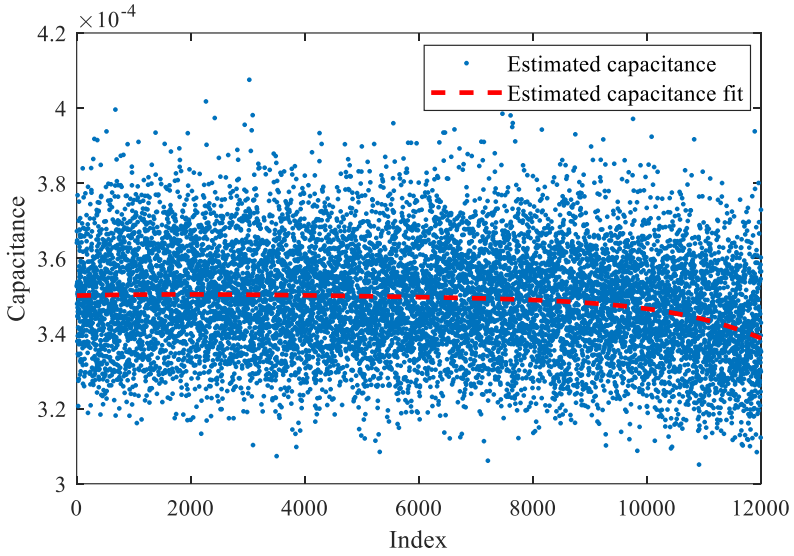


Fig. 4.11. Non-linear curve fitting of recorded estimations of capacitance over time.

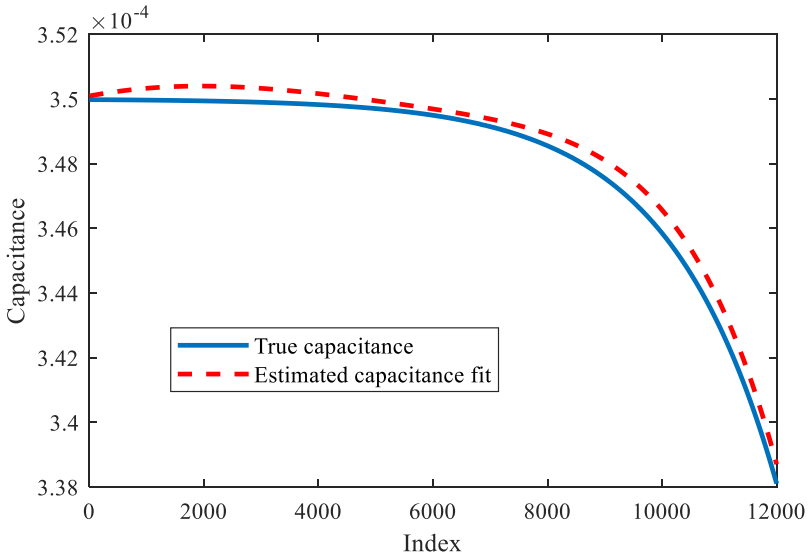


Fig. 4.12. Comparison of non-linear fit to capacitance estimation data to true value of capacitance over time.

There are several error metrics available to evaluate the ability of a given model to fit a set of data. The best fit and root mean square error (RMSE) are two strong indicators of

a model's ability to fit data and are used to evaluate the proposed model in this thesis. The plot in Fig. 4.12 has a best fit value of 83.56, and a RMSE of only 0.46 microns, indicating that the model is a very close fit to the true value.

Next, the influence of temperature consideration on the curve fitting of recorded estimations is evaluated. The maximum and minimum temperatures selected for simulation were based on historical weather data in Ontario in order to imitate a real-world scenario of a vehicle owner living in Ontario in the worst case scenarios. In Ontario, the highest and lowest recorded temperature over the last 100 years is 42.2˚C and -58.3˚C, respectively [25]. Although these values are the extreme cases of high and low temperatures, they are selected to highlight the significance of temperature consideration for capacitance estimation improvement. Therefore, the following temperature profile was used in the simulation environment.

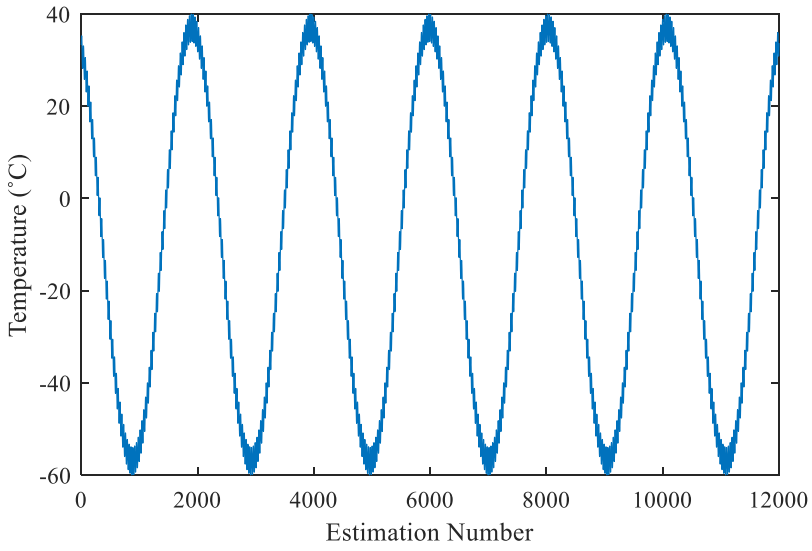


Fig. 4.13. Ambient temperature profile used in simulation based on extreme temperatures in Ontario [25].

The fluctuations in temperature will in turn cause the capacitance of the DC-Link capacitor to change, and then the estimation will attempt to measure this altered value of capacitance which does not truly reflect the level of degradation of the capacitor. This will cause all the estimations to be slightly skewed from the true value and lead to a weaker fit from the recorded estimations. However, by compensating for temperature in the individual estimations of capacitance, the final fit to the recorded estimations becomes closer to the true value, giving a strong estimation of the true capacitance for SOH monitoring. When

1.6 A of peak-to-peak noise is present on the current signal, and the temperature profile shown above is applied to the simulation, the following results were achieved when no compensation for temperature was applied to the estimation.

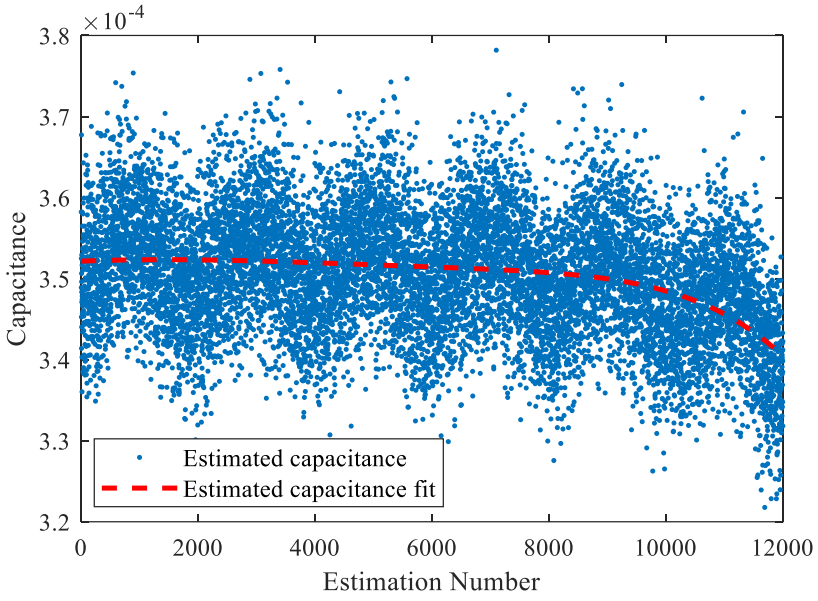


Fig. 4.14. Non-linear curve fitting of recorded estimations without temperature compensation.

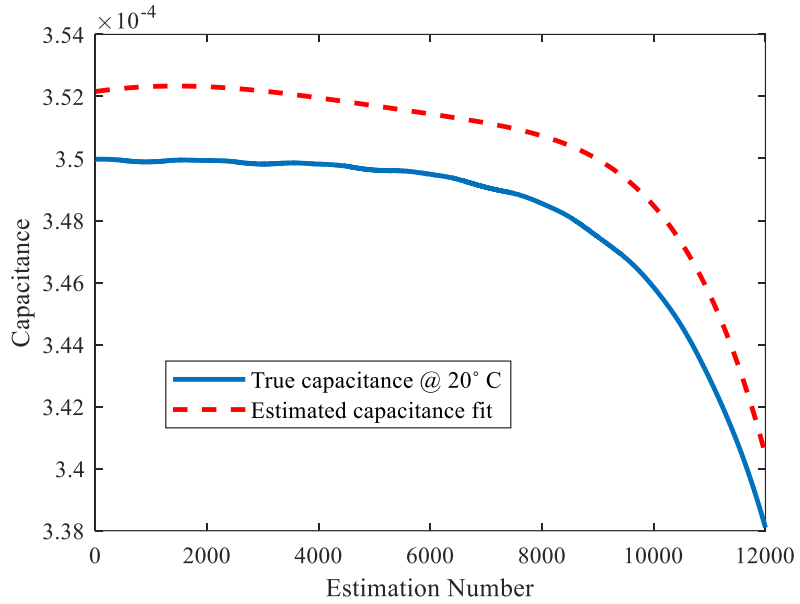


Fig. 4.15. Comparison of non-linear fit to true capacitance without temperature compensation.

The individual estimations shown in Fig. 4.14 are directly influenced by the fluctuations in temperature as it can be seen that the oscillations in the temperature profile

of Fig. 4.13 exactly match the oscillations of the individual estimations. These deviations from the true value cause the nonlinear curve fit to poorly represent the true value of capacitance as illustrated in Fig. 4.15. The improvement in individual estimations as well as the final curve fit is evident in Fig. 4.16 and 4.17.

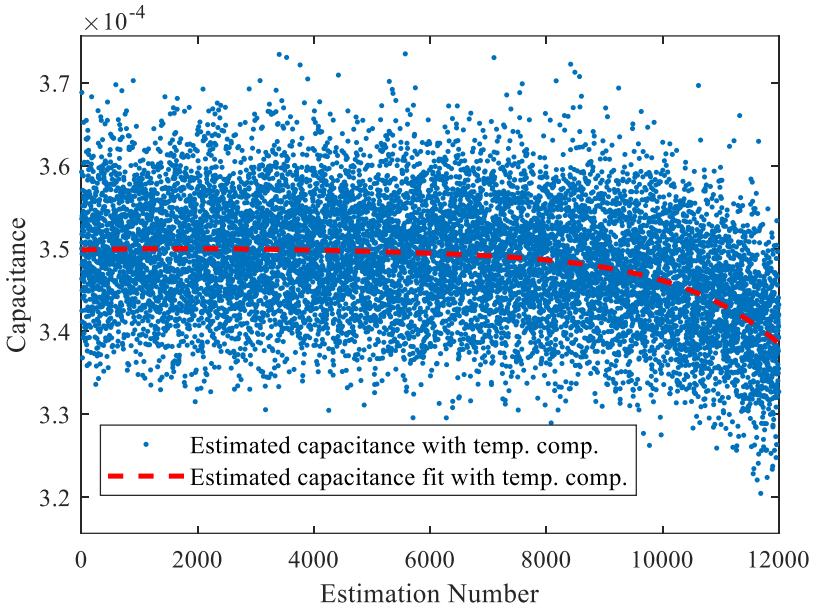


Fig. 4.16. Non-linear curve fitting of recorded estimations of capacitance with temperature compensation.

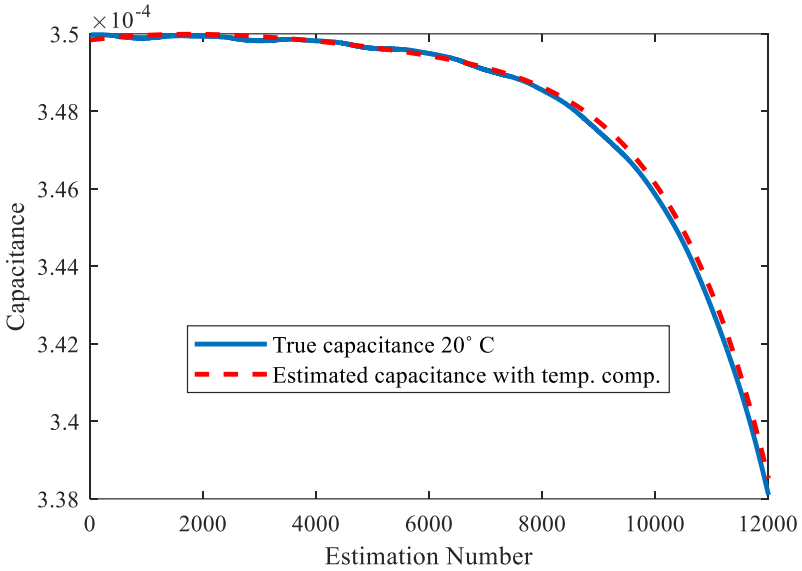


Fig. 4.17. Comparison of non-linear fit to true capacitance with temperature compensation.

TABLE 4.5: CAPACITANCE ESTIMATION CURVE FIT ERROR METRICS

Considering Temperature	BF	RMSE
No	35.797	2.31*10^-6
Yes	93.488	1.806*10^-7

TABLE 4.6: IMPACT OF TEMPERATURE ON CURVE FIT ESTIMATION ACCURACY

Considering Temperature	Estimation from fit	Absolute Error (%)
No	340.44 uF	0.689
Yes	338.53 uF	0.124

The consideration and compensation of the ambient temperature in the estimation of capacitance clearly improves the accuracy of the curve fitting of recorded estimations. In order to evaluate the accuracy with and without the consideration of temperature, the widely used best fit and root mean squared error metrics are applied to each fit, and the absolute error of the estimated value from the fit is calculated. The summary of the results can be found in Tables 4.5 and 4.6. The fit with temperature consideration has a much stronger BF value of 93.49 compared to only 35.8 without compensation. The RMSE is also reduced, and the absolute error of the estimation of capacitance was reduced from 0.689% to only 0.124%. It is also worth noting that without temperature compensation, the estimation accuracy using non-linear curve fitting is still below the required 1% accuracy mark, however adding temperature compensation just adds that much more accuracy on top of an already satisfactory system.

4.6 Motor Drive Power Loss Considerations

Since multiple discharges may be performed at each shutdown to provide a sufficient number of estimations to be used for curve fitting and this will take place over the whole lifetime of the capacitor, the power losses and energy dissipation within the system should be taken into consideration to ensure the capacitance estimation method is both practical for real implementation and safe for the long-term operation of the vehicle. As mentioned previously, the main principle behind this capacitance estimation method is to discharge

the DC-Link capacitor through the machine windings. Therefore, the power output from the capacitor will be dissipated through the copper windings mainly through heat dissipation. The power losses can be determined by the voltage and current waveforms generated from the discharging capacitor voltage. The waveforms of the capacitor voltage and current during the discharge are illustrated in the figure below.

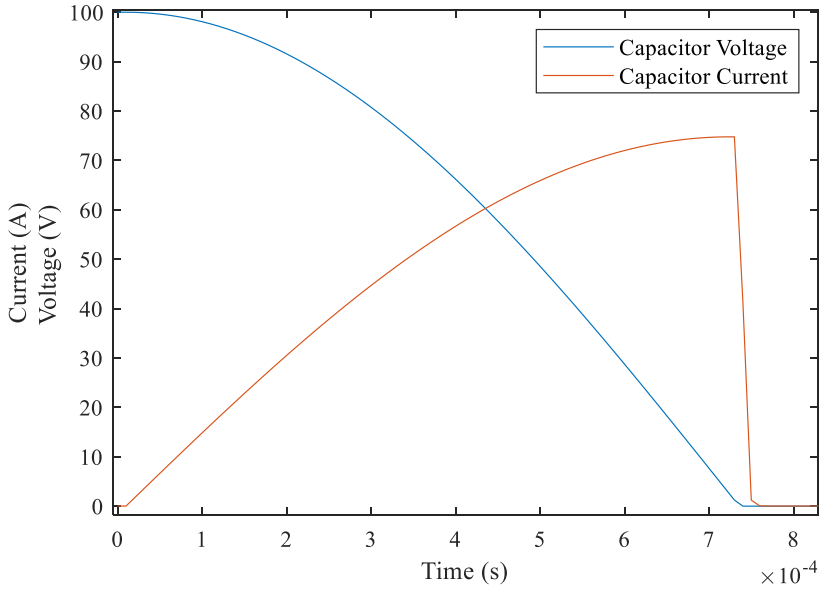


Fig. 4.18. DC-Link capacitor current and voltage discharge profile during capacitance estimation method.

With a 100 V initial voltage on the DC-Link capacitor, the peak current measured in the simulation is shown to be 74.76 A. This may seem like a significant amount of current to run through the motor. However, the motor windings of high-power electric machines used in EV applications are rated for several hundreds of amperes of continuous rms current. With the limited period of time that the current is present and the insignificant magnitude in comparison to the machines rated current, there should be no issue in executing this estimation method multiple times during every shutdown of the vehicle over its lifetime. However, more in-depth energy calculations are provided to quantitatively justify the execution of this method. Similar to the switch-on and switch-off loss calculation for a switching device, the power losses and energy dissipation of the capacitor can be determined as follows.

$$p_c(t) = v_c(i) * i_c(i) \tag{4.13}$$

$$E_c = \int_{t1}^{t2} p_c(t)\, dt \tag{4.14}$$

$$E_c = \int_{t1}^{t2} v_c(i) * i_c(i)\, dt \tag{4.15}$$

where, $p_c(t)$ is the power loss of the capacitor, $v_c(t)$ is the capacitor voltage, $i_c(t)$ is the capacitor current, and E_c is the energy dissipated by the capacitor in joules. The time t_1 and t_2 are traditionally set to the time to reach 10% of gate voltage and 2% of supply voltage respectively for IGBT switch-on loss calculations [26]. However, in this application, t_1 will represent 10% rise in $i_c(t)$, and t_2 indicates a 98% decrease in $v_c(t)$. Performing the estimation with an initial voltage of 100 V and considering the machine parameters of the PMSM considered throughout this study, the following power loss and energy dissipation profile was acquired from simulation results.

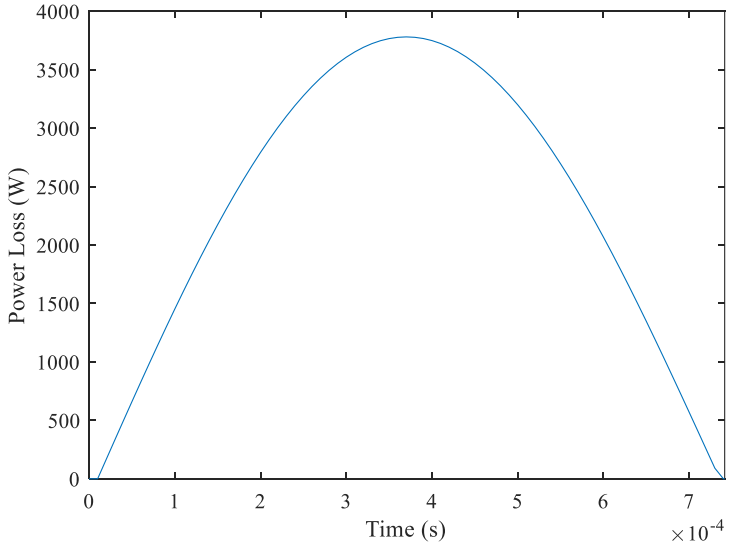


Fig. 4.19. Simulated DC-Link capacitor power loss considering 100 V initial voltage.

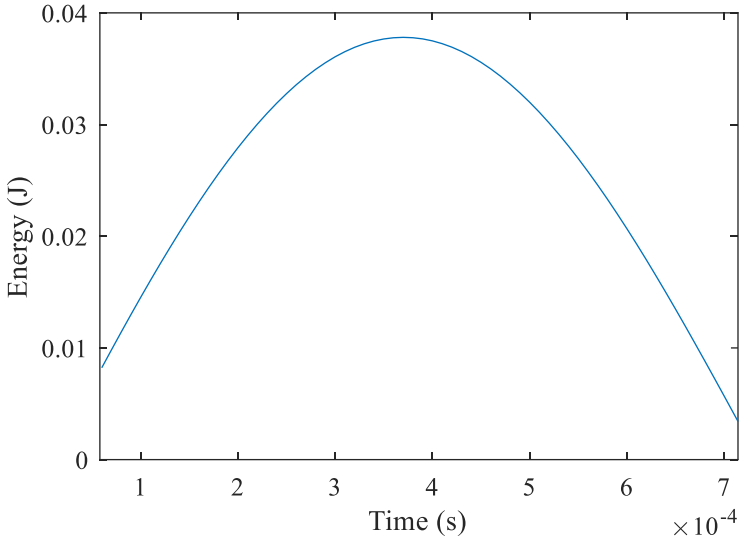


Fig. 4.20. Simulated DC-Link capacitor energy consumption considering 100 V initial voltage.

Fig. 4.19 shows that the power losses reach a peak value of 3,780 W. However, this only occurs for an extremely short period of time as the capacitor discharges very rapidly. This causes the low energy dissipation shown in Fig. 4.20, which reaches a peak value of only 0.378 J, showing that the energy consumption of this method is minimal and this method is feasible to perform over the lifetime of the EV.

4.7 Consideration of Parallel DC-Bus Capacitors

In typical EV architectures, the DC-Link capacitor is connected in parallel with the dc-bus. Several additional sub-systems within the vehicle including DC-DC converters and cooling pumps require capacitors which are similarly connected to the dc-bus. This may create an issue when attempting to perform the LC resonance discharge highlighted in section V since the DC-Link capacitor will not be the only capacitor contributing to the resonance current. This will cause the capacitance estimation method to estimate the total capacitance of the dc-bus as opposed to the capacitance of the individual DC-Link capacitor. This can lead to inaccurate estimations of the DC-Link capacitor SOH as the reduction in capacitance may be occurring in an alternate capacitor and not specifically the DC-Link capacitor. In comparison to the DC-Link capacitor, the additional capacitors have lower rated capacitance and experience reduced current stress. Therefore, it becomes

important to ensure the capacitance of the individual DC-Link capacitor is being accurately monitored for reliable drive operation.

In order to implement this capacitor SOH monitoring method in real EV applications, considerations of the practical issues facing the implementation must be addressed. Since the most important criteria to monitor is the change in capacitance and not necessarily the absolute value of capacitance, since the current stress on the previously mentioned additional capacitors is much less than the DC-Link capacitor, the overall capacitance of the DC bus can be measured, and if the total capacitance degrades by 5% this would be taken as the EOL of the DC-Link capacitor. An alternative solution to solve this issue of parallel capacitors on the dc-bus, is to utilize an online capacitor degradation model to validate the estimated capacitance of the DC-Link capacitor. When a reduction in capacitance is measured by the estimation method, the degradation calculated from the online model can be used to justify if the reduction occurred in the DC-Link capacitor or in an alternative capacitor connected to the dc-bus.

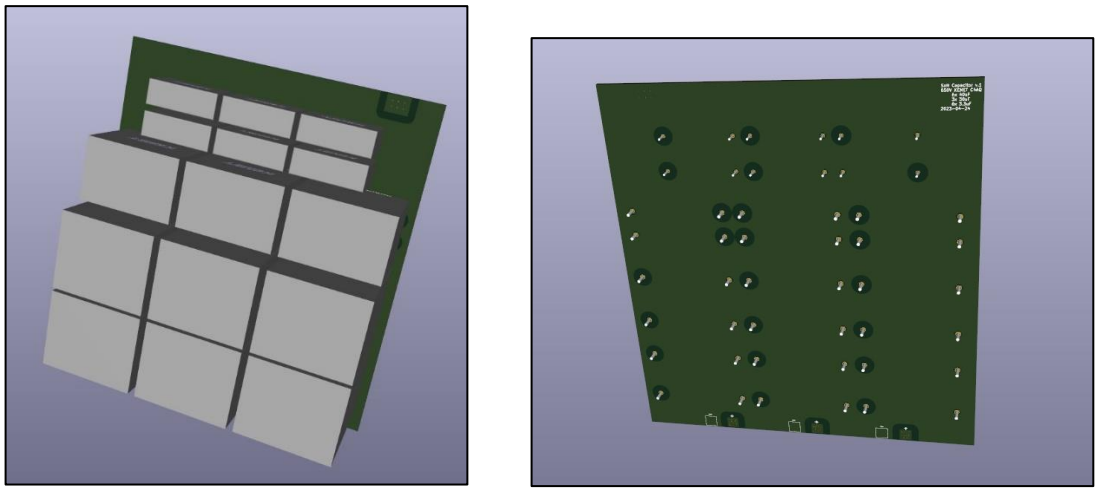
4.8 Hardware Implementation of Capacitance Estimation in PMSM Drive

In order to validate the ability to perform the estimation of DC-Link capacitance in a real electric traction drive, the parameter estimation method was performed on a drive featuring a 100 kW IPMSM, a 350 uF DC-Link film capacitor, and an IGBT based inverter. Three high precision CWT Ultra-mini Rogowski coils and a 1,500 V high-voltage differential probe were utilized with a Tektronix DPO 5034 digital oscilloscope to record and extract the required current and voltage waveforms at a sampling frequency of 1 MHz for post processing. Vector CANape software was utilized to communicate with the traction drive inverter in order to control the appropriate switches to execute the capacitor discharge through the motor windings when the predetermined initial voltage level is reached.

It is beneficial to see how effective the capacitance estimation strategy is at tracking the degradation of capacitance over time, and not just at estimating one consistent value of capacitance. However, in the case of DC-Link film capacitors the rated lifetime is typically over 100,000 hours [4], [18], [19]. Therefore, the capacitor would need to be in operation for an extremely long period of time before any noticeable degradation occurs to the value of capacitance, or some type of accelerated lifetime testing would need to take place. However, these tests require very precise operating conditions and a comprehensive

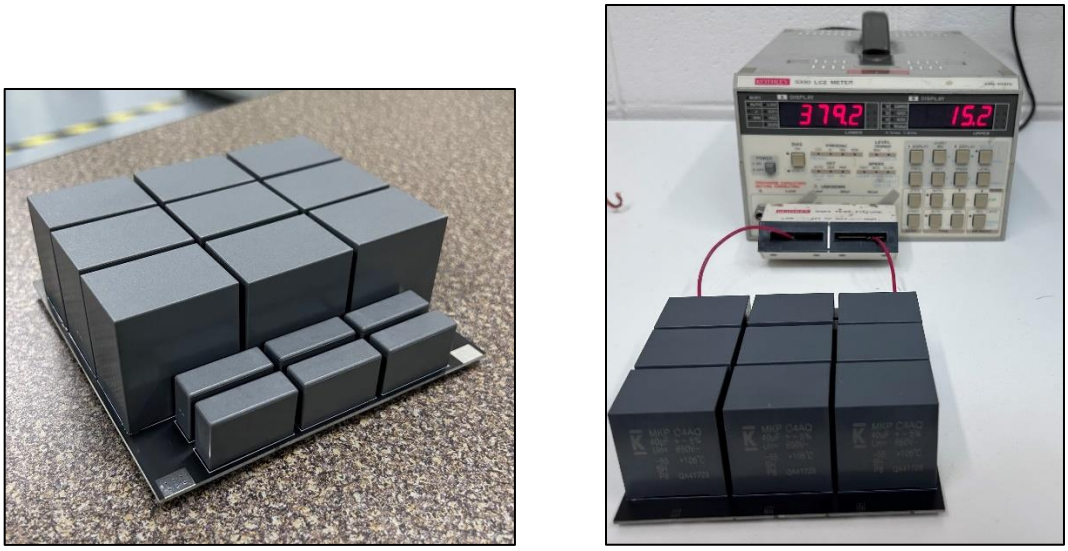
experimental setup and will still require an immense time commitment. Therefore, rather than degrading the capacitor through operation, a configurable DC-Link capacitor bank was developed in order to emulate the degradation of the capacitor over its lifetime.

A DC-Link capacitor bank with a total capacitance of 380 uF was designed for this experiment. The capacitor bank consists of 650 V Kemet film capacitors [27]. There are 6 slots for 3.3 uF film capacitors and 9 slots for 40 uF film capacitors. This allows for a steady reduction in capacitance from 380 uF to 360.2 uF in increments of 3.3 uF. This represents a 5.21% reduction in capacitance from the initial value of 380 uF. As mentioned previously in the section about the lifetime of DC-Link capacitors, the end-of-life criteria for DC-Link capacitors is a 5% reduction in capacitance, therefore the reconfigurable capacitance bank is designed to allow the capacitance estimation to be performed at each level of capacitance as the capacitor emulates reaching its end-of-life criteria in attempt to recreate the real world scenario that would occur attempting to implement this capacitance estimation method in a real EV. The initial computer-aided design (CAD) model of the reconfigurable capacitor bank and the finished product are illustrated in the following images.



(a) (b)

Fig. 4.21. Initial CAD design of PCB for configurable DC-Link capacitance bank. (a) Top view. (b) Bottom view.



(a) (b)

Fig. 4.22. Completion of DC-Link Capacitance bank (a) Soldered configurable capacitance bank (b) Validation of capacitance of bank.

The procedure for carrying out the capacitance estimation method is as follows. Initially the capacitance estimation method control must be enabled through CAN communication with the MCU of the electric drive. This control will set the appropriate duty cycle to each leg of the inverter to allow the discharge of the capacitor through phase A and returning through phases B and C when the DC-Link voltage reaches its predetermined value. When the control is enabled and a voltage trigger level has been selected, the DC-Link voltage is first charged up to a value greater than the value selected as the trigger level using a high voltage dc-supply. In this case, a TS series C79 with a maximum voltage of 600 V from Magna Power Electronics was utilized. After the voltage is brought up to an appropriate level, the HV disconnect is switched open to disconnect the HV supply from the DC-Link. When this occurs, the duty cycle setpoints have not been set yet and all switches of the inverter remain open so there is no connection to the motor. At this time, the DC-Link voltage begins to discharge slowly through a high resistance bank until it reaches the preset voltage trigger level. When the voltage trigger is reached, the inverter switches are controlled to allow the DC-Link voltage to discharge through the motor windings and the current can be measured using the inverter output phase current sensors embedded within the electric drive. For the sake of this experiment, the current was

measured using a Rogowski coil and a 1 MHz digital oscilloscope in order to achieve maximum sampling for estimation. In the real-world scenario, the current would be measured using the embedded sensors within the system, and calculations would be performed on the system MCU rather than exported to an external PC.

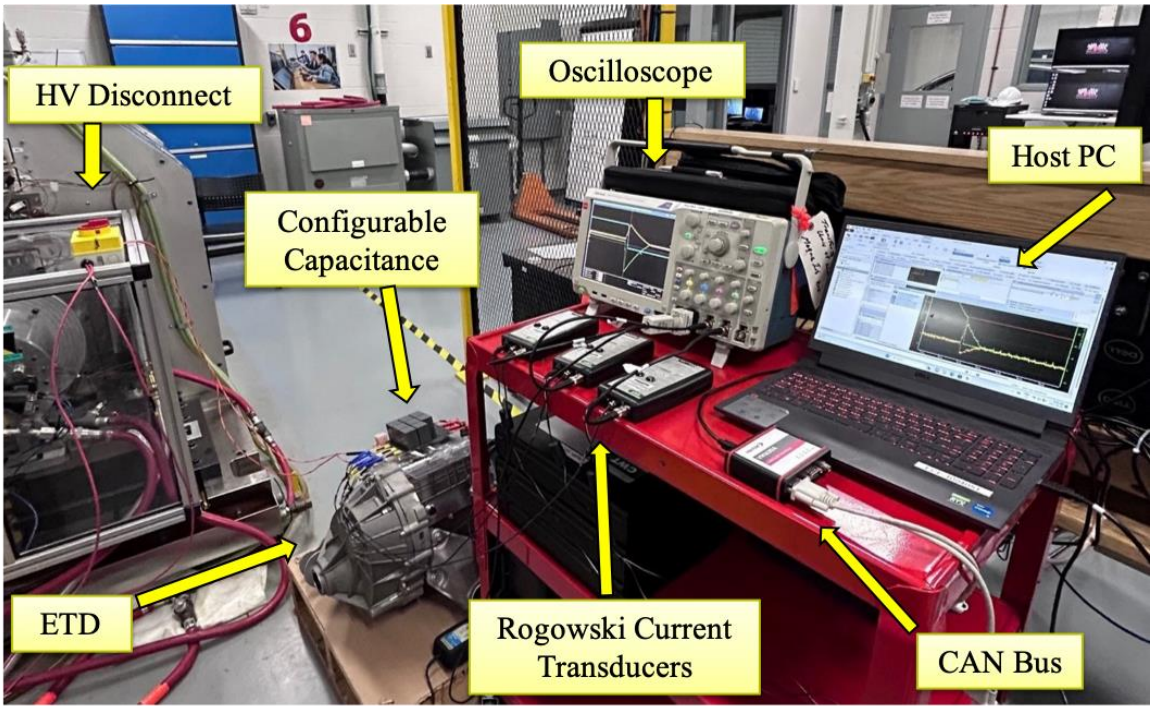


Fig. 4.23. Experimental test setup for performing DC-Link capacitor capacitance estimation.

4.9 Experimental Results

The DC-Link capacitance was estimated at various levels of capacitance in order to emulate the degradation of a film capacitor in a real-world application without having to leave the device in operation for hundreds of thousands of hours and test the ability of the estimation method to track the small incremental changes. The results can be compared with the results from the simulation study comparing sensor noise to estimation accuracy. The noise present on the current transducers utilized in the experimental setup is shown in Figure 4.22 and shows a peak-to-peak amplitude of 3.2 A. Therefore, the ability to perform accurate estimations in spite of sensor tolerance will be examined at various sampling frequencies.

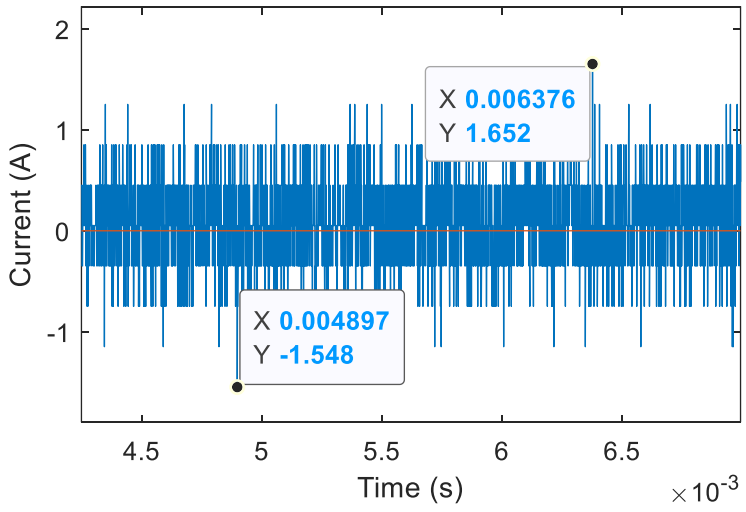


Fig. 4.24. Measured current sensor noise present in experimental setup from Fig. 4.23.

Figure 4.25 below shows that the experimental current waveform achieved closely matches the current waveform from the simulation model in terms of time duration and peak magnitude. Although the resistance and inductance of the drive in the experimental setup differed from the machines rated values, this may be due to the extra cabling used to add the configurable capacitance PCB. The estimation error with 3 A peak-to-peak noise on the current signal from experimental results achieved -0.64% from the value measured with an LCR meter.

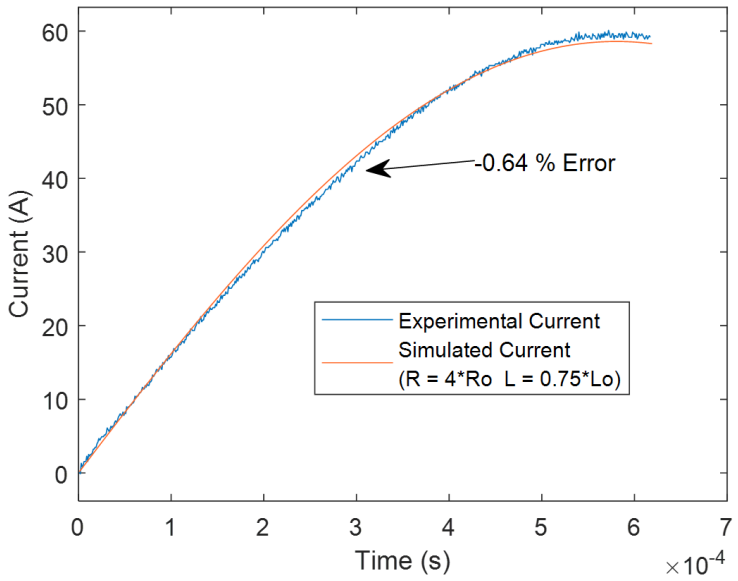


Fig. 4.25. Simulated discharge current compared with experimental results for 370 uF capacitance at 75 V.

TABLE 4.7. AVERAGE OF 5 REPEATED ESTIMATIONS AT 75 V WITH 1MHZ SAMPLING FREQUENCY

Measured Capacitance (LCR Meter) [uF]	Mean Estimation [uF]	Mean Estimation Error
383.9	382.774	-0.29%
380.58	377.023	-0.93%
377.25	370.619	-1.76%
374.05	369.638	-1.18%
370.85	374.665	1.03%
367.2	365.807	-0.46%
363.23	364.636	0.39%
341.85	344.595	0.96%
321.8	317.331	-1.39%

Table 4.7 illustrates the mean estimation of 5 measurements taken at each level of capacitance with a sampling frequency of 1 MHz. It is clear that with such a high sampling frequency, the estimation is very accurate in spite of noise present on the circuit as the average error across each level of capacitance is only -0.35%. The following figure illustrates the ability to track the degradation of the DC-Link capacitor over time.

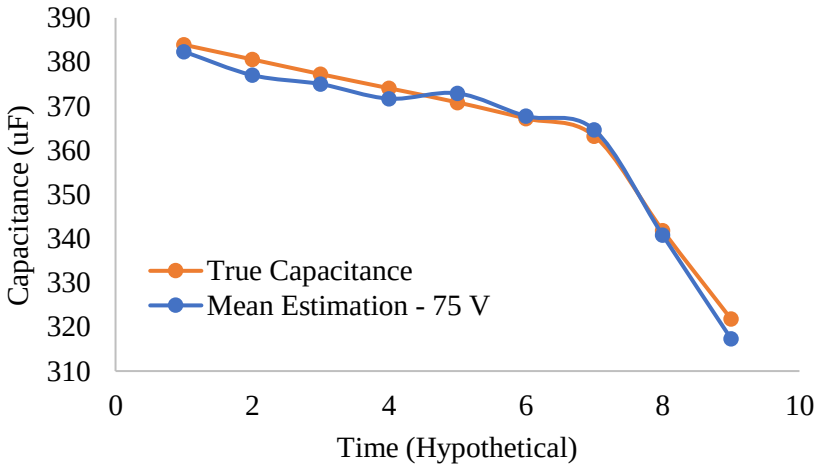


Fig. 4.26. Estimated vs measured capacitance at various levels of capacitance with 1 MHz sampling.

However, 1 MHz will rarely be available in a true EV drive application and if thousands of estimations are to be made over time this will add up to extensive amounts of data that is burdensome to the MCU. Therefore, it is beneficial to understand what is the minimum

sampling frequency that can adequately estimate the degradation of capacitance over time. Figs. 4.27 and 4.28 show how the mean estimations deviate from the measured value as the sampling frequency is reduced.

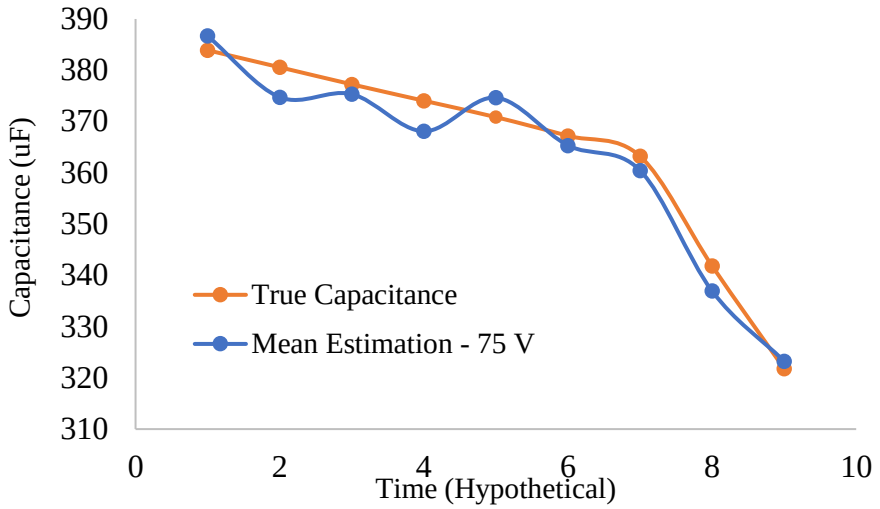


Fig. 4.27. Estimated vs measured capacitance at various levels of capacitance with 100 kHz sampling.

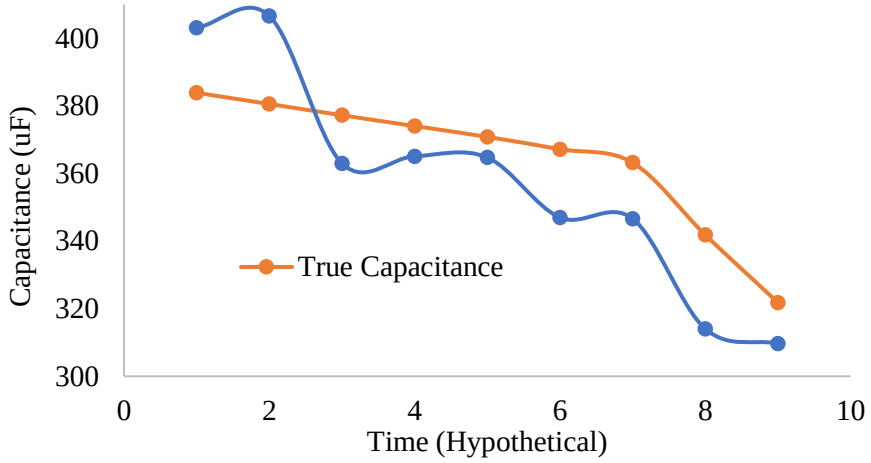


Fig. 4.28. Estimated vs measured capacitance at various levels of capacitance with 10 kHz sampling.

At 100 kHz the mean estimations are still relatively close to the true measured value and the trend of degradation is clearly followed with a maximum mean estimation error of merely -1.59%. Meanwhile, at 10 kHz deviations from the true value increase dramatically with a maximum error of -8.13% which is unacceptable for this application where very high accuracy is desired. To select an appropriate sampling frequency two conditions should be met, the maximum deviations between estimations should be limited to below 20%, indicating a maximum error of +/- 10%, and the mean estimation should be as close

to 1% or below as possible. The maximum deviations can be this high because the error of individual estimations is mitigated through averaging and curve fitting strategies as shown in the simulation studies. With this criterion set, a minimum sampling frequency for adequate estimations can be identified from the estimation results at sampling frequencies ranging from 5 – 500 kHz. The following figures illustrate the trends identified from the experimental results.

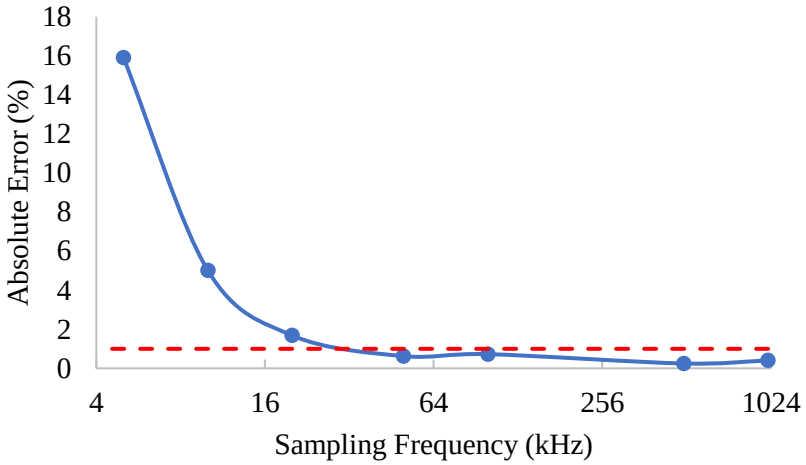


Fig. 4.29. Absolute estimation error at various sampling frequencies for 383 uF capacitance.

Figure 4.28 shows a clear indication of the influence that sampling frequency has on the estimation accuracy. This plot shows the absolute error of the mean estimation using 5 estimates of capacitance at 383 uF for sampling frequencies of 5, 10, 20, 50, 100, 500 and 1,000 kHz. The estimation accuracy falls below the desired requirement after the sampling frequency reaches 50 kHz and remains below 1% error for all exceeding sampling frequencies as shown in the plot. However, due to the random noise present on the current signal as well as the relatively small sample size of only 5, this exact trend is not followed at all 9 levels of capacitance that these tests were performed at in the experimental tests. Fig. 4.30 shows the absolute error of the mean estimation for several levels of capacitance.

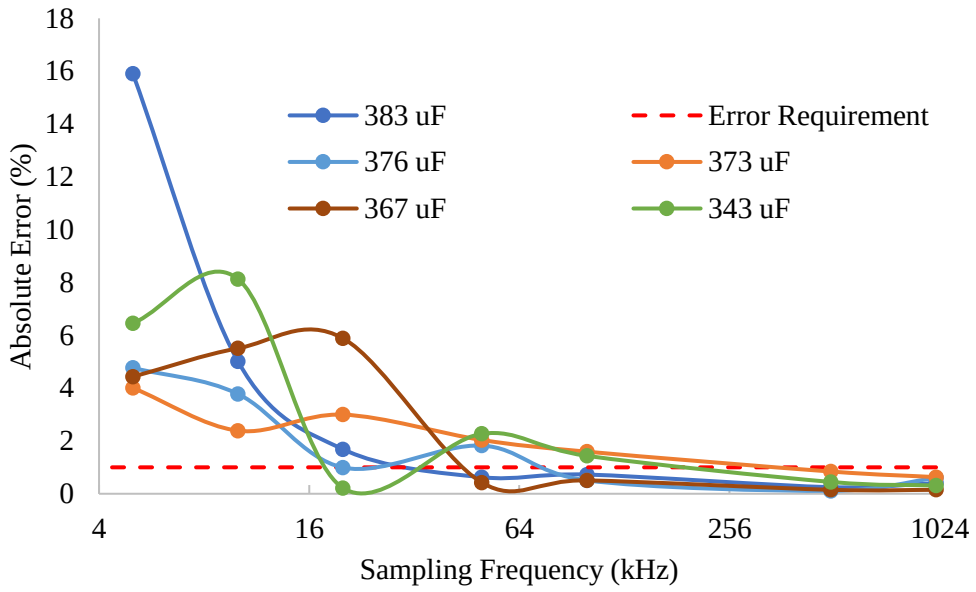


Fig. 4.30. Absolute estimation error at various sampling frequencies for various levels of capacitance.

As can be seen in Fig 4.30, the mean estimation error is not guaranteed to fall below 1% at exactly 50 kHz every time. In fact, in some cases, at 100 kHz the mean estimation falls outside of the error requirement, and a lower sampling frequency of 20 kHz was able to provide a mean estimation below the error requirements as in the case of 376 uF and 343 uF. As previously mentioned, this can be due to a small sample size used for mean estimation as well as due to the signal noise present on the current signal. However, a clearer image of the general trend followed by the mean estimation against the sampling frequency can be identified by taking the average value of the mean estimations across all tested levels of capacitance at each sampling frequency as shown in Fig. 4.31 below.

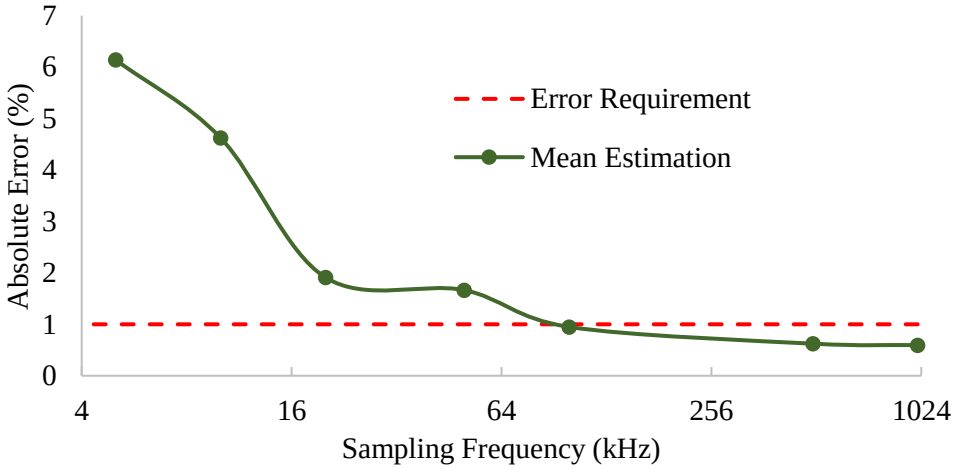


Fig. 4.31. Average absolute estimation error for all levels of capacitance at various sampling frequencies.

Figure 4.30 highlights the distinct relation between estimation accuracy and sampling frequency as more current samples allow for a better fit and higher estimation accuracy. According to the mean estimation of 5 estimations of capacitance at 9 levels of capacitance, 100 kHz sampling can ensure estimation error below 1%. However, 50 kHz still provides strong estimation accuracy with an absolute error of only 1.66%. As previously mentioned, the mean value is not the only metric of importance for this method, the maximum deviation between individual estimates is important because although very accurate mean estimations can be made at lower sampling frequencies as shown in Fig. 4.30, the likelihood of that occurring is very low if the variation in individual estimations is large. Generally, the closer the deviations in individual estimations, the more likely that the mean value will converge to the true value. Therefore, not only the mean value but also the maximum deviation between the 5 individual estimations is taken into account to determine the minimum sampling frequency required for reliable estimations.

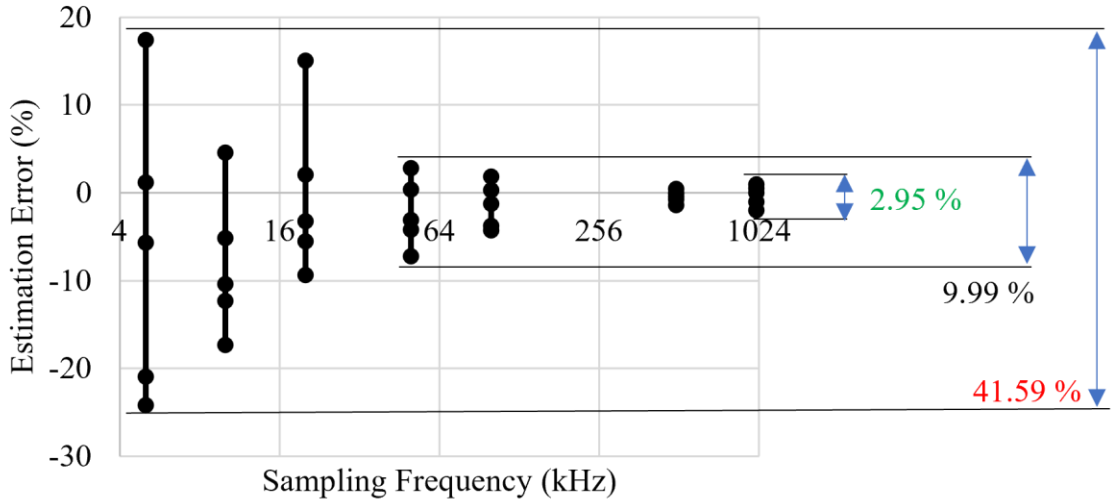


Fig. 4.32. Maximum deviation in estimations for 343 uF at various sampling frequencies.

From Fig. 4.32, it can be seen that the maximum deviation between the 5 estimates is also directly influenced by the sampling frequency. At 1 MHz a maximum deviation of only 2.95% is present, while at 5 kHz the maximum deviation between the individual estimates is 41.59%, and for 50 kHz the maximum deviation is an acceptable 9.99%. This trend is similar at all levels of capacitance and is illustrated in Fig. 4.33 which shows the average and maximum deviation between individual estimations across all levels of capacitance at each level of sampling frequency.

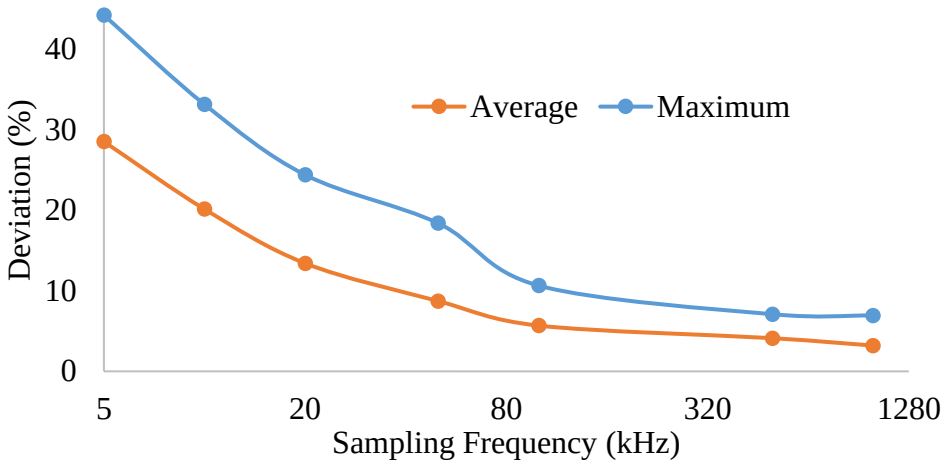


Fig. 4.33. Maximum and average deviation between estimations for 343 uF at various sampling frequencies.

The experimental results of Fig. 4.33 match well with the simulation results which found a maximum error of 24% at 50 kHz with 3 A of peak-to-peak current noise, while the experimental results found that the maximum deviation of individual estimations at 50 kHz with approximately the same level of signal noise is 18.4% with a smaller sample size.

Based on the experimental study, the results match the simulation study in identifying 50 kHz as the minimum sampling frequency required to make consistently reliably estimations in terms of both mean estimation accuracy as well as maximum deviations between estimations in a low inductance PMSM drive in the presence of current sensor noise. This information can be very useful to system designers in selecting a sampling frequency for their MCU and determining if this method would be implemented online or in some offline cloud computing methods.

4.10 References

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CHAPTER 5

DC-LINK CAPACITOR DEGRADATION MODELLING FOR EV MOTOR DRIVE APPLICATIONS

5.1 Analysis of Inverter DC-Link Capacitor Current (DCC)

Most often, the output currents of an inverter are the focus of research related to propulsion drives as it directly impacts the motor in terms of harmonic losses, torque ripple, noise, and vibrations. However, the currents on the input side of the inverter are important in the selection of a DC-Link capacitor when designing an inverter system, and in determining the impact on the lifetime of the capacitor in real operation [1]–[3]. Higher rms ripple currents through the DC-Link capacitor produce an increase in power losses, leading to elevated temperatures and a shortened lifetime. Therefore, if the DCC that flows through the system can be reduced, the lifetime of the DC-Link capacitor can be extended in motor drive applications.

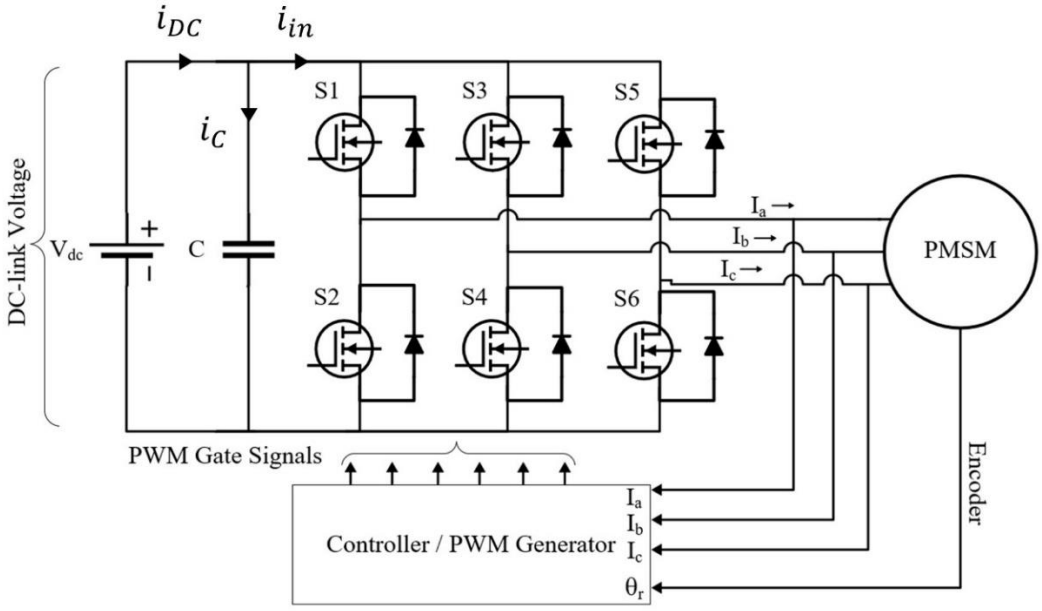

Fig. 5.1. Distribution of inverter input currents within PMSM traction drive.

At the input side of the inverter within a traction electric drive, there are three current components present as shown in Fig. 5.1. The first component is the DC current supplied from the high voltage battery i_{DC}. Next, is the current that is supplied to the inverter i_{in}. Finally, the difference between the input dc current and the inverter input current describes

the current that flows through the DC-Link capacitor. The inverter input current can be expressed in relation to the inverter switching states (s_a, s_b, s_c), and output phase currents (i_a, i_b, i_c) as in (5.1)

$$i_{in} = \sum_{a,b,c} (s_x(t) * i_x(t)) \tag{5.1}$$

where the switching states take a value of unity or zero if the switch is on or off respectively, and the phase currents are the magnitude of the output phase current. The inverter input current has two components, an average dc current supplied from the battery pack (i_{DC}), and the DCC which is a variable current which flows through the DC-Link capacitor (i_C) [4], [5]. The dc current supplied by the battery pack can be expressed as the average of the inverter input current over one sixth of the fundamental period $\left(\frac{3}{\pi}\right)$ since the input current operates at six times the frequency of the fundamental output current [5].

$$i_{DC} = i_{in_{avg}} = \frac{3}{\pi}\int_0^{\frac{3}{\pi}} \left(\sum_{k=a,b,c} \frac{t_k}{T_s} i_{in_k}(t) \right) d\theta \tag{5.2}$$

$$= \frac{3}{4} m_a * I_m cos\varphi \tag{5.3}$$

from (5.3) it is clear that the current supplied by the dc source is a function of the inverter's modulation index m_a, power factor $cos\varphi$, and the magnitude of the output phase current I_m. Finally, the DCC is determined by taking the difference between the inverter input current and the average dc current supplied by the battery pack as shown below.

$$i_c = i_{DC} - i_{in} \tag{5.4}$$

The previously highlighted analytic equations can be used to determine the front-end inverter currents in a full motor drive model. The analytically calculated inverter input current, and DCC for a given inverter output current, modulation index, and power factor are illustrated in the Fig. 5.2. This figure also demonstrates that the inverter input current

has a frequency six times as high as the fundamental frequency of the inverter output current.

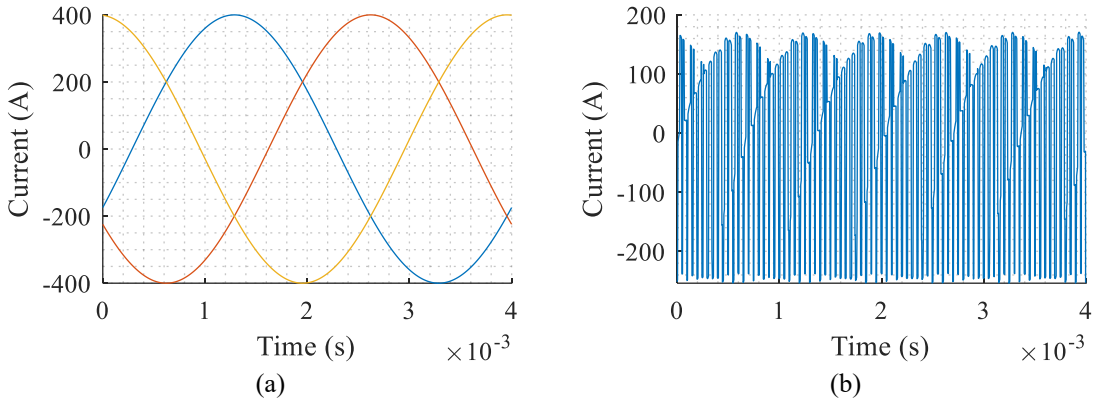

Fig. 5.2. Inverter drive currents (a) Inverter output balanced three-phase currents. (b) Calculated inverter capacitor current.

The inverter DCC can be analytically calculated or determined using a simulation model in an attempt to more accurately model the behaviour of the entire motor drive. The inverter DCC is impacted by the selected control strategy within the inverter as will be shown in a proceeding section. This thesis aims to propose a control selection strategy which reduces the DCC in certain operating regions in order to prolong the overall lifetime of the DC-Link capacitor without sacrificing the performance of the motor drive compared to conventional SVPWM control over the whole operating region.

5.2 DC-Link Capacitor Lifetime Modelling

There are several challenges present when attempting to model the degradation of DC-Link capacitors in inverter applications. Some of the major barriers include utilizing a realistic mission profile to emulate real world operating conditions for the given system, taking parameter variations over time into consideration, and also selecting an accurate lifetime model which takes into account all factors influencing the device [6]. There are generally two approaches to modelling the degradation of a DC-Link capacitor, a physics-of-failure based approach, or a data-driven approach [6]–[8]. There are also some state-of-the-art methods currently in literature which utilize both physics-of-failure as well as data-driven approaches in unison to provide a more reliable evaluation of the DC-Link capacitors SOH [9]. Several authors use Monte Carlo simulations in order to take parameter variation into account when making lifetime calculations in order to provide more realistic

estimations of RUL [9]-[13]. However, the data-driven methods require heavy computational power that can become burdensome to the MCU in some electric propulsion applications [14]–[16]. It is desirable to utilize a degradation model that can be easily implemented into the drives control architecture to allow for fast and efficient online evaluations of the DC-Link capacitors SOH.

5.2.1 Film Capacitor Lifetime Models

There has been a wide range of work completed to derive lifetime equations and to model the degradation of the DC-Link capacitor [7]-[13], [17]-[20]. As mentioned previously in Section 3.3, two of the critical stressors on the DC-Link capacitor in a traction electric drive are voltage stress and thermal stress. Understandably, voltage stress is caused by the applied voltage in relation to the rated voltage of the device. For film capacitors, voltage stress is expressed using an inverse power law [6]. Thermal stress is induced by the device power losses due to ripple current as well as due to heat propagation from other nearby devices [21]. Therefore, it is critical to model the voltage stress and thermal stress in the lifetime model for the DC-Link capacitor. The empirical model for the lifetime of capacitors is given below.

$$L = L_0 \left(\frac{V}{V_0}\right)^{-p_1} * e^{\left[\left(\frac{E_a}{K_B}\right)*\left(\frac{1}{T_h}-\frac{1}{T_o}\right)\right]} \tag{5.5}$$

where, L is the lifetime of the capacitor in hours, L_0 is the rated lifetime given by the manufacturer datasheet, V is the applied voltage, V_0 is the rated voltage, T_0 is the rated temperature, T_h is the capacitor hotspot temperature at operating conditions, and both are expressed in Kelvin [17]. p_1 is the voltage stress parameter, E_a is the activation energy, and K_b is Boltzmann's constant ($8.62e^{-5}eV/K$). Thus, p_1 and E_a are required to be determined for the specific device to provide accurate modelling. However, it can be difficult to determine E_a in some applications and it is not readily available from manufacturer datasheets. Thus, in [22] a simplified form of equation (5.5) shown above is derived for a specific case of activation energy and considering the highest useable temperature for an electrolytic capacitor (125℃) using the Arrhenius model [1], [18], [22], [23]. The Arrhenius model states that the lifetime of the device is divided by a factor of 2

for every 10℃ rise in temperature from rated conditions. The derivation from [17] is carried out as shown below.

$$L = L_0 \left(\frac{V}{V_0}\right)^{-p_1} * e^{\left[\left(\frac{E_a}{K_B}\right)*\left(\frac{1}{T_h}-\frac{1}{T_o}\right)\right]}$$

$$L = L_0 \left(\frac{V}{V_0}\right)^{-p_1} * e^{\left[\left(\frac{E_a}{K_B}\right)*\left(\frac{T_o-T_h}{T_o*T_h}\right)\right]}$$

then, according to the 10℃ rule of the Arrhenius model,

$$L = L_0 \left(\frac{V}{V_0}\right)^{-p_1} * e^{\left[\left(\frac{E_a}{K_B}\right)*\left(\frac{1}{T_o*T_h}\right)*\left(\frac{T_o-T_h}{10}\right)\right]}$$

$$L = L_0 \left(\frac{V}{V_0}\right)^{-p_1} * e^{\left[\left(\frac{0.94\ eV}{8.62e^{-5}eV/K}\right)*\left(\frac{1}{398\ K}\right)^2*\left(\frac{T_o-T_h}{10}\right)\right]}$$

$$L = L_0 \left(\frac{V}{V_0}\right)^{-p_1} * e^{\left[ln2*\left(\frac{T_o-T_h}{10}\right)\right]}$$

thus, the widely accepted lifetime model for film capacitors is given by the following analytic expression.

$$L = L_0 \left(\frac{V}{V_0}\right)^{-p_1} * 2^{\frac{T_0-T_h}{p_2}} \tag{5.5}$$

where, p_1 and p_2 are the voltage stress and temperature stress parameters respectively. These parameters are dependent on the internal characteristics of the capacitor and are unique for different devices. For film capacitors, the temperature stress parameter typically assumes a value of 10, while the voltage stress parameter varies from 5–12 depending on the structure and materials present in the device [20], [24], [25]. When developing a degradation model for a specific system, these parameters should be correlated to the exact device in the system for the most accurate results. However, for a general degradation model and for comparative studies, the mean value of the voltage stress component, 8.2, can be used. There are additional improved lifetime models which take into account the effects of humidity and or voltage harmonics on the lifetime calculation [1], [10], [19], [20], [25], [26]. Due to the extremely thin layer of metallized film present in film capacitors, corrosion occurs when the film is exposed to moisture, making film capacitors

more susceptible to the impacts of humidity. The impact on the lifetime of the device can be described by incorporating the following term in the lifetime equation.

$$L = L_0 \left(\frac{V}{V_0}\right)^{-p_1} * \left(\frac{RH}{RH_0}\right)^{-p_3} * 2^{\frac{T_0 - T_h}{p_2}} \tag{5.6}$$

where, RH is the relative humidity at operating conditions and RH_0 is the relative humidity at rated conditions. in the case of EV drives the capacitor is commonly in an air-sealed housing However, as previously mentioned in chapter 3, in the case of electric traction drives the DC-Link capacitor and inverter are housed within a metal case to create a rigid structure which also reduces EMI according to the IEC standards [27]. This drastically reduces the effects of humidity on the DC-Link capacitor and therefore, the inclusion of humidity into the lifetime calculation is not considered in this thesis.

There is also work that highlights that the previously discussed constant lifetime model can be improved by considering the aging of the capacitor ESR over time [10], [11], [19]. As the capacitor degrades, the capacitance reduces and the ESR increases, leading to increased power losses and in turn faster degradation. Therefore, an improved lifetime estimation method is proposed in which an ESR aging model is applied to consider the ESR drift over its lifetime for more accurate reliability assessment for the DC-Link capacitor. An additional improved lifetime model was proposed specifically for supercapacitors, very high-density electrolytic capacitors, in [28]. This method was inspired by the degradation of the supercapacitor under voltage step testing which found that degradation occurred slowly until a certain voltage was reached at which point the degradation occurred rapidly. The form of the proposed model is shown in (5.7).

$$L = L_0 * \max\left(\left[2 - e^{-p_1(V_0 - V)}\right], 0\right) * 2^{\frac{T_0 - T_h}{p_2}} \tag{5.7}$$

Another known lifetime model applied to film capacitors is originally developed in [29] and more recently applied in [30]. This model utilizes the conventional lifetime model but has additionally takes into account the effects of voltage harmonics on the capacitor lifetime. Three additional terms are included to the lifetime equation as shown in (5.8).

$$L = L_0 \left(\frac{V}{V_0}\right)^{-p_1} * 2^{\frac{T_0 - T_h}{p_2}} * K_{rms}^a K_p^b K_f^c \tag{5.8}$$

These additional terms include the RMS coefficient K_{rms}, the peak coefficient K_p, and the harmonic coefficient K_f. The exponents $a, b,$ and c represent the degree of influence of each parameter on the capacitor lifetime and are different for every capacitor depending on the materials, configuration and manufacturer of the device [30]. Therefore, the inclusion of these parameters again requires detailed knowledge of the specific capacitor under study and often requires extensive lifetime testing or must be provided by the manufacturer. Additionally, the DC voltage in the case of the EV drive is provided by a battery pack and requires no rectification which limits the amount of harmonic content greatly. Consideration of an improved lifetime model, changing load profile, and an aging ESR model can give an increasingly accurate and reliable assessment of capacitor SOH in comparison to the constant load constant lifetime model. However, in order to properly model the aging of the capacitor ESR and utilize improved lifetime models, knowledge of the given capacitor's initial aging rate, and temperature and voltage coefficients for the specific device are required, which entails detailed knowledge of the capacitor materials and performance from accelerated lifetime tests [10].

The voltage applied to the capacitor can be easily measured from the available sensors within the traction drive as DC-Link voltage is conventionally readily available within the drives control system via high voltage sensors on the DC-Link. However, the capacitor hotspot temperature is not as easy to determine since there are no thermocouples, or alternative temperature sensors, present on the capacitor, and there is no current sensor for the DC-Link capacitor in a conventional motor drive. Therefore, it is necessary to determine the current passing through the device using analytic modelling of the system in consideration, or through a simulation model, and use a thermal network of the DC-Link capacitor to gain an understanding of the device's internal temperature during regular operation.

5.2.2 Film Capacitor Thermal Modelling

An effective strategy to model the thermal behaviour of an electrical component is to utilize a lumped parameter RC thermal network [31]. RC thermal networks are determined based on the thermal impedance of a given device. The network is composed of various thermal resistances and capacitances which describe the changes in temperature at different junctions of the device based on the devices power losses. There are two types of RC

thermal networks commonly applied, the thermal Cauer model, and the thermal Foster model [32], [33]. Cauer models are able to depict the physical internal structure of a given device and can thus provide detailed information regarding the temperature of a certain material or location within a device. However, to develop a Cauer model extensive knowledge of the materials and construction of the device is required and it is computationally complex to implement in practice. Meanwhile, Foster models provide a more direct measurement of the internal temperature based on a behavioral model whose parameters can be extracted from the manufacturer datasheet or can be determined experimentally. The equivalent circuit the thermal network models are highlighted below.

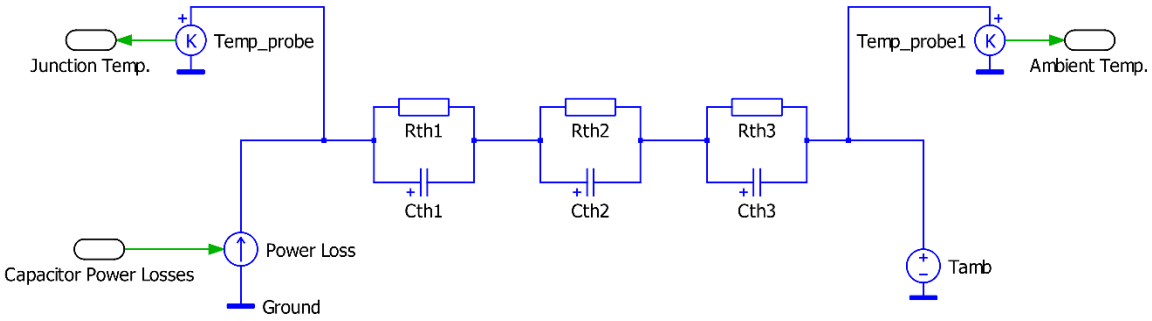

Fig. 5.3. Structure of 3rd order thermal Foster network.

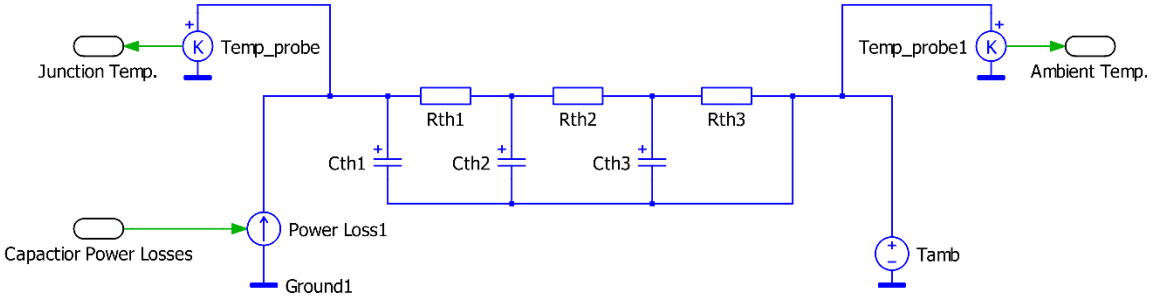

Fig. 5.4. Structure of 3rd order thermal Cauer network.

As shown in Fig 5.4, the input to the thermal network is heat in the form of power losses. The power losses of the capacitor are influenced by the ripple current through the device and are determined according to the following equation previously presented in Chapter 3.

$$P_{cap} = \sum_{i=1}^{n} \left[ESR(f_i) * {I_{cap}}^2_{RMS}(f_i) \right] \tag{5.9}$$

The capacitor power losses are dependent on the ripple current content as well as the ESR of the device. When the power losses for the device have been determined for a given operating condition, they are then input to the thermal model. The thermal resistances present in the network will determine the temperature that the junction under consideration will reach, while the thermal capacitances in the network will determine how fast the device will reach this temperature. In the case of this thesis, due to its simplicity and effectiveness, as well as the desire only to understand the capacitors core temperature and not understand the temperature at each layer, a 2nd order Foster-type thermal network is utilized to emulate the thermal behaviour of the DC-Link capacitor. The mathematical relation for converting the device power losses to junction temperature in a foster thermal network is highlighted below [32], [33].

$$T_{hs} = P_{cap} \sum_{i=1}^{n} R_i \left(1 - e^{-\frac{t}{R_i C_i}} \right) \tag{5.10}$$

where, T_{hs} is the hot-spot temperature of the device, R_i is the thermal resistance, C_i is the thermal capacitance, t is the time spent in the loading condition, and n is the number of elements considered in the foster model.

5.2.3 Damage Accumulation and Condition Monitoring

After the thermal network is derived and validated against the true characteristics of the device under study, it can be implemented into a reliability model for the capacitor for an accurate prediction of device temperature. The device's hot-spot temperature and applied voltage can be utilized to make lifetime calculations according to (5.8). From there, to take multiple loading conditions into consideration and determine the accumulated degradation over time, a commonly used method is to utilize the Miner's rule [34] – [36]. Miner's rule uses a linear relationship to express the accumulation of damage over time based on the individual operating conditions and the time spent in that condition. The formula to determine the damage accumulated from one operating condition is shown below.

$$D = \frac{t_i}{L_i} \tag{5.11}$$

where, D is the degradation, L_i is the calculated lifetime from (5.9), and t_i is the time spent in that operating condition. As mentioned previously in Chapter 3 and 4, the end-of-life criterion for the film capacitor is a 5% reduction in capacitance. Unfortunately, there are no well-known models to accurately depict the exponential increasing loss of capacitance over its lifetime. Therefore, when the capacitance is in the range of 0%-5% degradation, it can be approximated by a linear model [10], [19]. Thus, the capacitance loss due to an individual operating condition is expressed as follows,

$$\Delta C(t) = \frac{t_i}{L_i} * 5\%\ C_0 \tag{5.12}$$

where, ΔC is the change in capacitance, and C_o is the initial or rated capacitance. The next step is to consider multiple operating conditions to emulate real world operating scenarios for an EV for an improved reliability analysis. By dividing the total operating time into several time periods, each corresponding to a certain loading condition of the electric drive (torque, speed), the total damage accumulated can be calculated using a summation of the previously highlighted relationship.

$$\Delta C(n) = \sum_{i=1}^{n} \frac{t_i}{L_i} * 5\%\ C_0 \tag{5.13}$$

There has been an abundance of research conducted analyzing the reliability of DC-Link capacitors in various applications using the previously highlighted principles in which the voltage and thermal behavior of the DC-Link capacitor is used to make lifetime calculations, [8], [12], [35]-[38]. In [35] an accelerated testing method for DC-Link capacitors in a photovoltaic (PV) inverter system is developed which uses a variable load profile known as a mission-profile in order to evaluate the lifetime of the capacitor as opposed to using the traditional constant stress accelerated testing. In [38], the reliability of the DC-Link capacitor in a metro traction drive system is evaluated using a multiple time scale-based approach in which the passenger mass, slope, acceleration and speed are

all taken into account and damage accumulation is calculated for a single trip, a full day, and over the total lifetime of the system. In [37], the lifetime equations for electrolytic and film capacitors are utilized to determine the lifetime of a capacitor bank in a wind power converter based on a mission-profile with wind speed and ambient temperature information. [12] takes a similar approach to capacitor reliability monitoring and applies it to the IGBT switching devices in a railway propulsion inverter. [36] developed a health-oriented control strategy designed to extend the life of the DC-Link capacitor in a wind turbine inverter system. An analytic relation to determine the current harmonic spectrum of the DC-Link capacitor was established, and an improved ESR model which takes into account frequency and temperature was utilized for more accurate power losses. The outcome of the study was that the carrier phase shift angle of the PWM control can be adjusted to reduce the harmonic content of the ripple current in the capacitor, and thus reduce power consumption and improve overall lifetime. In [8], a capacitor lifetime model which also considers power module faults within electric traction drives is proposed to further improve the existing lifetime model.

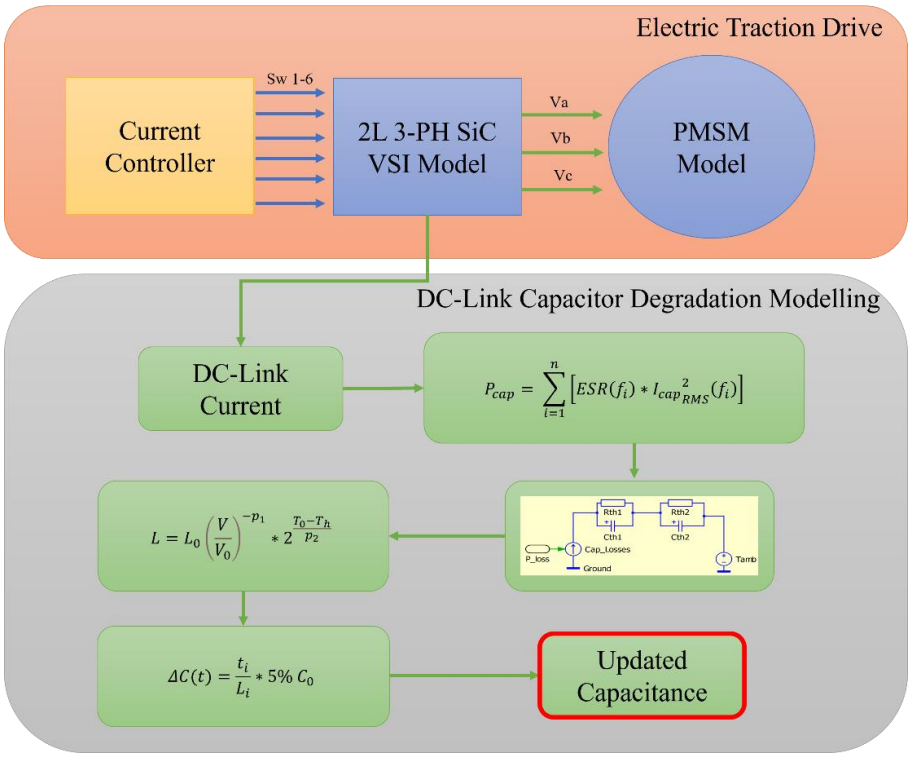

Fig. 5.5. Framework for conventional capacitance degradation modelling in PMSM drive.

A flowchart for the proposed DC-Link capacitor degradation modelling for a PMSM electric traction drive used in the simulation study in the proceeding Chapter of this thesis, and which can be used as a generic framework for future researchers where the lifetime model shown can be replaced with any of the previously presented improved lifetime models, is illustrated in Fig. 5.5. This framework can be used in parallel with the capacitance estimation method presented in Chapter 4 in order to provide increased reliability in condition monitoring by providing multiple estimations of the current level of capacitance, one from the parameter estimation, and one from the accumulation of damage based on loading conditions. When either of the readings of capacitance reaches the EOL criteria of 5% degradation, preventative maintenance should take place on the capacitor.

5.3 References

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CHAPTER 6

HIGH PERFORMANCE PWM SELECTION STRATEGY FOR IMPROVED CAPACITOR LIFETIME

The selected PWM strategy, DC-Link voltage, and inverter switching frequency all have a heavy influence on the output performance of the traction drive in terms of power losses and phase current quality [1]. Furthermore, it has been shown that the DC-Link capacitor current is also impacted by the selection of modulation strategy employed in the drive [2], [3]. Therefore, depending on the desired objectives for a given application, the PWM strategy can be selected to provide enhanced operation with respect to the critical performance criteria.

As the most prone to failure component within the motor drive, the extension of the DC-Link capacitor lifetime is imperative to prolong the lifetime of EVs and ensure safe and reliable operation during that lifetime. Therefore, this chapter aims to develop a PWM selection strategy with the intent of increasing the capacitor lifetime without significant sacrifice in output performance in terms of switching losses and output current quality by reducing the DCC in operating regions that provide an acceptable tradeoff between the DCC and the motor drive performance. A DC-Link capacitor health-oriented control strategy for wind turbine converter applications is developed in [2] with the goal of establishing a connection between the systems mission profile, selected control strategy, and the DC-Link capacitor lifetime. However, this strategy is developed specifically for the wind turbine converter system and considers a front and back-side converter. The core temperature of the DC-Link capacitor was reduced through the alteration of the PWM carrier phase angle to cancel the even-order carrier harmonics of both the front and back side converters and proposed that the service life of the capacitor could be increased from 3.65 years to 57.5 years in the given application. In [3], another PWM selection criterion for a high-performance drive with reduced CMV and DCC is proposed. However, this selection method does not provide a direct quantitative criterion to determine when it is desirable to reduce DCC but rather only highlights which PWM method should be selected if reduced DCC is desired. This chapter aims to develop a cost function which can be utilized to determine the optimal operating regions to select DCC reducing PWM methods

in order to maintain the high performance of the drive in terms of switching losses and output current quality, which directly impacts machine side losses of the motor drive system [1], while also extending the service life of the DC-Link capacitor.

6.1 DCC Reducing PWM Control Methods

The selection of voltage space vectors during a fundamental period directly impacts the inverter input current and in turn impacts the fluctuation and rms value of DC-Link current [4]. As mentioned previously in Chapter 2, in SVPWM there are six active vectors and two zero vectors available in a two-level three-phase inverter. When the zero vector is utilized, the three phases of the inverter are shorted to either the positive or negative rail of the DC-Link. This causes the inverter input current to fluctuate between the magnitude of output phase current, and zero amps [5]. Thus, the use of the zero vector causes the largest fluctuation in inverter input current and in turn causes the largest ripple current through the capacitor. This ripple current is responsible for the power losses and internal heating of the capacitor that eventually cause the device to reach its end-of-life criteria. The fluctuation on inverter input current and DCC under SVPWM is highlighted below.

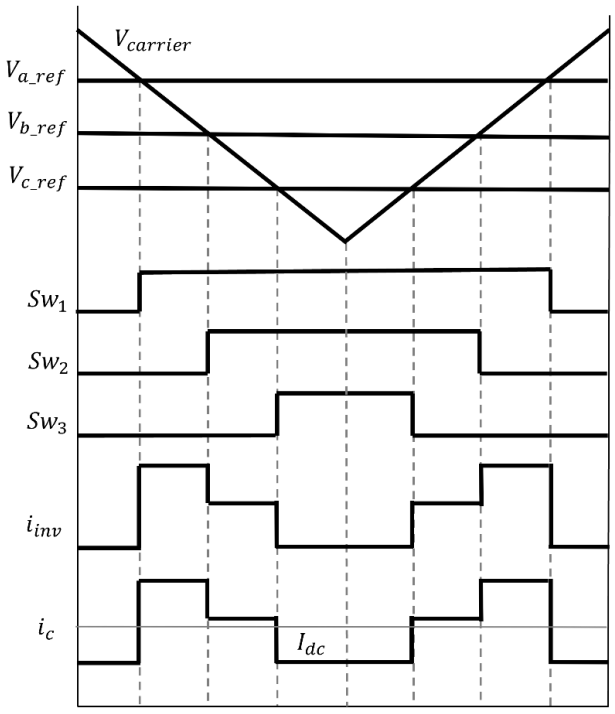


Fig. 6.1. Influence of SVPWM switching states on inverter input and DC-Link capacitor current. .

The use of the zero vectors is present in conventional PWM methods, such as SPWM and SVPWM, and is responsible for their poor performance in terms of DCC. Therefore, the main concept behind capacitor current reducing PWM methods is to avoid the use of zero vectors in the production of the output reference vector. There are PWM methods designed with the intention of reducing DCC proposed in literature [5]-[8], each posing potential benefits and drawbacks to the performance of the inverter. [6] proposes a carrier-based continuous PWM method to reduce the current stress on the DC-Link capacitor. This is accomplished by shifting the voltage reference vectors halfway through each switching period. This results in a lower fluctuation of inverter input current which in turn reduces the DCC. However, this method does not reduce switching losses in the inverter, increases the output phase current THD, and has an intricate LUT based calculation to perform the shifting of voltage references during a fundamental period. In [5], a novel PWM method is proposed to simultaneously reduce the inverter switching losses and rms capacitor current using a second triangle carrier wave utilized with the switching functions of SVPWM. However, this method is only applicable when the modulation index is greater than 0.77 and is therefore unsuitable for motor drive applications.

An extension of this PWM method was proposed in [7] to improve its operational range. Ext-DCPWM also implements a double carrier wave. However, this method uses the switching signals of DPWM1 or DDT-GDPWM depending on the system operating conditions. This method allows for operation across the entire operating range and therefore could be considered for motor drive applications. The multi-carrier GDPWM (MC-GDPWM) method is proposed in [8]. This PWM method utilizes the switching signals of DDT-GDPWM method, which minimizes the inverter switching losses at all operating points by alternating between the 4 DPWM variants. But, unlike DD-GDPWM, MC-GDPWM uses double carrier signals in order to further reduce the inverter DCC through the avoidance of zero-state voltage vector utilization. The difference between MC-GDPWM and Ext-GDPWM is that MC-GDPWM only uses the double carrier signal depending on the operating conditions of the inverters three-phase voltages and currents. The MC-GDPWM method provides the largest reduction in DCC across the entire range of modulation index and power factors, while also minimizing switching losses [9].

Due to the high performance of MC-GDPWM in reducing switching losses and DCC, along with the straightforward implementation of MC-GDPWM presented in [8], MC-GDPWM is selected to be used in the PWM selection method proposed in this thesis along with conventional SVPWM.

6.2 Development of PWM Selection Cost Function

As the most prominent and widely adopted PWM strategy within EV motor drives [10], [11], SVPWM is taken as the benchmark for motor drive performance in terms of switching losses and output current THD. Therefore, the performance of the DCC reducing MC-GDPWM method is compared to SVPWM in order to identify possible areas for improvement among the most critical inverter performance metrics. A cost function is developed which considers the level of THD in the output phase currents, inverter switching losses, and the DCC. The cost function F_{cost} is a function of output phase current THD I_{THD}, total inverter switching losses P_{sw}, and RMS inverter DCC I_{DCC} and is formulated as shown below.

$$F_{cost}(I_{THD}, P_{sw}, I_{DCC}) = X_{THD} + X_{Sw-loss} + X_{DCC}$$

where, X_n is the percentage change of each performance metric (THD, Switching Loss, DCC) in MC-GDPWM compared to SVPWM calculated simply as follows,

$$X_n = \frac{(SVPWM_n - MCGDPWM_n)}{SVPWM_n}$$

This cost function is designed to provide an equivalent comparison of the key performance metrics of the motor drive at a certain operating point under different PWM control strategies. In this application the PWM strategies considered are SVPWM and MC-GDPWM because the main goal is to extend the lifetime of the DC-Link capacitor, however this cost function can be applied to any alterative PWM strategy and the considered performance metrics can be altered to match the desired application. For example, if common-mode voltage (CMV) reduction is the main concern, a CMV reducing PWM method such as AZSPWM or TSPWM [12] may be considered instead of MC-GDPWM, and the inverter CMV change compared to SVPWM will be considered in the cost function as opposed to DCC. Thus, this thesis provides a simple but effective framework for

developing PWM selection strategies using a drive-cycle based analysis and an adaptable cost function. The procedure for developing and executing this cost function can be adapted by system designers to a variety of applications in the future.

The beauty of this simple cost function is the ability to adjust the weight of any distinct parameter in order to prioritize a certain performance metric for a given application. For example, if a VSI with next generation switching devices is utilized and switching losses no longer become a serious concern due to the low power loss devices, the focus on phase current THD can be enhanced by increasing the weight of the THD term in the cost function and re-evaluating the PWM selection map across the torque speed region. Furthermore, additional terms may be included in the cost function to incorporate the effects of time into the PWM selection strategy. This can be useful in the case of designing a capacitor health oriented PWM selection strategy. As mentioned previously in Chapter 3, the DC-Link capacitor faces inevitable degradation due to self-healing and other internal reactions caused by the harsh thermal and electrical operating conditions. So, near the end of the capacitor's useful life it experiences increased power losses due to the aging of ESR [13], [14] and rapid degradation begins to occur. In order to combat this process, the weight of the DCC parameter in the cost function can be increased near the end of the capacitor lifetime, to increase the focus of the PWM selection strategy on reducing the DCC.

6.3 Simulation Framework for EV Motor Drive

A full electric motor drive including a three-phase two-level VSI with SiC switching devices, 360 V DC-Link source, 350 uF DC-Link capacitor, current controller, and a 100 kW IPMSM is required to be modelled and simulated using simulation software in order to analyze the impacts of various PWM methods on inverter switching losses, output current THD and also DCC. PLECS power electronic simulation software was utilized for this task in this thesis. PLECS allows for simple yet effective calculation of switching and conduction losses for individual switching devices using a multidimensional LUT based approach as shown in the figures below. The LUT data can be supplied from Manufacturer datasheets or determined experimentally for a more accurate representation. Some specific devices even have ready to import thermal loss models for the device which makes importing the LUT data quick and easy.

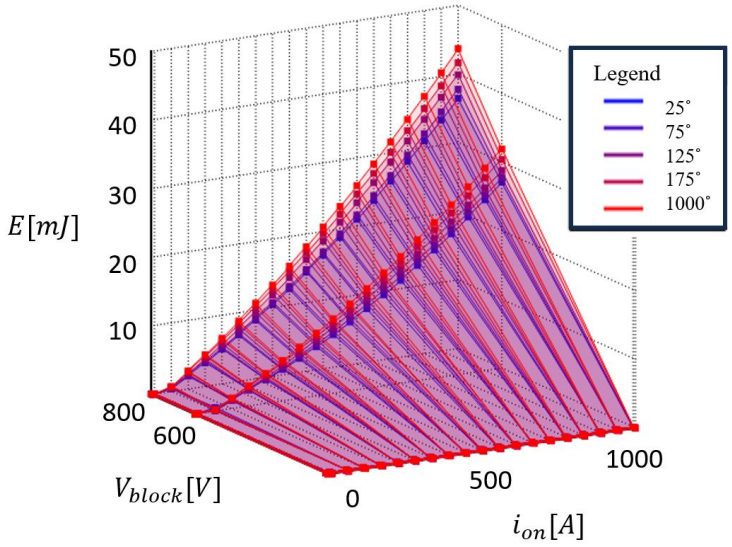


Fig. 6.2. Switching loss three-dimensional LUT utilized in PLECS.

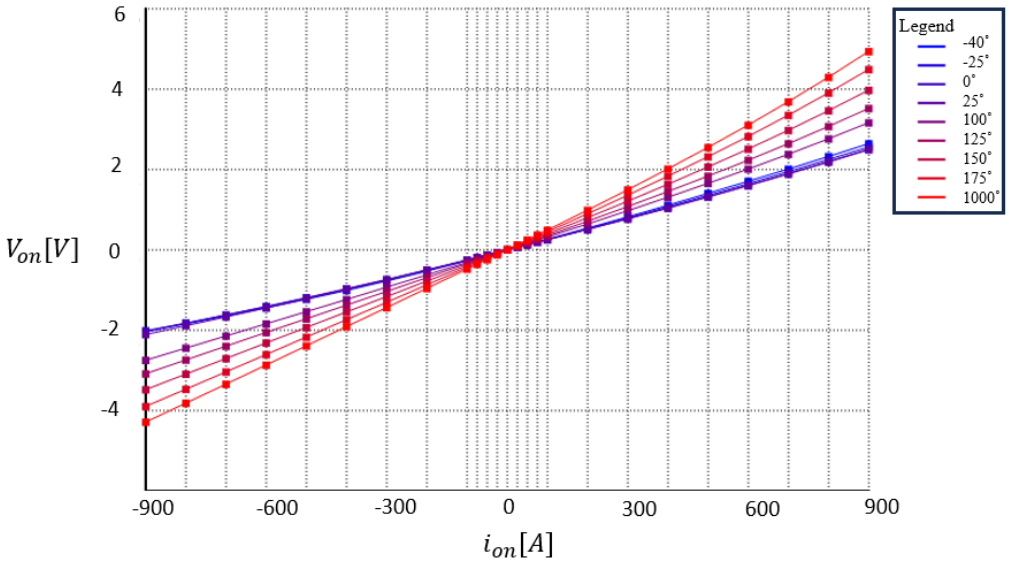


Fig. 6.3. Conduction loss two-dimensional LUT utilized in PLECS.

The various pulse width modulation strategies are implemented in PLECS according to the principles highlighted in the previous sections regarding SVPWM and MC-GDPWM. Commands of d and q-axis current are input to the model, along with the desired motor speed in rpm. The current controller uses PI controllers in order to mitigate the error between the current measured at the motor terminals and the commanded value and provide the proper output. The output of the current controller is 6 gate signals to be delivered to the 2-level 3-phase VSI modelled with SiC MOSFETS in order to control the output power

delivered to the machine. The operating conditions of the simulated traction drive and machine parameters are shown in Table 6.1.

TABLE 6.1. SIMULATION PARAMETERS FOR ELECTRIC DRIVE USED FOR PWM COMPARISON.

DC-Link Voltage	360 V
Switching Frequency	10 kHz
Switching Devices	SiC MOSFET
Electric Machine Type	IPMSM
Rated Power	100 kW
Base Speed	3,000 rpm
Maximum Speed	9,500 rpm

During the simulation, the SiC MOSFET switching, and conduction losses are calculated using the LUTs and operating conditions of the drive, and the output phase current THD is calculated using an inbuilt PLECS block. The DCC is measured using a simple current measurement block, and input into the degradation model which was highlighted in Chapter 5. The flowchart depicting the simulation framework for this study is illustrated below.

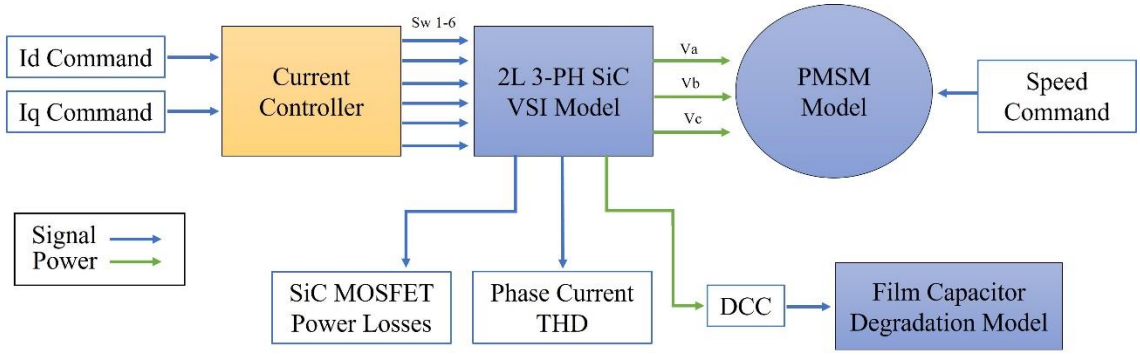


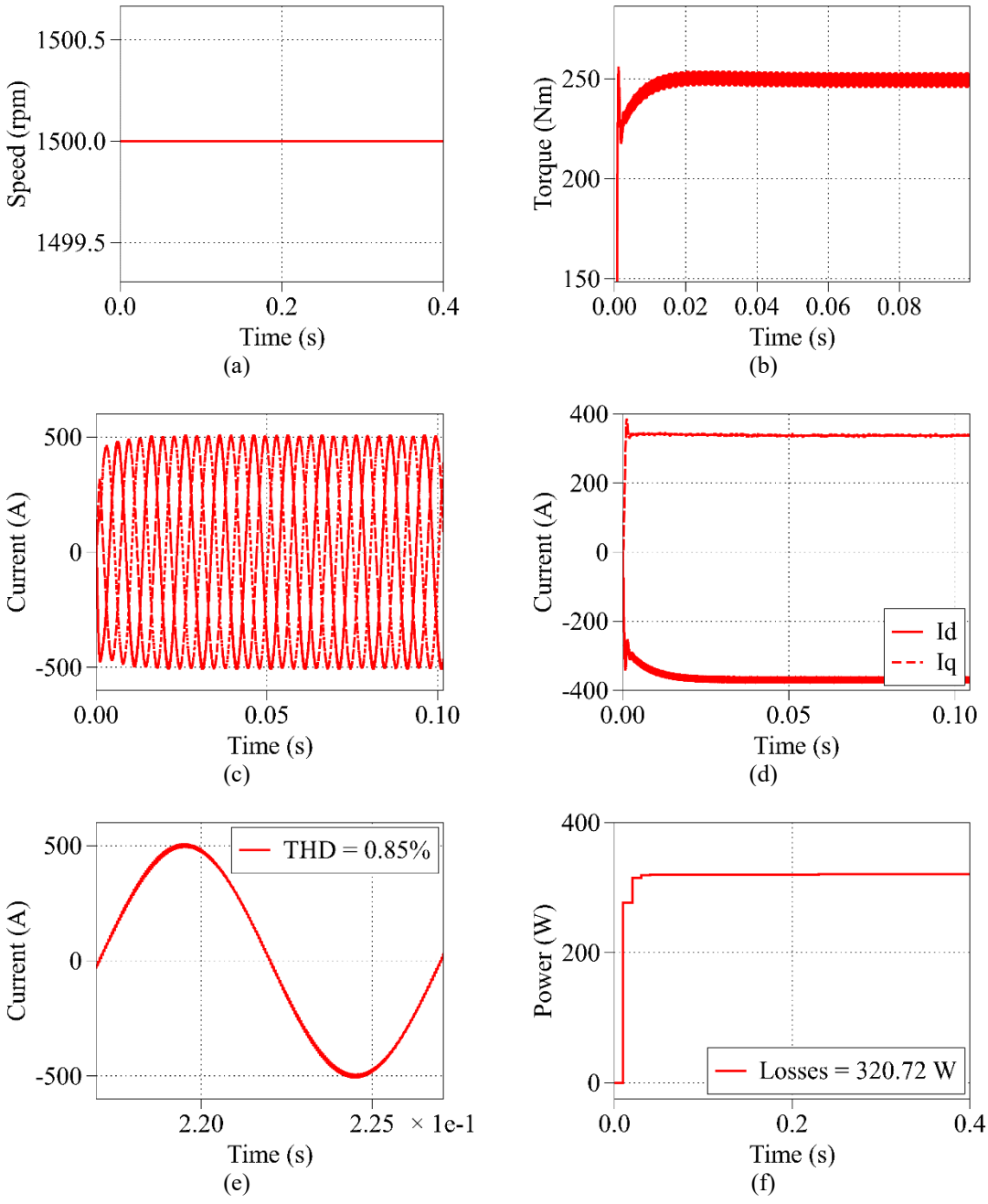
Fig. 6.4 Simulation framework for PLECS motor drive simulations.

6.4 Simulation of Electric Drive

The electric traction drive is simulated using the previously highlighted framework incorporating the capacitor degradation model, an IPMSM, SiC MOSFET based VSI and PI based current controller in order to simulate speed torque load points across the operating map of the drive through *dq*-axis current and machine speed commands. Some exemplary waveforms of the operation of the drive are illustrated in the following figures,

TABLE 6.2. SIMULATION PARAMETERS FOR SVPWM OUTPUT RESULTS

Motor Speed	1500 rpm
Motor Torque	249.4 Nm
d-axis Current	-369.28 A
q-axis Current	337.42 A
Modulation Strategy	SVPWM
DC-Link Voltage	360 V
Switching Frequency	10 kHz



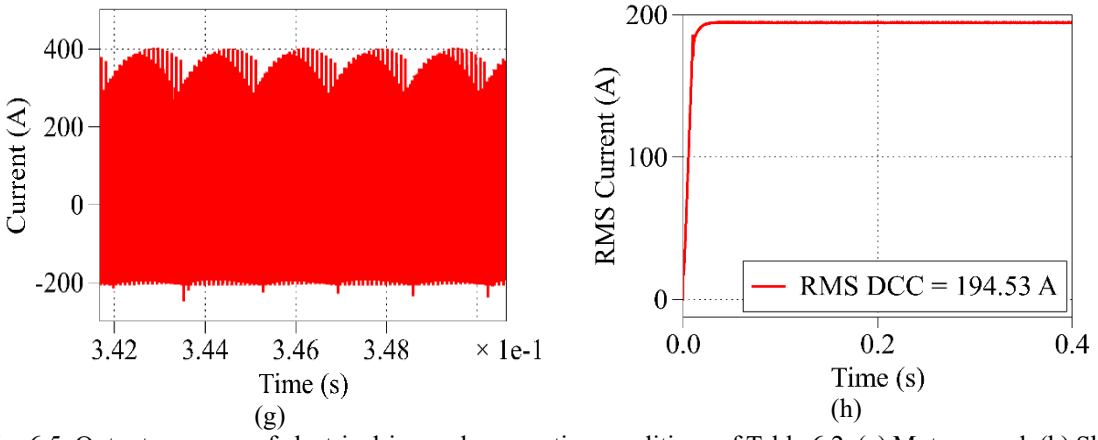
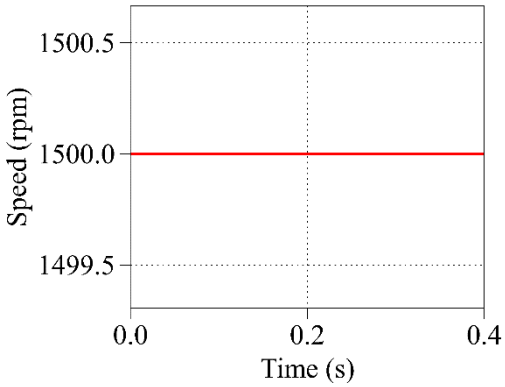


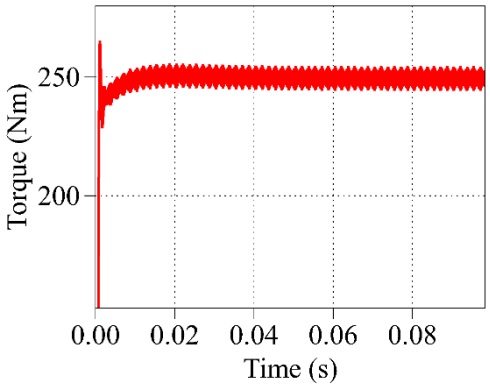
Fig. 6.5. Output response of electric drive under operating conditions of Table 6.2. (a) Motor speed. (b) Shaft torque. (c) Inverter output currents. (d) *dq* frame currents. (e) Enlarged phase current and THD. (f) VSI switching losses. (g) DC-Link capacitor current. (f) RMS value of DCC.

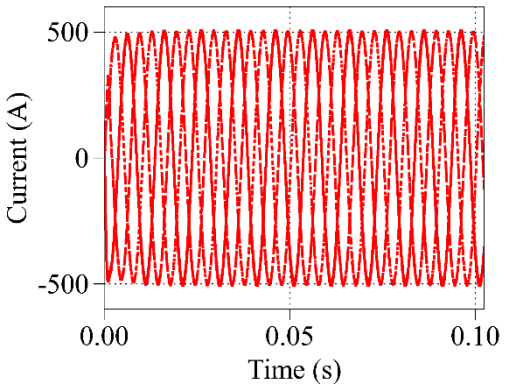
The previous figures illustrate the ability of the PLECS motor drive model to simulate the output characteristics of the drive and follow the referenced commands. The output phase current THD can be acquired as well as the switching device power losses and the RMS value of DCC used for degradation calculations. The performance under MC-GDPWM at 15 kHz switching frequency is also shown in the figures below. For the MC-GDPWM method the switching frequency is increased by a factor of 3/2 compared to SVPWM. This is because discontinuous PWM methods remain clamped for 120˚(or 1/3) of the fundamental period as mentioned in Chapter 2, and thus in comparative studies of discontinuous and continuous modulation methods the switching frequency of the discontinuous methods is often increased to 15 kHz to create equal average switching frequency of 10 kHz [9].

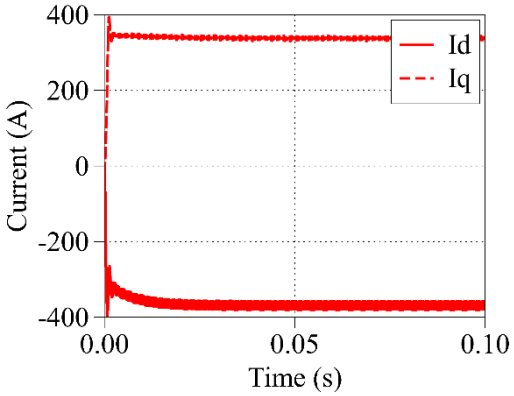
TABLE 6.3. SIMULATION PARAMETERS FOR MC-GDPWM OUTPUT RESULTS

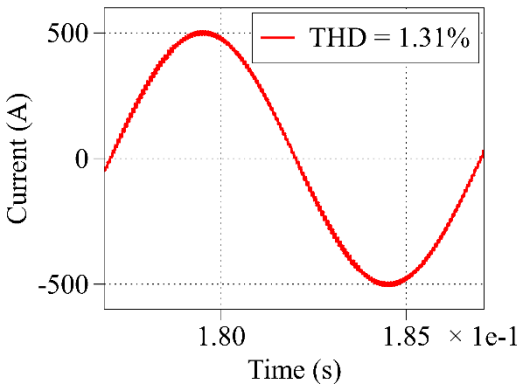
Motor Speed	1500 rpm
Motor Torque	249.4 Nm
d-axis Current	-369.28 A
q-axis Current	337.42 A
Modulation Strategy	MC-GDPWM
DC-Link Voltage	360 V
Switching Frequency	15 kHz

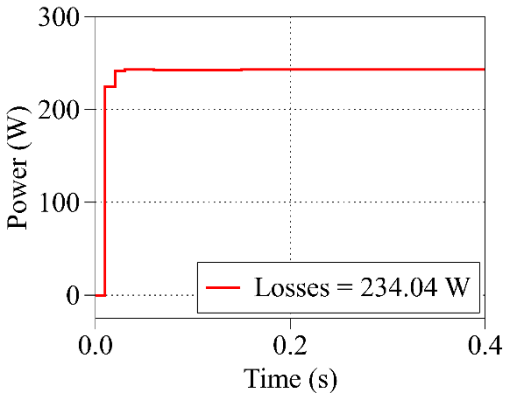

1500.5
1500.0
1499.5
Speed (rpm)
0.0
0.2
0.4
Time (s)
(a)


250
200
Torque (Nm)
0.00
0.02
0.04
0.06
0.08
Time (s)
(b)


500
0
-500
Current (A)
0.00
0.05
0.10
Time (s)
(c)


400
200
0
-200
-400
Current (A)
Id
Iq
0.00
0.05
0.10
Time (s)
(d)


500
0
-500
Current (A)
THD = 1.31%
1.80
1.85
× 1e-1
Time (s)
(e)


300
200
100
0
Power (W)
Losses = 234.04 W
0.0
0.2
0.4
Time (s)
(f)

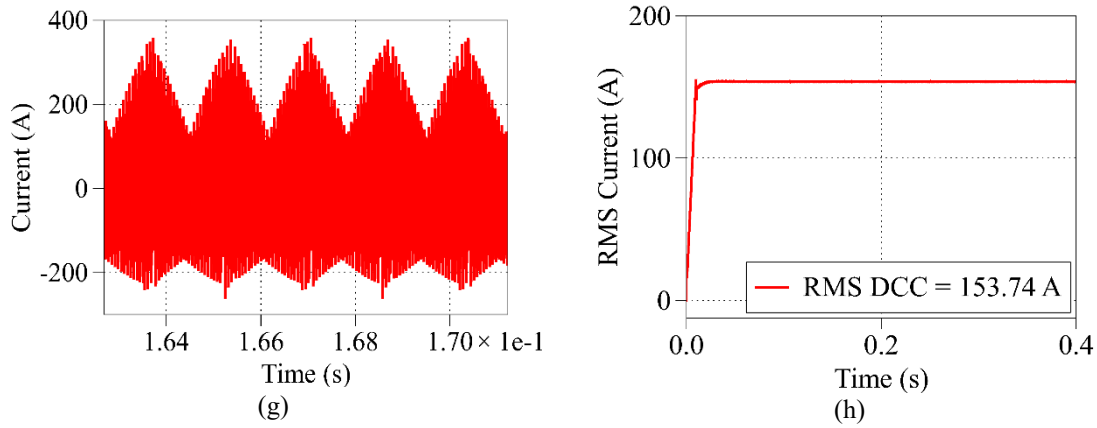
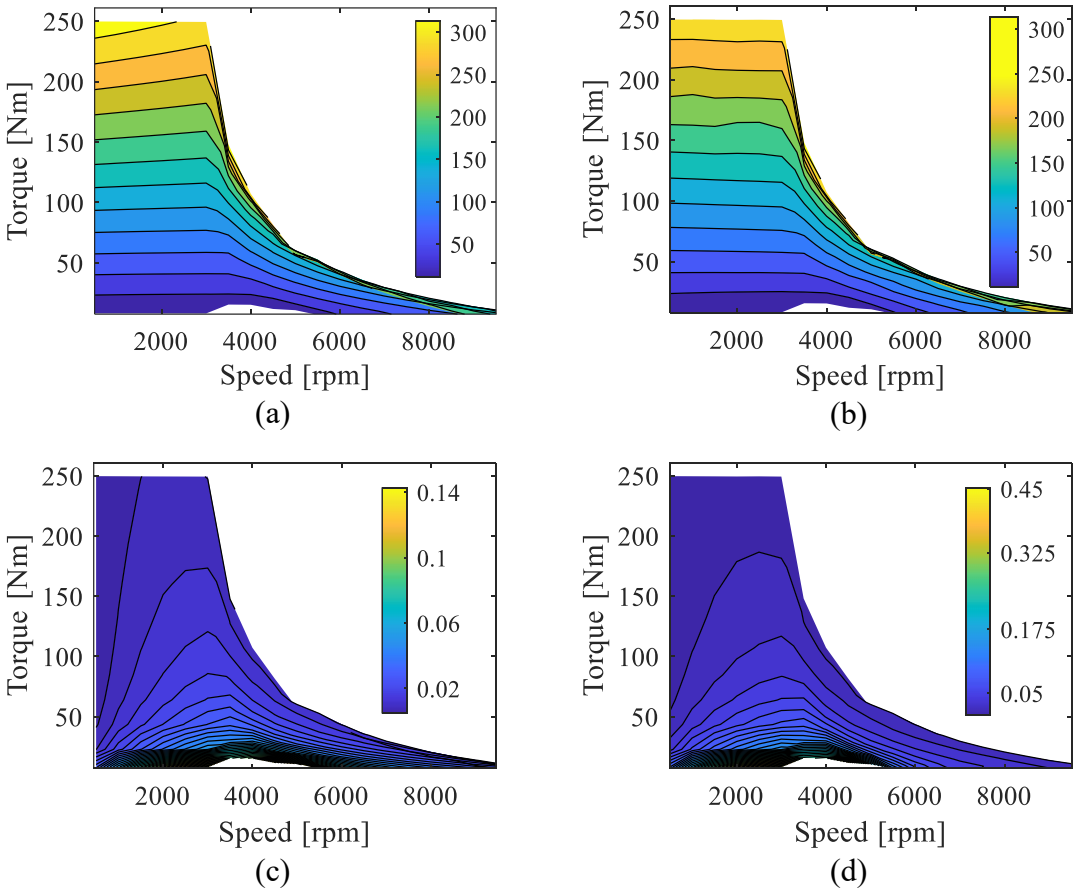


Fig. 6.6. Output response of electric drive under operating conditions of Table 6.3. (a) Motor speed. (b) Shaft torque. (c) Inverter output currents. (d) *dq* frame currents. (e) Enlarged phase current and THD. (f) VSI switching losses. (g) DC-Link capacitor current (f) RMS value of DCC.

By simulating the remaining operating points across the operating map of the electric drive under both SVPWM and MC-GDPWM, the following results were achieved.



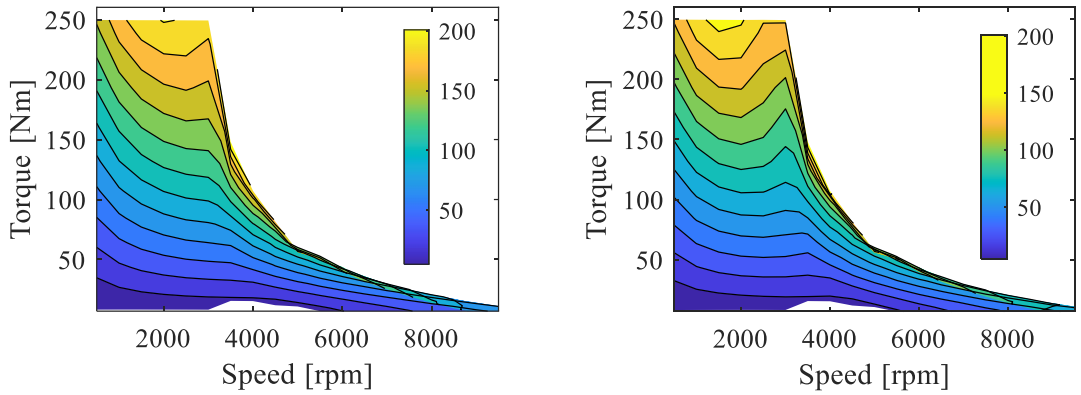


Fig. 6.7. Output response of electric drive across torque speed map. (a) SVPWM switching losses. (b) MC-GDPWM switching losses. (c) SVPWM VSI phase current THD. (d) MC-GDPWM VSI phase current THD. (e) SVPWM RMS DC-Link capacitor current. (f) MC-GDPWM RMS DC-Link capacitor current.

6.4.1 Implementation of Cost Function

Operating points across the entire torque-speed map of the PMSM are simulated under both SVPWM and MC-GDPWM with identical operating conditions in terms of DC-Link voltage, average switching frequency, and loading conditions. By extracting the switching losses, output phase current THD, and RMS value of DCC from the simulation model at each operating points and calculating the cost function, a map of the optimal PWM strategy over the torque speed map to prolong capacitor lifetime can be generated. The values of the cost function across the torque speed map of the electric drive are illustrated in Fig. 6.8 below.

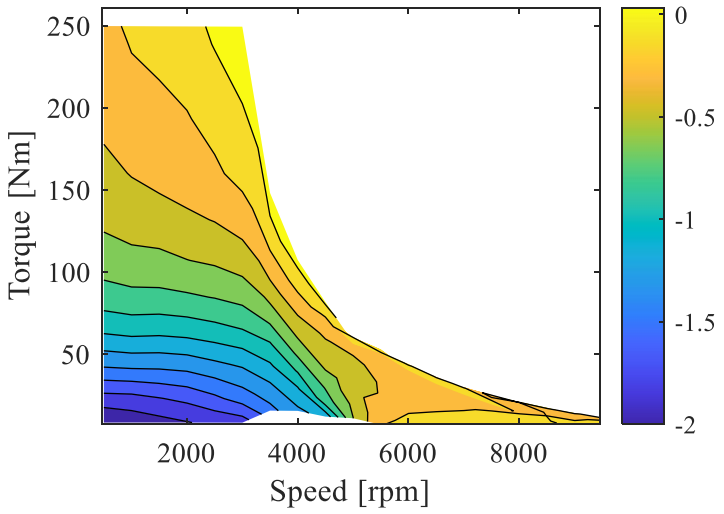


Fig. 6.8. Cost function calculations across the torque speed map of electric drive from PLECS model.

The cost function shows a relation to the torque and speed commanded to the electric drive. It appears that the lowest value of the cost function are present in the low speed and low torque region, indicating that the performance of the MC-GDPWM method in this region is significantly worse than SVPWM and that the benefit of reduced DCC and switching losses is too heavily outweighed by the increase in output phase current THD. However, as the torque is increased at each speed below the base speed of the machine, the cost function begins to increase, indicating a possible benefit of selecting the MC-GDPWM method opposed to conventional SVPWM which would allow for an extension of the DC-Link capacitors lifetime through the reduction of DCC. The reduced DCC will lead to lower device power losses, reduced hot-spot temperature and will prolong the useable lifetime of the device, and electric drive as a whole. The maximum calculated value of the cost function across the torque-speed map is 0.2 corresponding to a 20% increase in the summation of the three considered performance metrics (THD, switching loss, and DCC) and the minimum value is -2 corresponding to a 200% reduction.

Since the goal of this PWM selection strategy is to extend the lifetime of the DC-Link capacitor without sacrificing significant performance compared to conventional SVPWM, a maximum performance reduction criterion must be outlined to determine how much performance sacrifice is too much. This value will change depending on the specific system and application requirements, for example if minimal torque ripple is the main focus, or if reduced power losses is the main concern. In this thesis the main concern however is the capacitor lifetime and based on the calculated cost function across the torque speed map, a maximum performance reduction of 30% compared to SVPWM is taken as the maximum acceptable performance reduction.

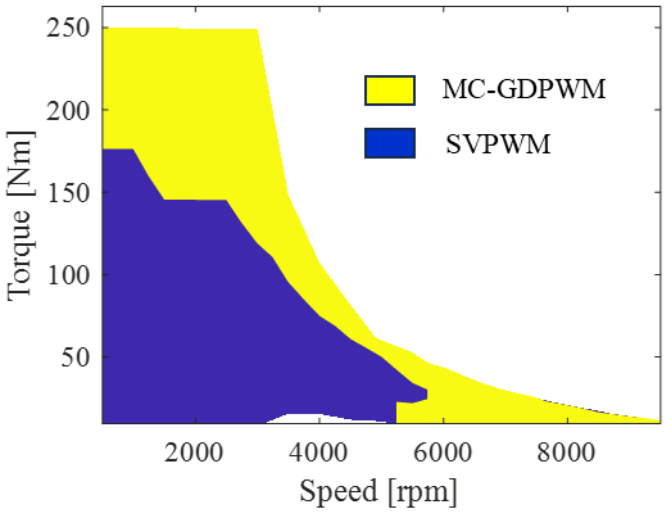


Fig. 6.9. PWM Selection determined from electric drive simulation model.

Based on the simulation results using PLECS software including the device switching and conduction loss characteristics of a SiC MOSFET based inverter for accurate power loss modelling, and based on the maximum performance sacrifice of 30%, the operating regions in which a given PWM strategy should be implemented can be generated. Fig. 6.9 shows that in the large majority of low torque and lower speed regions, conventional SVPWM still heavily outperforms the capacitor current reducing MC-GDPWM method and should this be selected for high performance operation in this region. The DCC can still be reduced in this region by selecting MC-GDPWM, however the cost of reducing DCC is outweighed by the reduction in performance in terms of THD and thus the extension of the capacitor lifetime in this region is not worth the sacrifice in drive performance according to the developed cost function. However, at certain high torque operating points as well as very high-speed operating points, the MC-GDPWM strategy can provide reduced DCC for reduced capacitor power losses, reduced internal temperature and in turn an increased remaining useful lifetime, as well as reduced switching losses without sacrificing significant performance in the electric drive in terms of output current THD. Further benefits could be achieved from the MC-GDPWM method if an increased switching frequency is adopted as THD could be further reduced, becoming more comparable to SVPWM. This may be possible in the near future as the industry shifts towards the use of fast switching wide-bandgap devices [15], [16] which offer the benefit of reduced power losses, and the ability to achieve higher switching frequencies which can

reduce output phase current THD, and in turn reduce machine side power losses and torque ripple resulting in a smoother ride for the user of the EV.

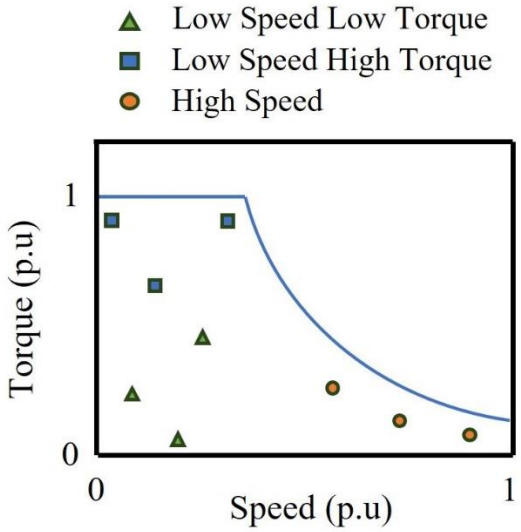
The implementation of the proposed PWM selection control strategy would consist of first identifying the torque and speed commands being requested from the ECU and determining if the given operating point falls within the SVPWM region or the MC-GDPWM region.

6.4.2 Simulation Validation of Extension of Capacitor Lifetime

In order to quantify the benefit of using the proposed PWM selection strategy, a drive-cycle based analysis of a PMSM traction drive is simulated under conventional SVPWM, and under the proposed PWM selection strategy. The online capacitor degradation model highlighted in the previous section is utilized to determine the accumulated damage experienced by the capacitor due to the drive-cycle simulation, and a final comparison of accumulated damage over the drive cycle is used to quantify the benefit of the proposed strategy. For this comparative study, lumped thermal parameters for the foster model of a film capacitor are arbitrarily selected with some influence from thermal parameters identified for film capacitors in [17] and [18], and the capacitor rated lifetime, and lifetime equation coefficients are extracted from [18] and [19], respectively.

For this comparative study, the thermal capacitance of the DC-Link capacitor is neglected to remove the period which the capacitor hot-spot temperature builds up to its maximum value at each load point. Each load point is simulated for 1 second simulation time to allow the switching losses, THD, and RMS capacitor current to settle at their final values respectively. The rated lifetime of the considered film capacitor is scaled down by a factor of 100 to allow the capacitor to produce more significant damage in the short simulation time, emulating the vehicle remaining at each load point for 100 seconds or 1 minute and 40 seconds. The simulations are complete under conventional SVPWM at 10 kHz switching frequency and the proposed PWM selection strategy utilizing MC-GDPWM at 15 kHz at 9 different load points. The load points are distributed across the torque speed map of the drive with 3 falling in the low-speed high torque region, 3 in the low speed low torque region, and 3 in the high speed region as shown in Fig. 6.10. The speed and torque commands of the load points are also highlighted in Fig. 6.10. The total switching losses and average THD over the course of the drive cycle will also be compared to allow for a

comprehensive comparison highlighting the tradeoffs between drive performance and DC-Link capacitor lifetime extension through degradation reduction.



Speed (rpm)	Torque (Nm)
500	238
1,000	64
1,500	160
2,000	23
2,500	107
3,000	238
4,500	70
6,000	30
8,000	11

Fig. 6.10. Load points used to validate proposed PWM selection method.

The results of the simulation show that the proposed PWM selection method is capable of effectively reducing the degradation of the DC-Link capacitor and thus extend its lifetime, without significant compromise of the electric drive performance under conventional SVPWM control. The total switching losses, average THD and total accumulated damage of the capacitor over the load points highlighted in Fig. 6.10 are illustrated in Table 6.4 below.

TABLE 6.4. SIMULATION RESULTS FOR PWM SELECTION METHOD VALIDATION

Performance Metric	**SVPWM**	**Proposed PWM Selection**
Total Switching Losses (W)	1,449.65	1,220.94
Average VSI THD (%)	1.831	2.311
Accumulated Damage (%)	5.362	1.368

The results of Table 6.4 clearly illustrate the effectiveness of the proposed PWM method, as the total capacitor degradation determined from the capacitor degradation model highlighted in Chapter 5 is reduced from 5.362% under conventional SVPWM to only 1.368%, for a total reduction of 3.994% under the proposed strategy. For a film capacitor with a rated lifetime of 100,000 hours as highlighted in [18], 3.994% corresponds

to 3994 hours, indicating that the useful lifetime of the DC-Link capacitor could be increased by several thousand hours under the proposed PWM control in comparison to SVPWM over the lifetime of the vehicle. The switching losses of the inverter were also reduced from 1,449.65 W to 1,220.94 W. Meanwhile, the average THD over these operating points was only increased from 1.83% under SVPWM to 2.31% under the proposed strategy, which is a small price to pay for the extension of capacitor lifetime and reduction in switching losses achieved under the proposed method.

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CHAPTER 7

CONCLUSIONS

This thesis provides background knowledge on the function of the DC-Link capacitor within an electric traction drive and highlights the various types of capacitors that are available for these applications. Film capacitors are identified as the most prevalent type of capacitor used in EV applications due to their reduced power losses and increased lifetime in comparison to alternative options. The need to monitor the condition of the capacitor over its lifetime is presented as it is shown that the DC-Link capacitor is the most prone to failure device within the traction electric drive, attributing to 30% of inverter faults. The various significant factors which impose stress on film capacitors and the failure mechanisms of the device are discussed in order to provide a deeper understanding of the factors impacting the lifetime of the capacitor during its operation in the traction drive.

The control theory of a traction drive is presented to provide a clear perception of the objective of the electric drive system within an EV and also to provide some background knowledge on how the selected control strategy can impact the lifetime of the capacitor. Several capacitance condition monitoring methods currently available in literature are discussed and the benefits and drawbacks of each are considered. An effective strategy for the condition monitoring of film capacitors in VSI is identified and several tasks are carried out in order to adapt this previously proposed method to EV applications through the consideration of various factors including current sensor noise, external environmental conditions, and the use of the history of recorded estimations to make an improved estimation of the current level of degradation present in the DC-Link capacitor. Simulation results of the impact of sensor noise and controller sampling frequency are provided to allow system designers to have a better understanding of the system requirements necessary to make reliable estimations of capacitance for condition monitoring purposes.

A simulation study was conducted to show the improvement in capacitance estimation that can be achieved through the consideration of ambient temperature. An improvement of 0.3245% in accuracy was achieved by including the effects of temperature on the capacitance of a film capacitor. Although this value may seem insignificant, when an estimation accuracy of 1% is desired for film capacitor capacitance estimation, and a 5%

reduction from its initial capacitance signifies the end-of-life, any improvement in accuracy is beneficial. Through curve fitting the history of recorded estimations, an accurate representation of the capacitance over time can be achieved as shown in the simulation studies. This provides knowledge of how the DC-Link capacitor degrades over its lifetime and can be useful as the implementation of this method in EV applications can allow for future use of these plots of capacitance over time to provide an understanding of the predicted lifetime of the DC-Link capacitor without the need for accelerated lifetime testing and other methods which require extensive time and effort. An experimental implementation of the capacitance estimation was performed to validate the ability to implement this method in a low inductance PMSM drive to emulate the true conditions of an EV system, and to also validate the simulation study to determine the minimal sampling frequency requirements of the controller to make consistent reliable estimations. The experimental results and simulation results concluded that a minimal sampling frequency of approximately 50 kHz is required to provide sufficient data to make reliable estimations in a low inductance PMSM drive.

Finally, a novel PWM selection strategy is proposed in this thesis which alternates between conventional SVPWM and DC-Link capacitor current reducing MC-GDPWM in certain operating regions based on a cost-function designed to compare the key performance metrics of the drive including VSI switching losses, phase current THD and DCC. A simulation based comparative study was conducted to show the ability of the proposed method to extend the lifetime of the DC-Link capacitor in comparison to conventional SVPWM. The study consisted of several load points scattered across the torque speed map of a high power PMSM drive with a 350 uF film capacitor using a capacitor degradation model to determine the accumulated damage over the simulated load points. The results of the study showed that the lifetime of the DC-Link capacitor could be increased by up to 3,994 hours under the proposed strategy compared to SVPWM for a capacitor with a lifetime of 100,000 hours, while also reducing the total switching losses by 15.78% while only increasing the average THD from 1.83% to 2.31%. Extension of the capacitor lifetime in turn extends the lifetime of the entire EV, which helps create a more cost-effective product for the user as they can receive a longer vehicle lifetime without an increase in cost.

7.1 Future Work

With the conclusion of the work in this thesis, with respect to the capacitance estimation study, future work may include the analysis and determination of the details related to the real implementation of the condition monitoring method in a real EV application, including but not limited to determining where the history of recorded estimation will be stored and where the curve fitting and post-processing will be complete, in the microcontroller or possibly in some cloud-based server to meet memory storage requirements. Additionally, determining how many times the estimation would be performed when the vehicle is shut down, if it will be complete only at shutdown or also before starting up, if it can be performed during charging activities etc. There are various small details that significantly impact the real implementation of this method in a true EV application and can be selected carefully in order to further optimize this capacitance estimation method for reliable and accurate condition monitoring.

The work of the PWM selection method can be extended in future work by taking full system performance into consideration to further analyze the impacts of the proposed PWM selection method on machine-side losses for a more comprehensive study. Using some physical model of the electric machine the phase currents generated from the VSI under the proposed strategy can be input to determine the machine side losses and determine if the benefit of the reduced capacitor current is still worth the sacrifice of the reduced phase current quality from the inverter. Furthermore, after the machine side study is complete this method could be implemented experimentally to truly validate the capability of the proposed method to extend the capacitor lifetime without significant sacrifice of the electric drive performance.

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