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Decentralized Control of Unbalanced Hybrid AC/DC Microgrids for Maximum Loadability

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By

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Decentralized Control of Unbalanced Hybrid AC/DC Microgrids for Maximum Loadability

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I. Co-Authorship

I hereby declare that this thesis incorporates material that is result of joint research, as follows: The thesis incorporates outcomes, results, and graphs of future unpublished material co-authored with, and under the supervision of, Dr. Maher Azzouz. In all cases, primary contributions, experimental designs, data analysis, interpretation, and writing were performed by myself; Dr Maher Azzouz contributed some of the key ideas, general literary guidance, editing, and review of the written papers.

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ABSTRACT

To realize a hybrid AC/DC microgrid, an interlinking converter (IC) is required to couple the AC microgrid (AMG) with the DC microgrid (DMG). While this configuration offers merits of bidirectional support and cooperation of both girds, which could improve the performance of the entire system, the ICs are left underutilized. The IC is an AC/DC converter and thusly has broad potential for AC-side support without any practical power cost on either side. This potential can be unleashed simply by utilizing an enhanced control and coordination schemes, without physical or hardware modification. The IC can provide different modes of support such reactive power support, and unbalance power mitigation. All of which could result in reduced loadability of the system, specifically on the AC-side. Several techniques have been demonstrated in the literature to utilize the IC for maximizing the loadability of the AC-side. However, all these methods are of the centralized type, or require extra or extraneous hardware. The centralized method, while more comprehensive, has several disadvantages, chiefly of them is complexity, which in turn impacts speed, cost, and reliability. The proposed work in this thesis develops a communication-free, decentralized method to achieve comparable results. The three-phase voltages and currents are decomposed into positive and negative sequence components. By controlling these sequences, the ICs can relieve the unbalanced power from the distributed generators of the AC-side, which helps maximizing their loadability. Furthermore, using a decentralized coordination method, the burden of the unbalanced power could be shared fairly between multiple ICs.

DEDICATION

Bismallah, and peace be upon His Prophet. As is for all of my work in my life, this thesis is also dedicated to Allah subhanahu wa ta'ala. I also dedicate it to the world and its people, but especially to my mother, father, siblings, relatives, friends, mentors, supervisors, and all those who have believed in me. All of whom helped me through this arduous journey and to finish this work.

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I'd like to give thanks to my family, without whom I wouldn't have been able to start nor finished. I'd like to thank my supervisor Dr. Maher Azzouz who believed in me when others didn't. I'd like to extend thanks to Dr. Mitra Mirhassani who believed in me when I didn't. I'm thankful for my committee members for keeping up with my terrible schedule and short notices. And great thanks to all my friends who kept me company when it got rough, and those who waited for me for when I was done. Lastly, thank you, the reader, for your interest in this work.

"To all the food in the world, I give my gratitude. Itadakimasu" – Toriko. This was a feast. Thank you.

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CHAPTER 1
INTRODUCTION

1.1 Background

For more than 100 years- since the inception of the electric power grid- most of the power generation sources and loads were of the Alternating Current (AC) type. With the recent technological development, and the proliferation of electronics and batteries and all facets of life, there has been a universal paradigm shift with the typical power generators and load into the Direct Current (DC) type [1].

DC generators and sources cannot run natively on the AC power grid. They require an AC/DC interfacing converter to be able to operate on the AC grid. This converter adds cost to the DC devices and results in power losses, with a typical efficiency of 87.5% minimum, according to regulations [2]. It should be noted that this is the one-way efficiency. Going from a DC generator, to AC transmission, and into a DC load compounds the issue. The resulting round trip efficiency would be the square of that, which reduces the efficiency to 76.6%. This figure is not true for every type of converter, but it is apt to demonstrate that any extra conversion step is inherently less efficient than the lack of such. This agrees with some sources claiming the loss of about third of the energy during conversion [3]. It should be noted that this figure keeps improving with emerging technologies [4].

Moreover, DC loads cause harmonic distortion in the AC power grid, thus affecting the power quality of the grid. These issues are amplified by the aggressive trend of electric vehicles (EV) penetration into the market [5], [6]. To be able to accommodate these changes, the electric grid needs to adapt and evolve.

Therefore, there has been an increased interest in DC power grids [7]. In this type of grid, the native generation, transmission, and load runs on DC. This eliminates, or greatly reduces the need for interfacing converters, leading to reduced cost, and increased total system efficiency. However, it is not feasible to completely replace the AC grid with a DC grid. At least not in the foreseeable future. The better solution for next-generation distribution grids is to have both; the AC grid can be used for AC loads and generators, and the DC grid for its kind of load. Both grids have their advantages and disadvantages. And there lies a great opportunity.

AC grid advantages:

1. Native to electrical machines. Practically all electromechanical generators run on AC natively. Minimal requirements for transformers/converters to connect to the grid.
2. AC transformers are passive elements. This simplifies the process of changing voltage level and galvanic isolation in the AC grid.
3. The frequency of the grid is a global variable. That is, at any single point of time, every device connected to the grid will see the same frequency, within the speed limits of causality. This allows for easier and more precise coordination between grid devices and equipment. The DC grid lacks this feature, which introduces errors in the proportional power generated by the DC generators.
4. Compatibility and infrastructure. Most devices are designed to run on the AC gird. Devices critical to operation of the AC grid, such protection relays and transformers, are designed to only run on AC. Newer versions of those need to be designed, manufactured, and installed to run on the DC grid.

DC grid advantages:

1. Significantly easier to control. The AC grid is comprised of three-phases that carry sinusoidal currents that requires more complicated designs for controllers [8]. Comparatively, DC control can be implemented using straightforward PI controllers.
2. Less requirements for operation and stability. Unlike the AC grid, there is no need for reactive power generation or limits; angle stability; or voltage balancing between the phases.
3. More efficient at transmission. DC transmission is not susceptible to inductive, capacitive, or skin effect losses [9].
4. Asynchronous. No need to synchronize generators to the grid and allows for interconnectivity between AC grids of different fundamental frequencies [10].

1.2 Conventional Power Generation

The operation of the electric power grid can be divided into three main parts: *generation*, *transmission*, and *distribution*. Each is a broad subject and an overarching field of research on its own. This thesis is mainly concerned with the distribution aspect of electric grid which impacts the generation of electric power. Therefore, it's very important to understand the basics of power generation.

1.3 Conventional Electric Power Grid

The mainstream electrical power grid uses an extremely centralized generation model. The power that feeds the grid is generated, and controlled, from a single, or few, locations and sources. Transmission lines carry this power to customers through transformers that

regulate and transform the voltage levels for reduced transmission losses. Figure 1.1 shows a simplified diagram of the conventional power grid.

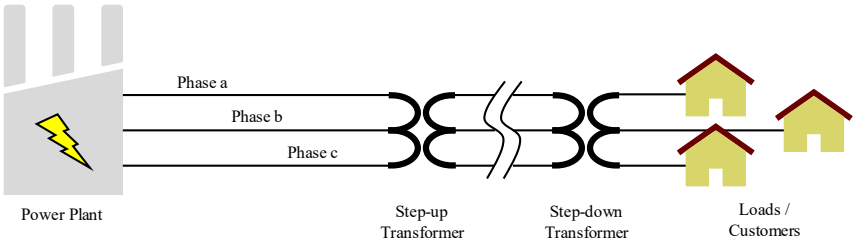

Figure 1.1: Simplified Power Transmission Topology

This approach allows for easier control and coordination of generation and enables tighter control on the power quality. But as it can be expected, if something happens to that centralized location, then power is lost to all those customers, leaving them in the dark for extended periods of time. This concept is called Single Point of Failure. Several of these notorious incidents occurred where entire regions of the US and Canada suffered from a blackout due to grid faults [11]–[14]. Not to mention the blackout that happened few days later in Europe. This drawback of centralized generation is more prominent during the times of sever weathers and natural disasters.

1.4 Microgrids

As per the IEEE Std 2030.7, a microgrid (MG) is: “A group of interconnected loads and distributed energy resources with clearly defined electrical boundaries that acts as a single controllable entity with respect to the grid and can connect and disconnect from the grid to enable it to operate in both grid-connected or island modes” [15].

So, there is a wide range to the possible size of a microgrid. It could be a district, a neighbourhood, or even a single building or home. The smallest microgrid could be a single

distributed generator (DG) with a single load, given that the DG can supply the load's demands on its own when this microgrid is disconnected from the main grid. Figure 1.2 shows an example of what a microgrid could look like with two distributed energy resources (DER), two loads, and a switch, or a relay of sorts. The two DERs consists of a DG and a battery bank for storage. The transmission lines impedances are omitted for simplicity. The enclosed region is able to operate normally, even when the switch is open. When the switch is closed, it operates as a single unit, as far as the infinite bus (main grid) is concerned.

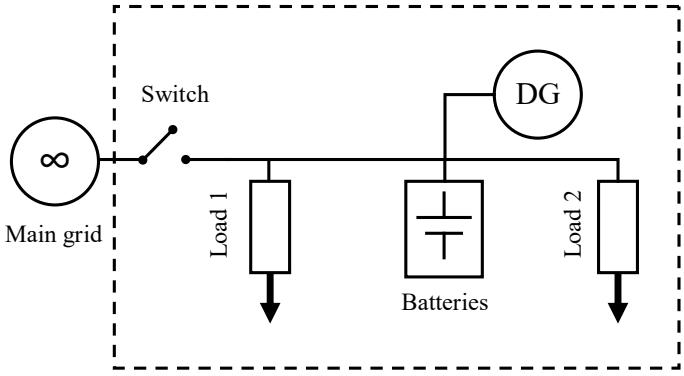

Figure 1.2: Example of a microgrid

It should be noted that there are no specifications for the type of current for the microgrid. Meaning, the microgrid can run on either AC or DC, or a hybrid configuration of both.

Microgrids are a relatively novel idea, with the earliest mention of it in the literature was in 2001 [16]. It was conceived as a response to the proliferation of DERs, such as photovoltaic (PV) panels, battery banks, and fuel cells. This helps the local grid, now a microgrid, be electrically isolated, and provides peak power and ride-through capability. Yet, it is still connected to the main grid for power exchange based on need and financial incentives. This contrasts with the centralized approach of the conventional AC grid. As

all things are, nothing is perfect. As such, this approach introduces new challenges and unique problems to be solved.

1.5 Hybrid Grid

A hybrid gird, in the context of this thesis, is a grid that utilizes both AC and DC. To operate as a single entity, the two grids must be interfaced, or interlinked, together through an interlinking converter (IC or ILC). This device is a bi-directional AC-DC voltage source converter (VSC). Its main goal is to balance the proportional power utilized on the DC-side, and the AC-side. For example, if the AC-side is loaded at 30% of its maximum generation limit, while the DC-side is sitting at 70%, then it will transfer power from the AC-side to the DC-side until they both become 50% loaded.

1.6 Motivation and Objectives

1.6.1 Motivation

The greatest challenge to the modern power grid is perhaps the aggressive adoption of electric vehicles (EVs). The shift of almost a century worth of gas-powered vehicles to the electric grid will force the grid to adapt to satisfy the voracious appetite of this beast of a challenge [17], [18]. For example, if all vehicles become electrically powered, this might increase the power loading of the electric grid by around 30% [19].

There are two intuitive ways to solve this. First option is to increase generation of centralized power plants by 30% and capacity of transmission line by 30% to withstand the increased load and demand. Also, increase by 30% the sizing of all the distribution transformers and relays. Given the relatively short time scale for full EV adoptions [20],

[21] and the urgency to solve climate change problems, this option is most likely financially prohibitive.

The second option would be to bring the power generation to the load, or as close as possible. This would require shifting the power grid paradigm from a centralized approach to a decentralized one. It would also require segmenting the grid into microgrids that have their own power generation and management capabilities. Since the power generation is localized to the load, the rest of the grid can be left untouched, with only upgrading the cabling for the final few meters, if needed.

Even though the concept of a microgrid is relatively new, the idea of *hybrid* AC/DC microgrid (HMG) is even more recent. Earliest reference of a hybrid microgrid and interlinking converters is from 2011 [22]. This makes the subject a fertile ground for novel ideas and exploration.

Many of the literature concerning the control of the hybrid AC/DC microgrid uses the centralized approach for coordination and management, as will be explored in CHAPTER 2. While this approach can be comprehensive, it is relatively slow and requires communication lines. Furthermore, utilizing the classical centralized control approach is antithetical to the concept of microgrids. The concept of the microgrid was incepted to decentralize power generation, allowing for a more dynamic and resilient power grid.

1.6.2 Objectives

As such, the objectives of this thesis are:

1. To develop a method that shifts the unbalanced power from the DGs to the ICs.

2. To utilize a decentralized, communication-free approach of coordinating the unbalanced power sharing between the ICs in the HMG.
3. To further mitigate the voltage imbalance caused by the unbalanced loads.
4. To implement all the previously mentioned objective with minimal impact to the dynamic performance of the controllers.

1.7 Thesis Outline

Chapter 2 A literature survey to explain the state of art regarding HMGs and the trends in control and coordination methods.

Chapter 3 Establishes a theoretical framework as a basis for the proposed methodology.

Chapter 4 Presents the proposed methodology and explains in detail how each feature of the control scheme works, and how contributes to the end result.

Chapter 5 Demonstrates the dynamic performance of the proposed controller, and how it compares to conventional methods in the literature.

Chapter 6 Showcases the steady-state simulation results proposed control scheme using a hybrid microgrid case study. The case study results are compared to centralized solution in the literature which using the same test system.

Chapter 7 Wraps up the thesis with a summarized conclusion, and suggestions for possible future improvements and additional work.

CHAPTER 2
LITERATURE SURVEY

To better understand the motivation and the novelty of the proposed methodology, it is important to examine the development of the literature regarding the subject of the hybrid microgrids, the current state of the art, and the gaps in the literature. It also helps to understand the direction of the literature to better plan for future works.

2.1 Microgrids

The paper trail starts when the idea of a microgrid (MG or μG) was conceptualized in 2001 in [16], which has become the cornerstone for all things microgrids. The paper has since been cited in many papers regarding the topic. It was shortly followed by [23] by the same author to create a power flow model for MGs. The model can be used for three-phase and single-phase loads, and therefore can be used for simulating unbalanced conditions.

Since then, the development of the MG concept branched into a myriad of topics, each targets a facet, or more, of MGs. Some of the more prevailing concepts are concerned with the integration of renewable energy resources (RES) [24]–[31], energy storage systems (ESS) [31]–[35], or both [36]–[41].

Another prominent topic is the subject of control and management of MGs. The type of control can be broadly split up into two types: communication based [42]–[54], and communication free [55]–[59]. The communication-based control can be divided into centralized [42]–[46], hierarchal [47]–[50], and multi-agent [51]–[54] control schemes.

However, the issue with communication-based control and coordination methods is that they are antithetical to the concept of a microgrid as it was originally conceptualized. The

impetus of the MG is to paradigm shift electric power from a centralized concept to a decentralized concept that can operate without communication links, and which can adapt flexibly to change. That is why, ideally, the MG control or coordination method should be one that is a decentralized and communication free. Furthermore, it seems there is less work done on communication-free methods compared to communication-based controls.

Although the initial concept of an MG is based on an AC grid, the definition [15] of an MG is not restricted to the AC microgrid (AMG). On the contrary, a DC microgrid (DMG) might prove to be a more practically useful concept. This is because DC grids are currently quite rare in practice. Therefore, it would be more logical to start with implementing them on a smaller scale, which is an apt role for DMGs.

As such, the literature for DMGs expanded following the increased popularity of AMGs [60]–[75]. It should be noted that the seventeen cited papers regarding DMGs all directly cite [16] and span sixteen years. Five of those are from the last two years, alone. This indicates an increased interest in DMGs, as expected from the trends caused by RES, ESS, and EVs. One of the earliest papers regarding a DMG is when one was used to supply power for telecommunication towers [60]. Another similar case can be seen in [76]. One emerging application is as DC Shipboard Microgrids [77]–[81].

Another trend indicator that can be used is the number of returned search result in literature. Between 2015 and 2018, IEEE Xplore returns 10,045 search results for conference and journal papers using the term “Microgrids”. 29.7% of these results are “DC Microgrids. This is compared to 32.1% for the time period of 2019-2022.

2.2 Hybrid Microgrids

Hybrid microgrids offers the best of the two worlds of AMGs and DMGs. The core device of the HMG is the IC. Hence, it is the target subject when talking about HMGs. The concept of HMGs was introduced in [22] when the IC was incepted. This is another pivotal paper that has been cited more than [16] with a significantly larger impact. This is a possible indication that HMGs are a bigger trend in literature than MGs.

Like MGs, one of the most popular publication topics is microgrid control. And similarly, the control can be categorized into communication-based and communication free. Likewise, communication-based can be categorized into centralized, hierarchical, and multiagent control schemes.

A straightforward centralized control method is proposed in [82]. Using a communication link, a centralized controller gathers all the required measurements in the HMG. Then, it generates the reference values for the ICs to command the power flow between the various subgrids. Since the central controller supervises all the ICs in the system, it is able to coordinate them in a way that avoids circulating currents between them.

A more advanced centralized control method is proposed in [83]. Its main goal is to maximize the loadability of the HMG by mitigating load imbalance in the AMG. Since the load imbalance can be translated as three phases having independent voltage, current, and power, the power flow model of the system considers each of the AC phases separately. The central controller consolidates the various measurements of current and voltage from the DGs and ICs. Then, using the proposed dynamic power routing scheme, the central controller then adjusts the droop settings for the ICs to achieve two goals. The first goal is

to balance the loading between the AC and DC side of the HMG. The second goal is to utilize the ICs to alleviate the burden of unbalanced power from the AC DGs. This allows the DGs to maximize their real power loading capabilities.

A multi-agent control method uses communication between ICs to coordinate the power sharing of subgrids based on events. This reduces the communication between the agents [84]. Another control scheme communicates with the ICs in a hierarchical structure to command their power transfer, ac support, and dc support functions [85]. Since it uses a mix of centralized and decentralized levels, it is able to offer some mitigation during communication link faults and failures. Another way to use communication links is using peer-to-peer architecture [86].

One of the biggest challenges with the communication-free control scheme is due to the DC subgrid of the HMG [87]. This is because the IC can only sense local variables on the DC side, like voltage and current. Due to line impedances of the DMG, different points in the subgrid will observe different voltages.

This issue is most apparent when there are parallel ICs between a DMG and an AMG. While all ICs are able to accurately measure the loading level of the AC side, different ICs measure different loadability levels for the DC side. That means the amount of power they transfer between the two subgrids will not be equal. In some cases, that leads to sharing error between the two subgrids. In other cases, it might lead to circulating current between the parallel ICs [88].

A commonly proposed method to mitigate this issue in the literature is to superimpose a small AC voltage on the DMG. This creates a global variable in the DC grid in the form of

frequency of the small AC voltage. In [88], [89], the power of said AC voltage is calculated to be used in a droop that relates the power loading level with the frequency. A similar concept is used in [90], except the superimposed voltage is controlled by a single device, like a DC DG or an IC. The other devices on the grid extract the frequency from the measurements of the small AC voltage. Then, each individual, local controller can use it as a global variable to infer the loading level of the DC side.

A different communication-free control scheme utilizes the zero sequence of a $dq0$-frame transformation on the AC-side to eliminate the circulating current [91]. Furthermore, it points out that the relationship between the power on the DC side is linear with the square of the DC voltage. Thus, it proposes the usage of P_{dc}-V_{dc}^2 droop for the DMG. This is in contrast with the conventional P_{dc}-V_{dc} droop. With this proposed method, the control scheme is able to eliminate the circulating current between the parallel ICs.

2.3 Unbalanced Power in Hybrid Microgrids

After surveying literature for the topics of MGs and HMGs, as discussed in the previous sections, a gap was identified. Unbalanced power condition in microgrids is not a farfetched issue. Especially with smaller sized MGs. To the point that the first paper that proposed a power flow model for MGs had considered unbalanced conditions [23]. While unbalanced power is an issue present in AMGs and not DMGs, it is nevertheless an issue for HMGs as well.

Despite that, it seems to be an understudied issue in the literature when MGs or HMGs are concerned. One of the few papers to address this issue is [83], which was discussed in the previous section. In one of the case studies simulated in the paper, it was found out that the

real power generation of the AC DGs was limited to 64% of their capacity due to unbalanced loading conditions. The issue was alleviated by having the ICs route power between phases to balance the loading in the system.

While this is a remarkable improvement, the proposed control scheme utilizes a central controller with communication links. Designing a decentralized, communication-free control scheme that achieves the same goal would make a significant contribution.

2.4 Decentralized Coordination Methods

With the gap identified, the goal is to emulate the results of [83] but in a communication-free manner. Achieving that can be done by means of controlling the negative sequence components of voltages and currents in the grid. Several techniques exist in the literature to achieve that requirement. Since the negative sequence voltage or current appears as a ripple in the *dq*-frame with twice the frequency of the positive sequence voltage or current respectively, the conventional technique is to utilize a low-pass or a notch filter to remove said ripple [92], [93].

However, this gives rise to another issue. In cases where there are more than one IC in the HMG, the unbalanced power support might not be shared equally between the ICs. This might cause one the of the ICs to become overloaded when the other one is underutilized. In effect, this reduces the total rated capacity of the ICs. This is the same reasoning behind the need for equivalent sharing of DGs loading or balancing the loading between the subgrids of and HMG.

Luckily, the literature offers several solutions to this particular issue. One paper [94] proposes a droop between the unbalance power and negative sequence conductance. This

allows for proportional unbalanced power sharing between DGs, similar to the conventional droop for proportional sharing of reactive power. However, there are several issues with this solution, especially when applied as a solution for the identified gap. First, it is designed for DGs operating in an AMG. The gap requires this solution to be adapted for ICs in the HMG. Second, unbalanced power is a local variable depending on the equivalent impedance between the DGs, or ICs, and the load unbalance. This will often lead to sharing error. Third, it adds a negative sequence impedance between the DGs, or ICs, and the unbalanced load, which would raise the voltage unbalance in the system.

One solution considers ICs equipped with power electronic transformer (PET) [95]. By adjusting the control and droop setting of the ICs, it is possible to utilize the PETs to provide the power unbalance for the AC side of the HMG. However, a glaring issue with this approach is that it requires additional hardware, or physical modification to the ICs. Conventionally, ICs do not include PETs in their design, so this approach can't be used with a typical IC.

Another candidate solution is the one used in [96]. It uses a superimposed small signal on the MG. It uses a droop to relate the unbalanced power with the frequency of the generated small signal. This influences the power of the small signal. Then, a second droop is used to relate the small signal power with the negative sequence impedance of the DGs. This way, they can restrict the unbalanced power flow until they are sharing the unbalanced power burden proportionally. Since the small signal frequency is a global variable, the sharing error is nullified, for all intended purposes. However, this method uses a negative sequence impedance. As with all methods using a virtual impedance implementation, it might lead to increased negative sequence voltage in the AMG.

2.5 Summary of Identified Gap

At this point, it is possible to summarize the features of various solutions in the literature, and how they apply to the requirements for the identified gap. Furthermore, they can be compared with the features of the proposed methodology. This helps highlights where the other methods fall short compared to the proposed methodology. This summary is tabulated in Table 2.1.

Table 2.1: Gap analysis summary

Method	**Utilizes IC**	**Does not increase V^-**	**Communication-free**	**No extra hardware required**
Centralized [83]	X	X		X
Negative sequence droop [94]			X	X
Power electronics transformer [95]	X	X	X	
Small signal coordination [96]			X	X
Proposed control scheme	X	X	X	X

As it can be seen, the proposed method combines the features and techniques of decentralized and communication-free coordination methods to produce results comparable to the centralized method without the need for a centralized controller or communication links. Furthermore, the control scheme does not require any physical modification or addition to the existing hardware of the ICs.

CHAPTER 3
THEORETICAL FRAMEWORK

This chapter establishes the theory needed to understand and implement the proposed methodology. The information in this chapter is not basic or common knowledge. It is relatively specialized, and without it, the proposed methodology would be very confusing.

3.1 Phasors and Frames

3.1.1 Space-phasor

A balanced three-phase sinusoidal function with amplitude, $\hat{f}$, angular frequency, ω, and initial phase angle, θ_0 is conventionally defined [8] as:

$$f_a(t) = \hat{f}\cos(\omega t + \theta_o),$$
$$f_b(t) = \hat{f}\cos\left(\omega t + \theta_0 - \frac{2\pi}{3}\right),$$
$$f_c(t) = \hat{f}\cos\left(\omega t + \theta_0 - \frac{4\pi}{3}\right) \quad (3.1)$$

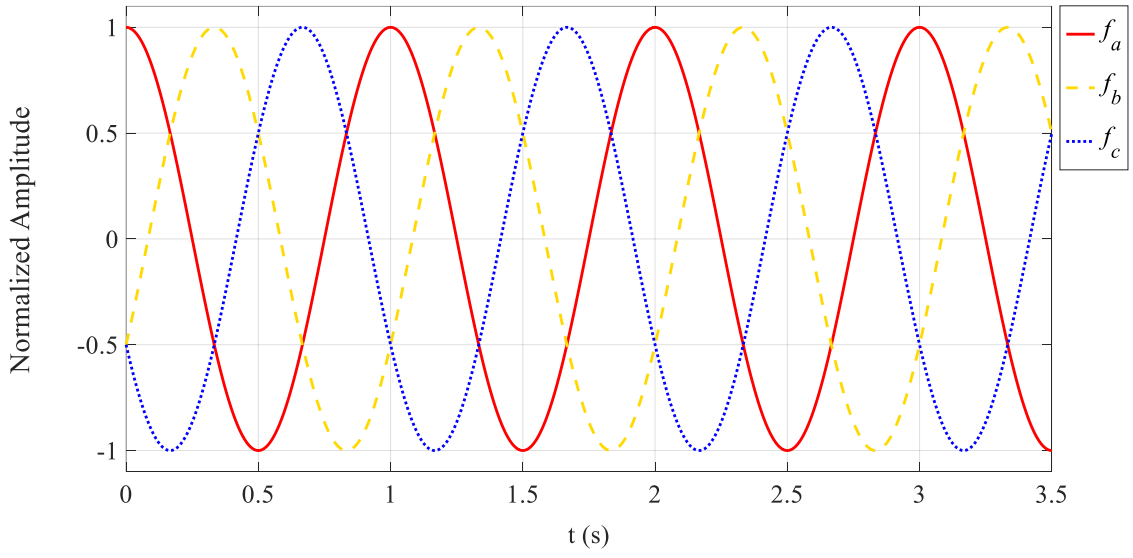

Figure 3.1: Balanced three-phase sinusoidal function.

In this form, the function can be tedious to represent and display, while also being confusing and difficult to understand. Luckily, there are better ways to present it in a more concise manner, without the loss of information or subtle details. The phasor, $\vec{f}$, can be defined as

$$\vec{f}(t) = \frac{2}{3}\left[f_a(t)e^{j0} + f_b(t)e^{j\frac{2\pi}{3}} + f_c(t)e^{j\frac{4\pi}{3}}\right] \tag{3.2}$$

Substituting (3.1) into (3.2), and defining $\psi = \omega t + \theta_0$ for conciseness, the phasor equation can be solved as

$$\vec{f}(t) = \frac{2}{3}\hat{f}\left[\cos(\psi)\, e^{j0} + \cos\left(\psi - \frac{2\pi}{3}\right)e^{j\frac{2\pi}{3}} + \cos\left(\psi - \frac{4\pi}{3}\right)e^{j\frac{4\pi}{3}}\right] \tag{3.3}$$

$$\because \cos(\theta) = \frac{e^{j\theta} + e^{-j\theta}}{2} \tag{3.4}$$

$$\begin{aligned}\therefore \vec{f}(t) = \frac{1}{3}\hat{f}[&e^{j0}\left(e^{j\psi} + e^{-j\psi}\right) + e^{j\frac{2\pi}{3}}\left(e^{j\psi - j\frac{2\pi}{3}} + e^{-j\psi + j\frac{2\pi}{3}}\right) \\ &+ e^{j\frac{4\pi}{3}}\left(e^{j\psi - j\frac{4\pi}{3}} + e^{-j\psi + j\frac{4\pi}{3}}\right)]\end{aligned} \tag{3.5}$$

$$\vec{f}(t) = \frac{1}{3}\hat{f}\left[\left(e^{j\psi} + e^{-j\psi}\right) + \left(e^{j\psi} + e^{-j\psi + j\frac{4\pi}{3}}\right) + \left(e^{j\psi} + e^{-j\psi + j\frac{2\pi}{3}}\right)\right] \tag{3.6}$$

$$\vec{f}(t) = \frac{1}{3}\hat{f}\left[3e^{j\psi} + e^{-j\psi}\left(1 + e^{j\frac{4\pi}{3}} + e^{j\frac{2\pi}{3}}\right)\right] \tag{3.7}$$

$$\because 1 + e^{j\frac{2\pi}{3}} + e^{j\frac{4\pi}{3}} \equiv 0, \qquad \psi = \omega t + \theta_0 \tag{3.8}$$

$$\therefore \vec{f}(t) = \hat{f}e^{j\omega t + \theta_0} = \left(\hat{f}e^{\theta_0}\right)e^{j\omega t} = \underline{f}\, e^{j\omega t} \tag{3.9}$$

Or in summary, the balanced three-phase function can be represented in the complex plane with a complex vector, $\underline{f}$, that has the same length as the amplitude of the sinusoidal functions, $\hat{f}$. This vector rotates at the same frequency, ω, of the sinusoidal functions.

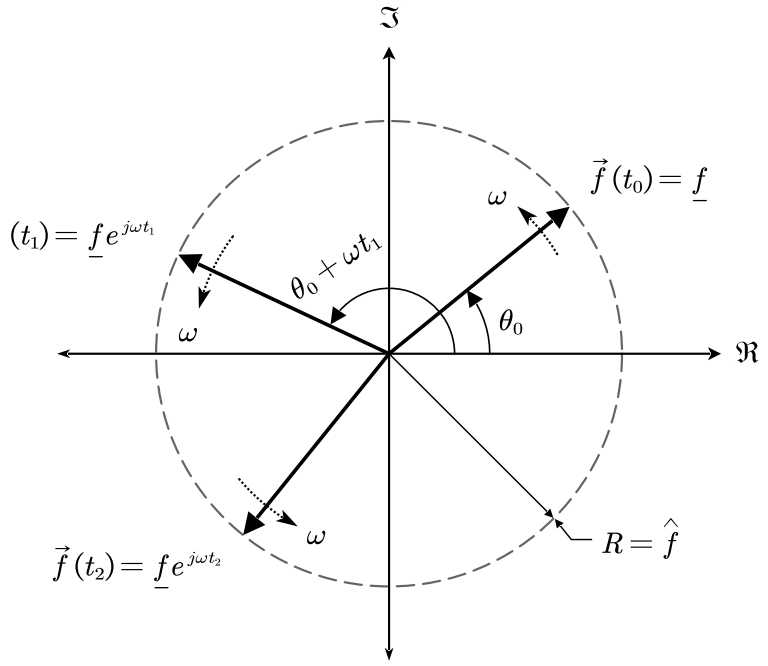

Figure 3.2: Rotating space-phasor in the complex plane.

It should be noted that the three-phase function can be referred to as the *abc*-frame. The space-phasor equation is not limited to a fixed amplitude, $\hat{f}$, nor frequency, ω. Rather, it can be extended to a more general form with a variable amplitude, $\hat{f}(t)$, and variable frequency, $\omega(t)$ [97], where

$$\theta(t) = \theta_0 + \int_0^t \omega(\tau)\, d\tau \tag{3.10}$$

By replacing ωt in (3.9) with $\int_0^t \omega(\tau)\, d\tau$ the general form of the space-phasor definition becomes

$$\vec{f}(t) = \left(\hat{f}(t)e^{\theta_0}\right)e^{j\left(\int_0^t \omega(\tau)\, d\tau\right)} = \hat{f}(t)e^{j\left(\theta_0 + \int_0^t \omega(\tau)\, d\tau\right)} \tag{3.11}$$

Then, using definition in (3.10), (3.11) becomes

$$\vec{f}(t) = \hat{f}(t)e^{j\theta(t)} \tag{3.12}$$

The same can be extended to the *abc*-frame in (3.1), and can be more concisely written as

$$\boldsymbol{f}_{abc} = \begin{bmatrix} f_a(t) \\ f_b(t) \\ f_c(t) \end{bmatrix} = \hat{f}(t) \begin{bmatrix} \cos\big(\theta(t)\big) \\ \cos\left(\theta(t) - \frac{2\pi}{3}\right) \\ \cos\left(\theta(t) - \frac{4\pi}{3}\right) \end{bmatrix} \tag{3.13}$$

$$\boldsymbol{f}_{abc} = \hat{f}(t)\boldsymbol{D}(t) \tag{3.14}$$

It is useful to define the transformation between the space-phasor and *abc*-frame, or any two different frames for that matter, as a linear equation with a transformation matrix. The transformation from the *abc*-frame to the space-phasor that results in (3.9) can be calculated by

$$\vec{f}(t) = \frac{2}{3} \begin{bmatrix} 1 \\ e^{j\frac{2\pi}{3}} \\ e^{j\frac{4\pi}{3}} \end{bmatrix}^T \begin{bmatrix} f_a(t) \\ f_b(t) \\ f_c(t) \end{bmatrix} \tag{3.15}$$

$$\vec{f}(t) = \frac{2}{3} \boldsymbol{C}_{sp,abc}^T \begin{bmatrix} f_a(t) \\ f_b(t) \\ f_c(t) \end{bmatrix} \tag{3.16}$$

$$\vec{f}(t) = \frac{2}{3} \boldsymbol{C}_{sp,abc}^T \boldsymbol{f}_{abc} \tag{3.17}$$

While going from the space-phasor to the *abc*-frame can be done with

$$\begin{bmatrix} f_a(t) \\ f_b(t) \\ f_c(t) \end{bmatrix} = Re\left\{ \begin{bmatrix} \vec{f}(t) \\ \vec{f}(t)e^{-j\frac{2\pi}{3}} \\ \vec{f}(t)e^{-j\frac{4\pi}{3}} \end{bmatrix} \right\} \tag{3.18}$$

Where $Re\{.\}$ is the real-component operator. It is also useful to represent these transformations as signal blocks to be used in block diagrams. Figure 3.3 (a) and (b) represents the transformation made by (3.15) and (3.18) respectively.

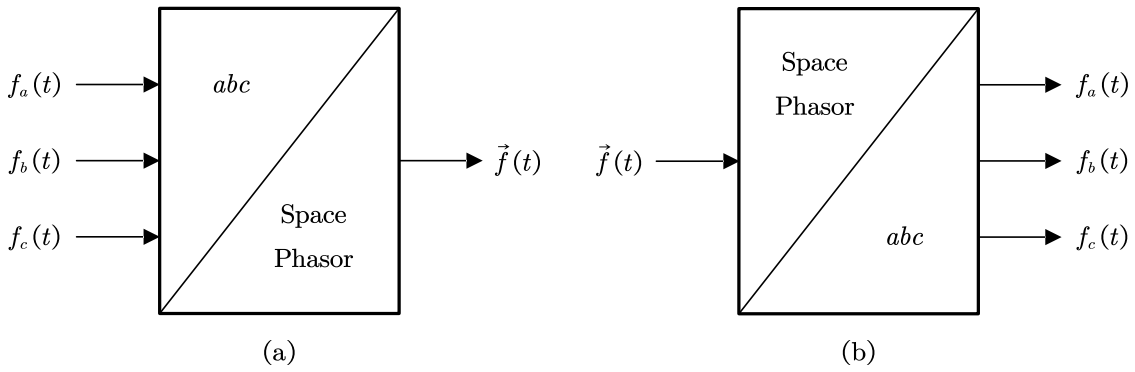

Figure 3.3: Signal transformation blocks (a) *abc*-frame to space-phasor (b) space-phasor to *abc*-frame

While the space-phasor representation reduces the size of the equation compared to the *abc*-frame, and allows for easier interpretation of the amplitude, phase, and frequency of the signal, it has its limitations. The signal transformation only applies to a balanced, or symmetrical, three-phase signal. A balanced three-phase signal is where all three phases have the same amplitude, and their angles are equally separated by $\frac{2\pi}{3}$ rad.

Therefore, it cannot be used for unbalanced three-phase signals which are critical to the goals of this work. Not to mention that many practical applications require working with unbalanced signals. Furthermore, it can be inconvenient to control systems or circuits with a polar quantity like the space-phasor. Instead, using a frame that is cartesian in nature, and deals with real-value functions, is preferred.

3.1.2 Stationary frame

To address some of the drawback of the space-phasor, the three-phase signal will be transformed into a two-dimensional frame that is based on the space-phasor. One of the candidates is the $\alpha\beta$-frame. Another name for it is the stationary frame. It is also known as the Clarke transformation [98].

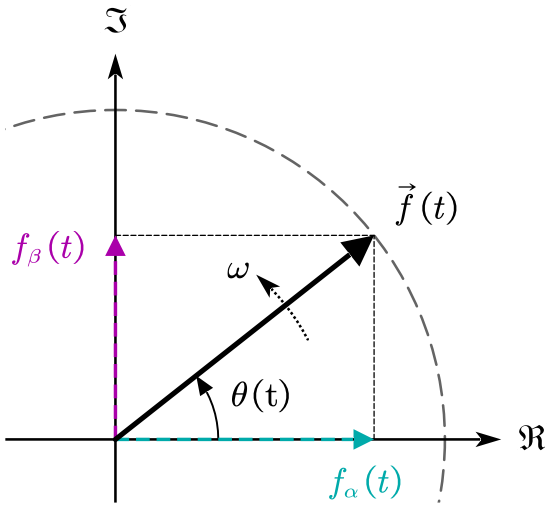

Figure 3.4: $\alpha\beta$ projection of space-phasor.

The transformation begins by defining the projection of the space-phasor $\vec{f}(t)$ onto the real-axis, $\mathfrak{R}$, as $f_\alpha(t)$, while its projection on the imaginary-axis, $\mathfrak{I}$, as $f_\beta(t)$, as seen in Figure 3.4. Therefore

$$\vec{f}(t) = f_\alpha(t) + j f_\beta(t) \tag{3.19}$$

Using basic trigonometry, it can be seen that

$$f_\alpha(t) = \hat{f}(t)\cos\big(\theta(t)\big) \tag{3.20}$$

$$f_\beta(t) = \hat{f}(t)\sin\big(\theta(t)\big) \tag{3.21}$$

$$\begin{bmatrix} f_\alpha(t) \\ f_\beta(t) \end{bmatrix} = \hat{f}(t)\begin{bmatrix} \cos\big(\theta(t)\big) \\ \sin\big(\theta(t)\big) \end{bmatrix} \tag{3.22}$$

One way to transform a three-phase signal to the $\alpha\beta$-frame is to use the transformation of the *abc*-frame to space-phasor as an intermediary step. Equating (3.19) with (3.2)

$$f_\alpha(t) + j f_\beta(t) = \frac{2}{3}\left[f_a(t)e^{j0} + f_b(t)e^{j\frac{2\pi}{3}} + f_c(t)e^{j\frac{4\pi}{3}}\right] \tag{3.23}$$

$$f_\alpha(t) + j f_\beta(t) = \frac{2}{3}[f_a(t)\big(\cos(0) + j\sin(0)\big) + f_b(t)\left(\cos\left(\frac{2\pi}{3}\right) + j\sin\left(\frac{2\pi}{3}\right)\right) + f_c(t)\left(\cos\left(\frac{4\pi}{3}\right) + j\sin\left(\frac{4\pi}{3}\right)\right)] \quad (3.24)$$

Equating the real components of each side together, and imaginary components of each side together

$$f_\alpha(t) = \frac{2}{3}\left[f_a(t)\cos(0) + f_b(t)\cos\left(\frac{2\pi}{3}\right) + f_c(t)\cos\left(\frac{4\pi}{3}\right)\right],$$
$$f_\beta(t) = \frac{2}{3}\left[f_a(t)\sin(0) + f_b(t)\sin\left(\frac{2\pi}{3}\right) + f_c(t)\sin\left(\frac{4\pi}{3}\right)\right] \quad (3.25)$$

$$f_\alpha(t) = \frac{2}{3}\left[f_a(t) - \frac{1}{2}f_b(t) - \frac{1}{2}f_c(t)\right],$$
$$f_\beta(t) = \frac{2}{3}\left[0 + \frac{\sqrt{3}}{2}f_b(t) - \frac{\sqrt{3}}{2}f_c(t)\right] \quad (3.26)$$

$$\therefore \begin{bmatrix} f_\alpha(t) \\ f_\beta(t) \end{bmatrix} = \frac{2}{3}\begin{bmatrix} 1 & -\frac{1}{2} & -\frac{1}{2} \\ 0 & \frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2} \end{bmatrix}\begin{bmatrix} f_a(t) \\ f_b(t) \\ f_c(t) \end{bmatrix} \quad (3.27)$$

$$\boldsymbol{f}_{\alpha\beta} = \boldsymbol{C}_{abc}^{\alpha\beta}\begin{bmatrix} f_a(t) \\ f_b(t) \\ f_c(t) \end{bmatrix} \quad (3.28)$$

$$\boldsymbol{f}_{\alpha\beta} = \boldsymbol{C}_{abc}^{\alpha\beta}\boldsymbol{f}_{abc} \quad (3.29)$$

And similarly, the *abc*-frame can be calculated from the *αβ*-frame using the inverse Clarke transformation

$$\boldsymbol{f}_{abc} = \boldsymbol{C}_{\alpha\beta}^{abc}\boldsymbol{f}_{\alpha\beta} \quad (3.30)$$

To find the inverse transformation matrix, it is necessary to find a matrix $\boldsymbol{C}_{\alpha\beta}^{abc}$ such that

$$\boldsymbol{C}_{abc}^{\alpha\beta}\boldsymbol{C}_{\alpha\beta}^{abc} = \begin{bmatrix} 1 & 0 \\ 0 & 1 \end{bmatrix} \tag{3.31}$$

Assume that $\boldsymbol{C}_{\alpha\beta}^{abc}$ has the form

$$\boldsymbol{C}_{\alpha\beta}^{abc} = \begin{bmatrix} A & B \\ C & D \\ E & F \end{bmatrix} \tag{3.32}$$

Then, the solution can be found by plugging in two different values for $\theta(t)$ in (3.29), then taking in the resulting $\boldsymbol{f}_{\alpha\beta}$ and $\boldsymbol{f}_{abc}$ and plugging them into (3.30). This results in

$$\theta(t) = 0 \Longrightarrow \hat{f}\begin{bmatrix} 1 \\ -\frac{1}{2} \\ -\frac{1}{2} \end{bmatrix} = \begin{bmatrix} A & B \\ C & D \\ E & F \end{bmatrix} \hat{f}\begin{bmatrix} 1 \\ 0 \end{bmatrix}, \tag{3.33}$$

$$\therefore \begin{bmatrix} A \\ C \\ E \end{bmatrix} = \begin{bmatrix} 1 \\ -\frac{1}{2} \\ -\frac{1}{2} \end{bmatrix} \tag{3.34}$$

$$\theta(t) = \frac{\pi}{2} \Longrightarrow \hat{f}\begin{bmatrix} 0 \\ \frac{\sqrt{3}}{2} \\ -\frac{\sqrt{3}}{2} \end{bmatrix} = \begin{bmatrix} A & B \\ C & D \\ E & F \end{bmatrix} \hat{f}\begin{bmatrix} 0 \\ 1 \end{bmatrix} \tag{3.35}$$

$$\therefore \begin{bmatrix} B \\ D \\ F \end{bmatrix} = \begin{bmatrix} 0 \\ \frac{\sqrt{3}}{2} \\ -\frac{\sqrt{3}}{2} \end{bmatrix} \tag{3.36}$$

$$\boldsymbol{C}_{\alpha\beta}^{abc} = \begin{bmatrix} A & B \\ C & D \\ E & F \end{bmatrix} = \begin{bmatrix} 1 & 0 \\ -\frac{1}{2} & \frac{\sqrt{3}}{2} \\ -\frac{1}{2} & -\frac{\sqrt{3}}{2} \end{bmatrix} \tag{3.37}$$

Plugging in the obtained value for $\boldsymbol{C}_{\alpha\beta}^{abc}$ into (3.31) proves the matrix to be correct

$$\boldsymbol{C}_{abc}^{\alpha\beta}\boldsymbol{C}_{\alpha\beta}^{abc} = \frac{2}{3}\begin{bmatrix} 1 & -\frac{1}{2} & -\frac{1}{2} \\ 0 & \frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2} \end{bmatrix}\begin{bmatrix} 1 & 0 \\ -\frac{1}{2} & \frac{\sqrt{3}}{2} \\ -\frac{1}{2} & -\frac{\sqrt{3}}{2} \end{bmatrix} = \frac{2}{3}\begin{bmatrix} \frac{3}{2} & 0 \\ 0 & \frac{3}{2} \end{bmatrix} = \begin{bmatrix} 1 & 0 \\ 0 & 1 \end{bmatrix}\blacksquare \qquad (3.38)$$

The signal block diagrams for the Clarke transformation (3.29) and inverse Clarke transformation (3.30) are shown in Figure 3.5 (a) and (b), respectively.

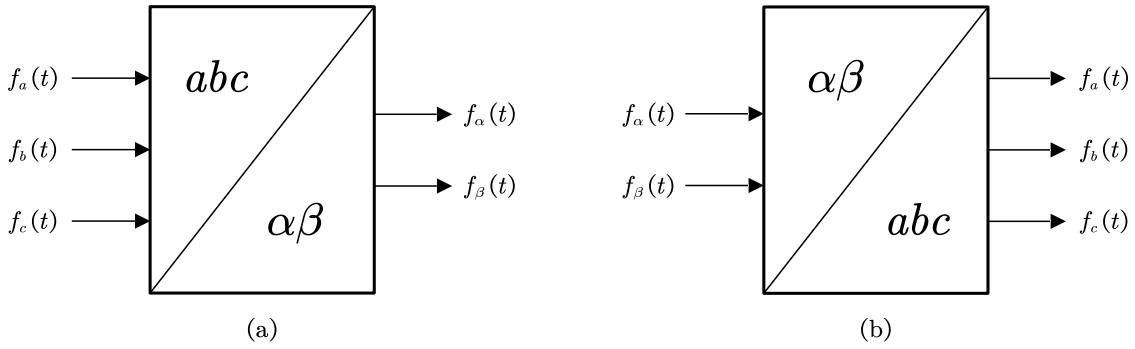

Figure 3.5: Signal transformation blocks (a) *abc*-frame to *αβ*-frame (b) *αβ*-frame to *abc*-frame

As it can be inferred by (3.29), the three-phase sinusoidal signals are reduced to two sinusoidal signals. For example, the Clarke transformation of the signals shown in Figure 3.1 is shown in Figure 3.6.

In practice, this means that the voltage or current can be controlled using two controllers instead of three. However, the signals are still in sinusoidal form, which require more complex controllers compared to DC signals.

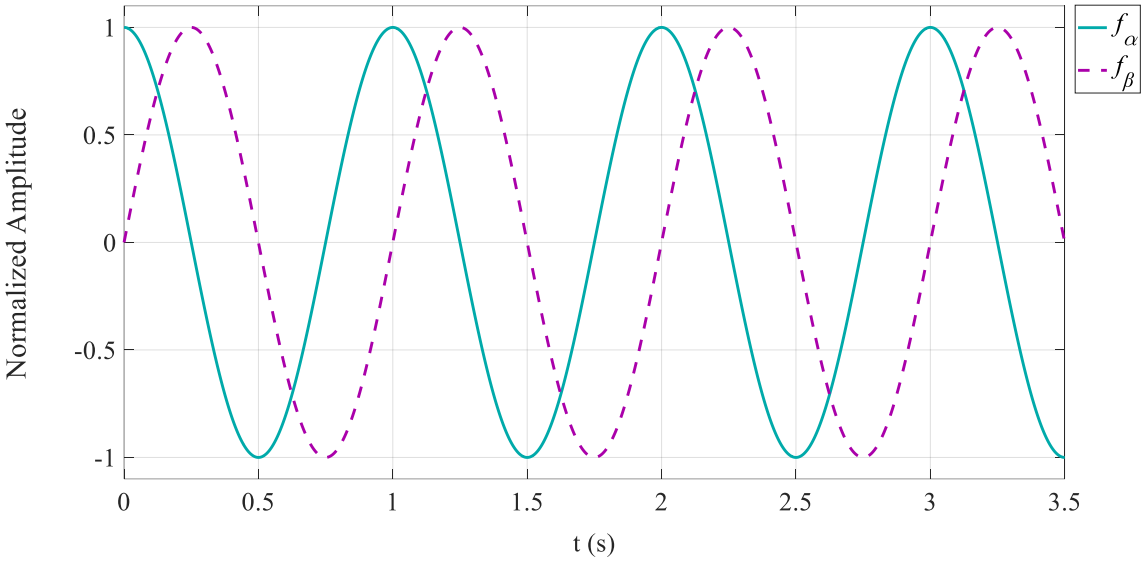

Figure 3.6: Clarke Transformation of a balanced three-phase sinusoidal signal

3.1.3 Synchronous frame

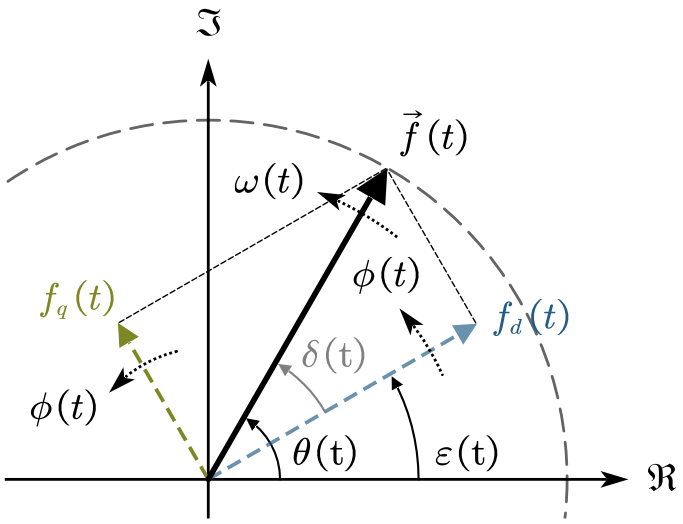

Figure 3.7: Rotating *dq*-frame in the complex plane

It is possible to convert these sinusoidal signals into a DC form. By having the $\alpha\beta$-frame rotate along with the space phasor, the perpendicular components of this frame would remain constant. This frame is known as a rotating frame, synchronous frame, or simply, the *dq*-frame. There are different conventions in literature for which axis is assigned as the

direct (d) or quadrature (q) axis. The convection chosen here is where the real component, or cosine projection, of the space-phasor is assigned as the d-axis. The q-axis is assigned the imaginary component, or the sine projection. Using trigonometry, it can be surmised from Figure 3.7 that

$$\hat{f} = \sqrt{f_d^2 + f_q^2} \tag{3.39}$$

$$f_d = \hat{f}\cos(\delta) \tag{3.40}$$

$$f_q = \hat{f}\sin(\delta) \tag{3.41}$$

$$\delta = \cos^{-1}\left(\frac{f_d}{\hat{f}}\right) = \cos^{-1}\left(\frac{f_d}{\sqrt{f_d^2 + f_q^2}}\right) \tag{3.42}$$

According to Figure 3.7, the dq-frame can be described as a stationary frame, like the $\alpha\beta$-frame, rotating at angular speed of $\Phi(t)$. The angle of the direct axis is $\varepsilon(t)$, where

$$\varepsilon(t) = \varepsilon_0 + \int_0^t \Phi(\tau)\, d\tau \tag{3.43}$$

The angle between the direct axis and the space-phase is $\delta(t)$, where

$$\delta(t) = \theta(t) - \varepsilon(t) \tag{3.44}$$

As such, the dq-frame can be mathematically equated to the space-phasor as

$$\vec{f}(t) = [f_d(t) + j f_q(t)]e^{j\varepsilon(t)} \tag{3.45}$$

Plugging (3.45) into (3.23.24)

$$[f_d(t) + j f_q(t)]e^{j\varepsilon(t)} = \frac{2}{3}\left[f_a(t)e^{j0} + f_b(t)e^{j\frac{2\pi}{3}} + f_c(t)e^{j\frac{4\pi}{3}}\right] \tag{3.46}$$

$$f_d(t) + jf_q(t) = \frac{2}{3}\left[f_a(t)e^{j0} + f_b(t)e^{j\frac{2\pi}{3}} + f_c(t)e^{j\frac{4\pi}{3}}\right]e^{-j\varepsilon(t)} \tag{3.47}$$

$$f_d(t) + jf_q(t) = \frac{2}{3}\left[f_a(t)e^{-j\varepsilon(t)} + f_b(t)e^{j\left(\frac{2\pi}{3}-\varepsilon(t)\right)} + f_c(t)e^{j\left(\frac{4\pi}{3}-\varepsilon(t)\right)}\right] \tag{3.48}$$

$$\begin{aligned} f_d(t) + jf_q(t) = \frac{2}{3}[&f_a(t)\left(\cos\left(-\varepsilon(t)\right) + j\sin\left(-\varepsilon(t)\right)\right) \\ &+f_b(t)\left(\cos\left(\frac{2\pi}{3}-\varepsilon(t)\right) + j\sin\left(\frac{2\pi}{3}-\varepsilon(t)\right)\right) \\ &+f_c(t)\left(\cos\left(\frac{4\pi}{3}-\varepsilon(t)\right) + j\sin\left(\frac{4\pi}{3}-\varepsilon(t)\right)\right)] \end{aligned} \tag{3.49}$$

$$f_d(t) = \frac{2}{3}\left[f_a(t)\cos\left(-\varepsilon(t)\right) + f_b(t)\cos\left(\frac{2\pi}{3}-\varepsilon(t)\right) + f_c(t)\cos\left(\frac{4\pi}{3}-\varepsilon(t)\right)\right],$$

$$f_q(t) = \frac{2}{3}\left[f_a(t)\sin\left(-\varepsilon(t)\right) + f_b(t)\sin\left(\frac{2\pi}{3}-\varepsilon(t)\right) + f_c(t)\sin\left(\frac{4\pi}{3}-\varepsilon(t)\right)\right] \tag{3.50}$$

$$\therefore \begin{bmatrix} f_d(t) \\ f_q(t) \end{bmatrix} = \frac{2}{3}\begin{bmatrix} \cos\left(\varepsilon(t)\right) & \cos\left(\varepsilon(t)-\frac{2\pi}{3}\right) & \cos\left(\varepsilon(t)-\frac{4\pi}{3}\right) \\ -\sin\left(\varepsilon(t)\right) & -\sin\left(\varepsilon(t)-\frac{2\pi}{3}\right) & -\sin\left(\varepsilon(t)-\frac{4\pi}{3}\right) \end{bmatrix}\begin{bmatrix} f_a(t) \\ f_b(t) \\ f_c(t) \end{bmatrix} \tag{3.51}$$

$$\begin{bmatrix} f_d(t) \\ f_q(t) \end{bmatrix} = \boldsymbol{T}_{abc}^{dq}[\varepsilon(t)]\begin{bmatrix} f_a(t) \\ f_b(t) \\ f_c(t) \end{bmatrix} \tag{3.52}$$

$$\boldsymbol{f}_{dq} = \boldsymbol{T}_{abc}^{dq}[\varepsilon(t)]\boldsymbol{f}_{abc} \tag{3.53}$$

Equation (3.53) is known as the Park transformation [99]. It's important to be able to convert *dq*-frame signals into the *abc*-frame to produce the three-phase voltage or current required for the grid. This is done through the inverse Park transformation

$$\boldsymbol{f}_{abc} = \boldsymbol{T}_{dq}^{abc}\boldsymbol{f}_{dq} \tag{3.54}$$

The inverse transformation matrix is the transpose of the transformation matrix, $\boldsymbol{T}_{abc}^{dq}$ [8]

$$\boldsymbol{T}_{dq}^{abc}[\varepsilon(t)] = \boldsymbol{T}_{abc}^{dq}[\varepsilon(t)]^T = \begin{bmatrix} \cos(\varepsilon(t)) & \sin(\varepsilon(t)) \\ \cos\left(\varepsilon(t) - \frac{2\pi}{3}\right) & \cos\left(\varepsilon(t) - \frac{4\pi}{3}\right) \\ \sin\left(\varepsilon(t) - \frac{2\pi}{3}\right) & \sin\left(\varepsilon(t) - \frac{4\pi}{3}\right) \end{bmatrix} \tag{3.55}$$

The signal block diagrams for the Park transformation (3.53) and inverse Park transformation (3.54) are shown in Figure 3.8 (a) and (b), respectively.

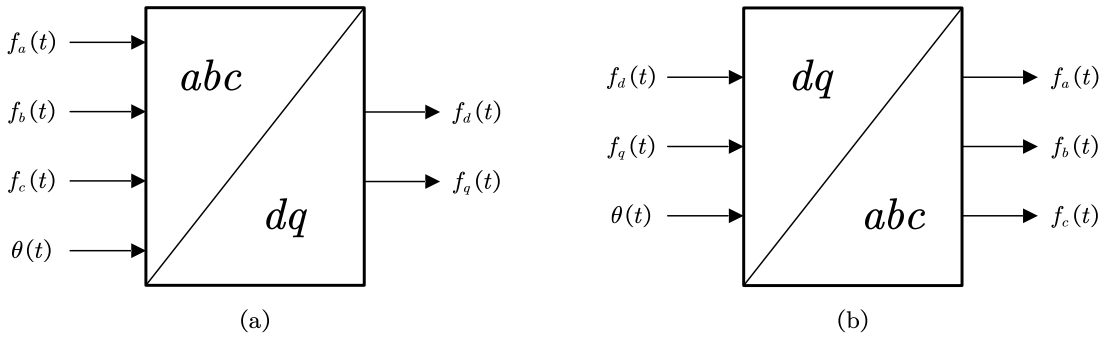

Figure 3.8: Signal transformation blocks (a) *abc*-frame to *dq*-frame (b) *dq*-frame to *abc*-frame

For the *dq*-frame to become synchronous and produce the required DC signals, $\Phi(t)$ must be made equal to $\omega(t)$. This can be achieved by using a Frequency-Locked Loop (FLL).

However, for the control scheme proposed here, the output voltage should be *phase* synchronized with the grid. This requires the use of a Phase-Locked Loop (PLL). The PLL adjusts the frequency, $\Phi(t)$, and the phase, ε_0 of the *dq*-frame so that they become equal to $\omega(t)$, and θ_0, respectively. Or in other words, δ is set to zero.

A typical PLL is shown in Figure 3.9. There are various PLL designs in the literature, but the proposed control schemed does not require any advanced or exotic designs. In fact, since the signals are properly filtered, as will be explained later, even a simple proportional controller can be adequate. That is because of the integrator term that follows the proportional controller. This eliminates the steady-state error of the outputted angle.

Since the objective is maintaining δ at zero, then according to (3.41)

$$f_q = \hat{f}\sin(\delta) = \hat{f}\sin(0) = 0 \tag{3.56}$$

Therefore, the compensator takes in $f_q$and adjusts the frequency, ω, until f_q becomes zero. A saturation block is added to maintain ω within reasonable range. A wrapping integrator, or a voltage-controlled oscillator (VCO), integrates the value of ω coming out of the saturation block to produce the angle, θ. The angle is limited to the range $[0,2\pi)$. Any value of θ greater than the upper bound is wrapped to zero, while any value lesser than the lower bound is wrapped to 2π. Then the angle is fed back into the Park transformation block, which calculates f_q, which feeds back into the compensator, closing the loop.

The information laid in here thus far is crucial to the understanding of the proposed control scheme. The reason being that the entirety of the controllers' design will be in the *dq*-frame.

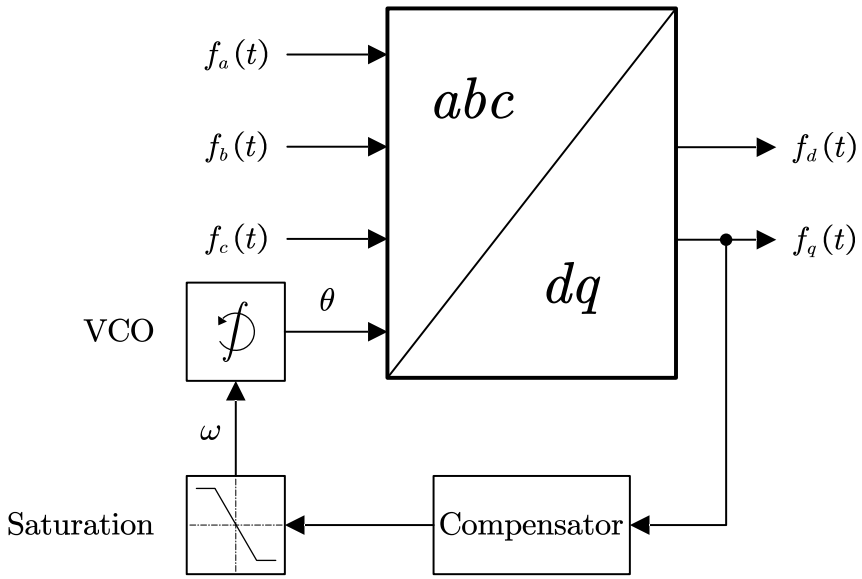

Figure 3.9: Park Transformation with PLL

The transformation of the signal shown in Figure 3.1 into a phase-locked dq-frame is shown in Figure 3.10.

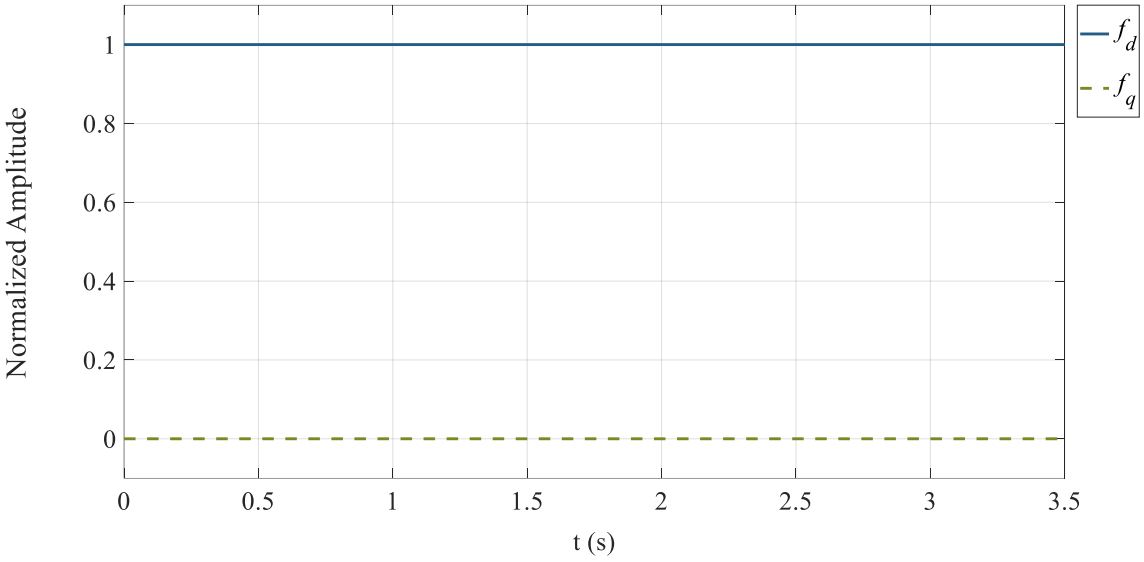

Figure 3.10: Park Transformation of a balanced three-phase sinusoidal signal

Furthermore, it is useful to define the orthogonal dq-frame that corresponds to the orthogonal of a phasor, $\vec{f}_{\perp}$. In this thesis, the convention for $\vec{f}_{\perp}$ will be defined as the *lagging* orthogonal phasor. Therefore, $\vec{f}_{\perp}$ can be represented in the dq-frame as

$$\vec{f}_{\perp} = \begin{bmatrix} -f_q \\ f_d \end{bmatrix} \tag{3.57}$$

3.2 The Droop Coordination Method

In a conventional AC grid, the centralized generation station acts as a stiff grid, or an infinite bus. That is, it maintains a constant voltage amplitude and frequency. The MG usually operates while being connected to this infinite bus, and thus have its frequency and voltage amplitude fixed by this bus. The DGs operate in constant-power mode to contribute to the power generation.

However, in some cases, the MG needs to disconnect, or is forcefully disconnected, from the stiff grid. When that occurs, the MG enters the islanding mode. In this mode, the DG become grid-forming, and they take up the responsibility of determining and maintaining the voltage amplitude and frequency. This is a trivial case when there is a single DG in the MG. The issue arises when there are multiple DGs connected to the same MG. In that case, there should be a method to coordinate the power generation between the DGs. Ideally, this method should be autonomous, decentralized, and communication-free. This is to increase the resilience and flexibility of the MG.

Luckily, such methods exist in the literature [16]. The conventional method is using droop control to coordinate the active and reactive power loading. Any device, like a DG, can measure a few variables locally. The most convenient ones to use for the droop method are the frequency. ω, and the voltage amplitude, $\hat{V}$. The frequency is a global variable. That is, no matter where it is measured in the MG, it measures equally. The voltage amplitude, however, is not global, but only local. This is due to the impedance in the transmission lines that leads to various voltage drops in different locations in the grid. Nevertheless, it makes for a good estimation of the state of the grid.

Ideally, the DGs should share their power in a proportional manner. That is, no matter the size of the DGs, all of them should contributing power of the same percentage as each other's rated power. For example, if the total load in the MG is equivalent to 30% of the total power rating of the DGs, then each DG should be loaded at 30% of their respective rated power. This can be expressed mathematically as

$$\frac{P_{DGx}}{P_{DGx}^{rated}} = \frac{P_{DGi}}{P_{DGi}^{rated}} \tag{3.58}$$

where P_{DGx} and P_{DGi} are the active power generated by the xth and ith DGs, respectively. P_{DGx}^{rated} and P_{DGi}^{rated} are the maximum active power that can be generated by the xth and ith DGs, respectively.

It is known that in grids where the line impedances are mostly inductive, the active power transfer is proportional to the power angle, δ. Meanwhile, the reactive power transfer is proportional to $\hat{V}$ [16]. That is

$$P \propto \delta,$$
$$Q \propto \hat{V} \tag{3.59}$$

As such, for the coordination method, ω should be used to coordinate the active power sharing, while $\hat{V}$ should govern the reactive power sharing. If the frequency of the grid is made variable, such as that it has a predefined minimum, ω_{min}, maximum, ω_{max}, and nominal, ω_{nom}, a slope can be defined to relate P with ω. This is known as the P-ω droop. The droop slope is defined as

$$\omega^* = \omega_{max} - m \cdot P \tag{3.60}$$

where ω^* is the reference frequency. It may also be referred to as ω^{ref}. And m is the droop coefficient. The value of m is calculated as

$$m = \frac{\omega_{max} - \omega_{min}}{P_{DG}^{rated}} \tag{3.61}$$

It can be seen that when P is zero, ω^* becomes equal to ω_{max}. On the other hand, when P reaches its maximum allowable value, ω^* becomes equal to ω_{min}. The slope representing (3.60) can be seen in Figure 3.11a.

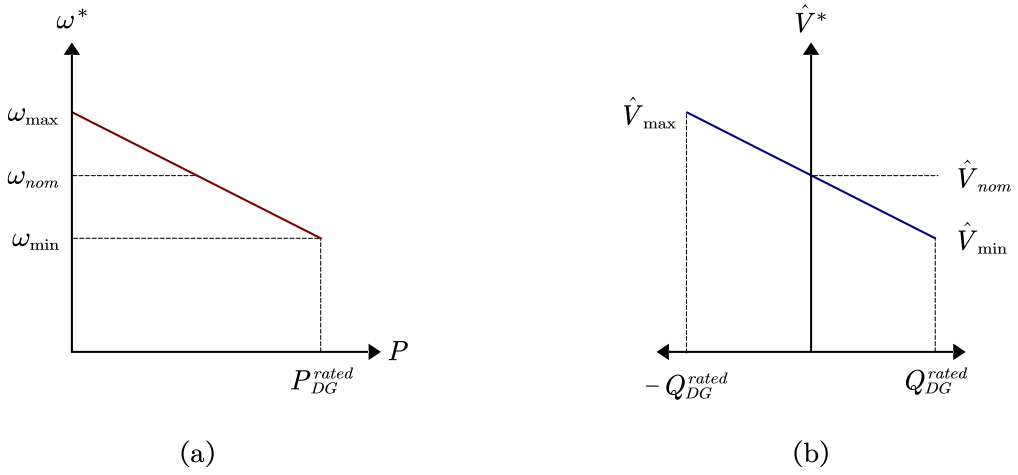

Figure 3.11: Droop slopes for (a) P-ω and (b) Q-$\hat{V}$

In practice, that translates to the DG adjusts ω^* depending how loaded it is. If the resulting ω^* happens to be less than the ω of the grid, this leads the DG to contribute less power to grid. That leads to other DGs contributing more power, and in return, decreasing their ω^*. In a sense, the DG "pulls down" the ω of the grid until all DGs are sharing power proportionally. The same concept applies if the DG is producing more proportional power than the other DGs, where it "pushes up" the ω of the grid.

Similarly, Q is related to $\hat{V}$ through the Q-$\hat{V}$ droop. The slope for this droop is defined as

$$\hat{V}^* = \hat{V}_{max} - n \cdot Q \tag{3.62}$$

where $\hat{V}^*$ is the reference frequency. It may also be referred to as V^{ref}. And n is the droop coefficient. The value of n is calculated as

$$n = \frac{\hat{V}_{max} - \hat{V}_{min}}{2Q_{DG}^{rated}} \tag{3.63}$$

It can be seen that when Q is zero, $\hat{V}^*$ becomes equal to $\hat{V}_{nom}$. On the other hand, when Q reaches its maximum allowable positive value, $\hat{V}^*$ becomes equal to $\hat{V}_{min}$. Meanwhile,

when the DG is consuming maximum Q, $\hat{V}^*$ becomes equal to $\hat{V}_{max}$. The slope representing (3.62) can be seen in Figure 3.11b.

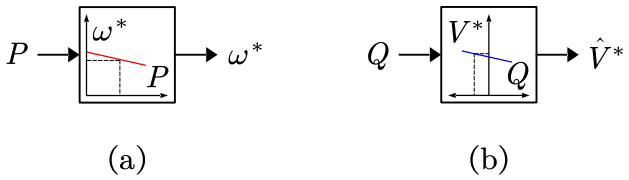

Figure 3.12: Block diagram representation of the (a) P-ω and (b) Q-$\hat{V}$ droop

There is a need to represent the droops as block diagrams for when controllers are explained in detail. The block diagrams for (3.60) and (3.62) can be seen Figure 3.12 (a) and (b), respectively.

3.3 Controller Design in the *dq*-Frame

3.3.1 The interlinking converter

The centerpiece of this thesis is the interlinking converter. Therefore, it is important to understand the structure of the converter, and how the controller is designed in the *dq*-frame. The IC is designed as a voltage source converter operating using current-mode control. As such, it includes a filtering inductor to smooth the output current, I. The output voltage, V_o, is measured after the inductor.

A controller sends a reference signal to the pulse width modulation (PWM) block. It converts the reference three-phase voltage to six PWM signals based on the DC voltage measurement, V_{DC}. The PWM signals control the six switches that compose the VSC to produce the required three-phase voltage. This can be seen in Figure 3.13.

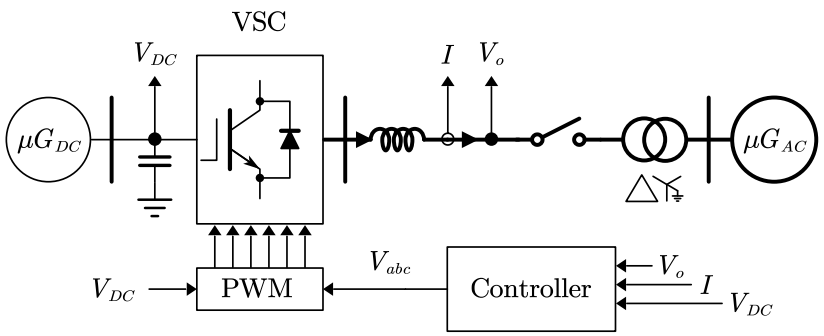

Figure 3.13: Simplified diagram of the interlinking converter

The IC connects to the DMG with a filtering capacitor. On the other side, it connects to the AMG through delta-wye transformer. This isolates the IC from any zero-sequence current. It should be noted that the thicker line on the AC-side indicates a three-phase line. As such, V_o and I in Figure 3.13 are three-phase quantities, each. A more detailed look at the controller is depicted in Figure 3.14.

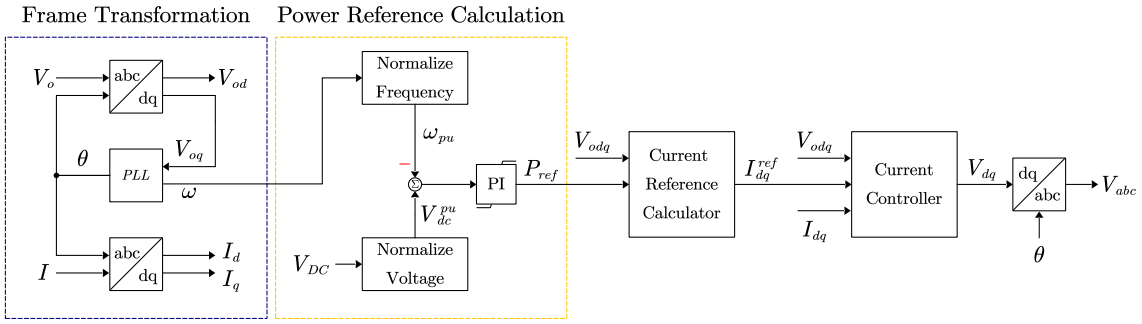

Figure 3.14: Detailed diagram of a typical IC controller

The controller takes in the measurements $V_o$and I, and uses the Park transformation to produce their dq-frame components, V_{odq} and I_{dq}, respectively. As explained in subsection 3.1.3, the PLL locks onto the phase of the grid, θ, and calculate the grid frequency, ω. These variables are passed to other parts of the control circuitry as required.

The IC's prime objective is to balance the loading between the two subgrids. To do that, it needs to be able to compare the two variables, one from each side. The AC-side's loading can be calculated from ω, as explained section 3.2. Similarly, the DC-side's loading can be determined from V_{DC}. However, it is not possible to compare two quantities that have different units. Therefore, they need to be transformed in a per unit basis for proper comparison purposes. The per unit frequency, ω_{pu}, can be calculated as [22]

$$\omega_{pu} = \frac{\omega - 0.5(\omega_{max} + \omega_{min})}{0.5(\omega_{max} - \omega_{min})} \tag{3.64}$$

where ω_{max} and ω_{min} are the predefined maximum and minimum allowable grid frequency, respectively. And similarly, the per unit DC voltage V_{DC}^{pu}, can be calculated as

$$V_{DC}^{pu} = \frac{V_{DC} - 0.5\left(V_{DC}^{max} + V_{DC}^{min}\right)}{0.5\left(V_{DC}^{max} - V_{DC}^{min}\right)} \tag{3.65}$$

where V_{DC}^{max} and V_{DC}^{min} are the predefined maximum and minimum allowable DC voltage, respectively. To ensure that the difference between these per unit quantities is eliminated, ω_{pu} is subtracted from V_{DC}^{pu}. Then, the difference is fed to a PI controller to maintain that difference at zero.

To do that, the PI controller sends out the reference active power, P_{ref}. Then, the reference current, I_{dq}^{ref}, to be fed to the current controller can be calculated from that. The active power, P, is defined as

$$P = \vec{V} \cdot \vec{I} \tag{3.66}$$

where $\vec{V}$ and $\vec{I}$ are the voltage phasor and the current phasor, in that order. Using (3.45), the active power can be calculated using dq-frame measurements as

$$P = \frac{3}{2}\begin{bmatrix} V_d & V_q \end{bmatrix}\begin{bmatrix} I_d \\ I_q \end{bmatrix} = \frac{3}{2}\left(V_d I_d + V_q I_q\right) \tag{3.67}$$

Since the PLL maintains V_q at zero, (3.67) can be reduced to

$$P = \frac{3}{2} V_d I_d \tag{3.68}$$

Therefore, the d component of the reference current, I_d^{ref} can be calculated with

$$I_d^{ref} = \frac{2}{3}\left(\frac{P_{ref}}{V_d}\right) \tag{3.69}$$

Similar steps can be taken to calculate the q component of the reference current, I_q^{ref}. The reactive power, Q, is defined as

$$Q = \vec{V} \cdot \vec{I}_{\perp} \tag{3.70}$$

Using (3.45), and the definition of orthogonal dq-frame in (3.57), the reactive power can be calculated using dq-frame measurements as

$$Q = \frac{3}{2}\begin{bmatrix} V_d & V_q \end{bmatrix}\begin{bmatrix} -I_q \\ I_d \end{bmatrix} = \frac{3}{2}\left(V_q I_d - V_d I_q\right) \tag{3.71}$$

Since the PLL maintains V_q at zero, (3.71) can be reduced to

$$Q = -\frac{3}{2} V_d I_q \tag{3.72}$$

Therefore, the q component of the reference current, I_q^{ref}, can be calculated with

$$I_q^{ref} = -\frac{2}{3}\left(\frac{P_{ref}}{V_q}\right) \tag{3.73}$$

However, in this case, the IC is set to produce unity power. That is, the reactive power reference, Q_{ref}, is set to zero. Therefore, I_q^{ref} will be fixed to zero. Thus, the equation for the reference current calculator is

$$I_{dq}^{ref} = \begin{bmatrix} I_d^{ref} \\ I_q^{ref} \end{bmatrix} = \begin{bmatrix} \frac{3P_{ref}}{2V_d} \\ 0 \end{bmatrix} \tag{3.74}$$

To regulate the output current, a current controller is used. Since all the input to the controller are in the dq-frame, PI controllers can be used to control the d and q components of the reference current.

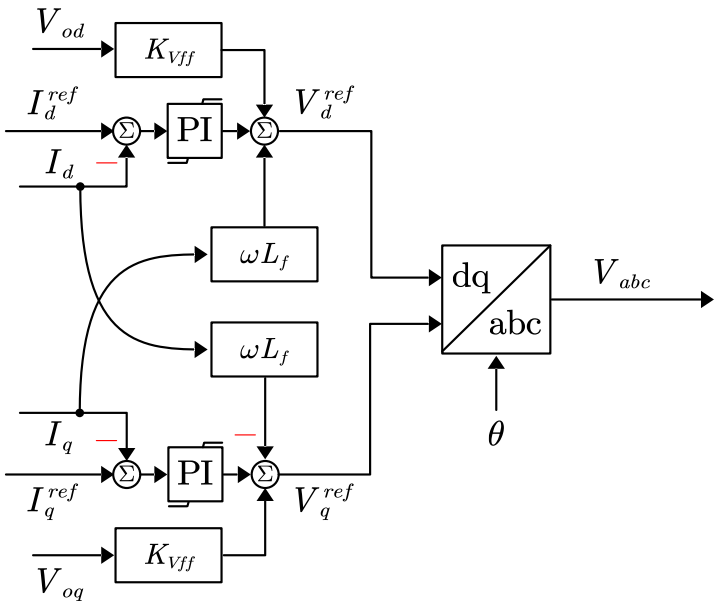

Figure 3.15: Detailed block diagram of the current controller of an IC

To decouple the d component from the influence of the q component due to the filtering inductor, I_q is multiplied with ω and the inductance value of the filtering inductor, L_f. Furthermore, to improve performance, V_o is fed forward through a feedforward filer. This

filter value can be tuned as desired and is optional. The structure of the current controller shown in Figure 3.14 is displayed in detail in Figure 3.15.

3.3.2 The distributed generator

DGs can take many forms and use different energy sources. Some DGs are electromechanical and are directly interfaced to the grid. For example, gas turbines, or diesel generators. However, the main concern in MGs is the use of electronically interfaced generators. One example of such type is a PV system, where a DC-DC converter is used to regulate the power output of PV panels. Another example is wind turbines, where the AC power generated by a synchronous generator is rectified to DC, then inverted to AC voltage suitable for the grid [100].

Therefore, the DGs in this thesis are modelled as electronically interfaced generators. The form they take is similar to ICs; a VSC. However, this VSC operates using voltage-mode control. Furthermore, the DGs are grid forming. As such, they have a filtering capacitor at the output of their AC-side for voltage support, in addition to a filtering inductor. The structure of the DG can be seen in Figure 3.16.

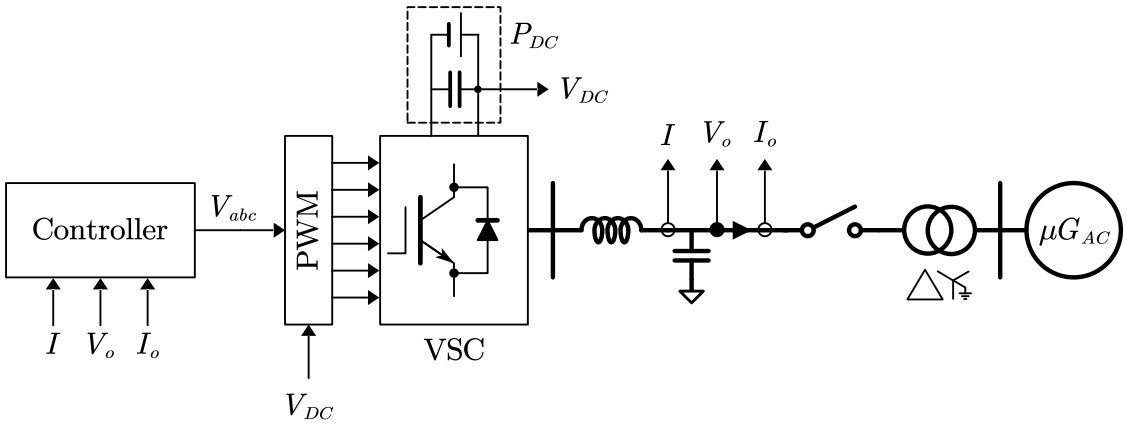

Figure 3.16: Simplified diagram of the distributed generator

The inductor current, I, is measured before the filtering capacitor. The output voltage and currents, V_o and I_o, respectively, are measure after the filtering capacitor. The DC-side of the VSC is the power source of the DG, P_{DG}. Its voltage is measured as V_{DC}. Similar to the case of the IC, the controller of the DG takes in the measurements, and outputs a three-phase voltage signal, V_{abc} that is fed to a PWM block. Then, said block produces six PWM signals to transfer power from the DC power source to the grid. A detailed view of the controller for the DG can be observed in Figure 3.17.

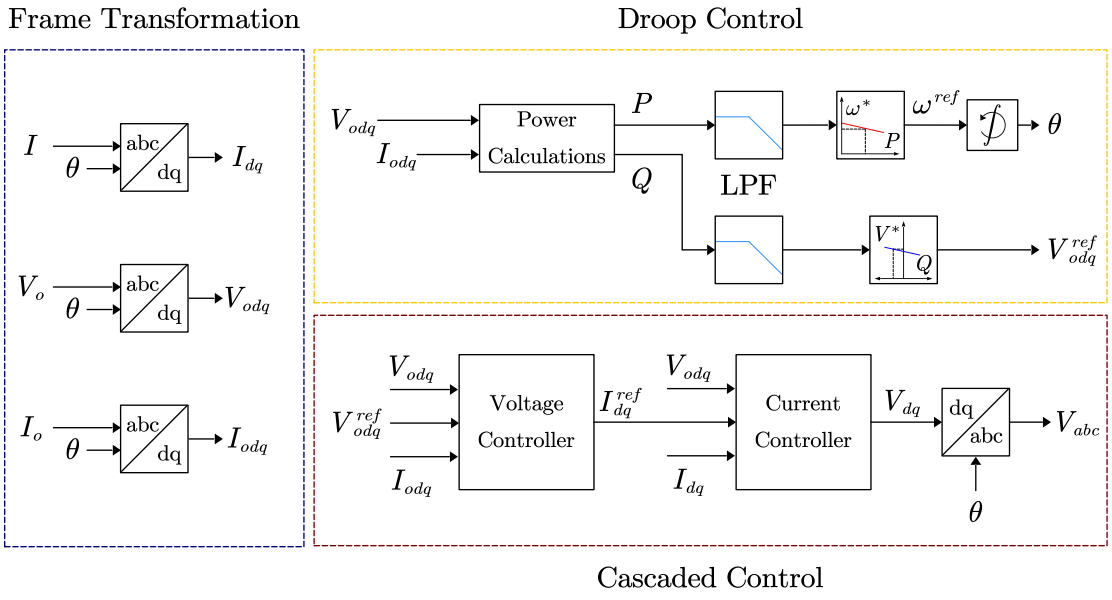

Figure 3.17: Detailed diagram of a typical DG controller

Frame transformation of the inputs is done through three Park transformation blocks. The angle fed into the block comes as a result of the P-ω droop in the droop control section.

The output voltage and current dq-frame quantities, V_{odq} and I_{odq}, respectively, are fed into the power calculations block. Using the equations (3.67) and (3.71), the active and reactive power of the DG are calculated. Their values are fed into low-pass filters (LPF). This helps slowdown the droop control to allow the cascaded control time to track the

reference voltage, V_{odq}^{ref}. As a rule of thumb, the droop control should be at least 10 time slower than the cascaded control.

Using the droop slopes, the reference frequency, ω^{ref}, and V_{odq}^{ref} are generated. A VCO is used to produce the phase angle, θ. This way, DGs do not require the use of PLLs as the droop control naturally tends to synchronize with the grid.

Then, V_{odq}^{ref} is fed into the cascaded control. Since the DG is a volage controlled VSC, there needs to be a controller for the voltage. This produces a reference current signal, I_{dq}^{ref}, that is sent to the current controller. Then, just like in the case of the IC, the current controller produces the voltage signal, V_{dq}, to be transformed into a three-phase voltage signal, V_{abc} that is fed into the PWM block to control the switches of the VSC. A detailed view of the cascaded control can be seen in Figure 3.18.

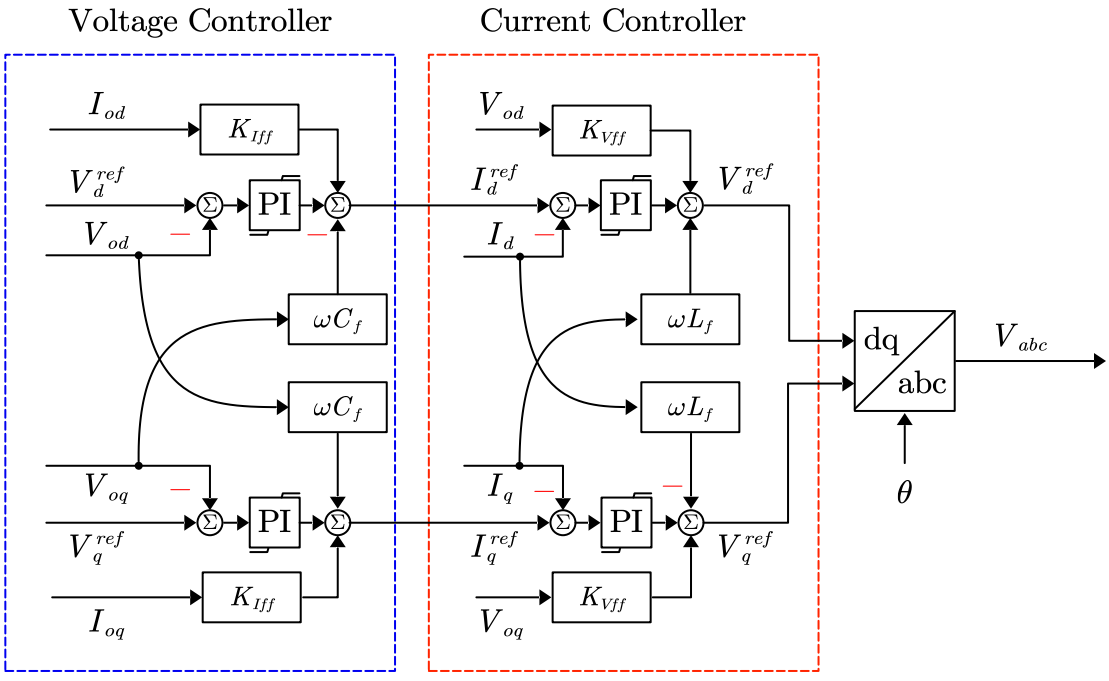

Figure 3.18: Detailed block diagram of the cascaded control of a DG

A prominent feature of the dq-frame is the simplicity and symmetry of the controller design. The current controller for the DG is identical to that of the IC, except for tuning parameters in some cases. Likewise, the voltage controller is identical to the current controller. The major differences are the usage of a current feedforward filter, the usage of the value of the output filter capacitor for the decoupling of the dq components, and the tuning parameter to achieve the desired performance and stability.

3.4 Symmetrical Components Decomposition

A typical assumption made when designing the control loops for power devices is that the grid is in a balanced condition. That is, the assumption of balanced voltages, currents, and loads. However, the proposed control scheme tackles an issue stemming from unbalanced conditions. Unbalanced conditions do not abide by the phase or amplitude rules set by balanced conditions. Phases can have varying amplitudes from one another, and they can be separated by arbitrary angles, as seen in Figure 3.19.

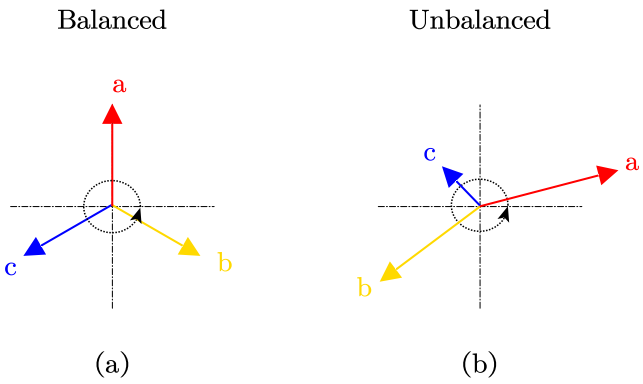

Figure 3.19: Comparison between (a) balanced and (b) unbalanced conditions

That leads to six variables that need to be accounted for, instead of two in the balanced condition. Furthermore, it is difficult to get intuitive understanding of the grid's condition

from these variables. Luckily, under that chaotic exterior lies a superposition of order. In any three-wire system with no faults, the unbalanced voltage or current can be decomposed into two independent, balanced sequences [101]. These are known as the positive sequence and negative sequence, as shown in Figure 3.20. It can also be represented as

$$f_{abc} = f_{abc}^{+} + f_{abc}^{-} \tag{3.75}$$

$$\begin{bmatrix} f_a \\ f_b \\ f_c \end{bmatrix} = \begin{bmatrix} f_a^{+} \\ f_b^{+} \\ f_c^{+} \end{bmatrix} + \begin{bmatrix} f_a^{-} \\ f_b^{-} \\ f_c^{-} \end{bmatrix} \tag{3.76}$$

$$\vec{f} = \overrightarrow{f^{+}} + \overrightarrow{f^{-}} \tag{3.77}$$

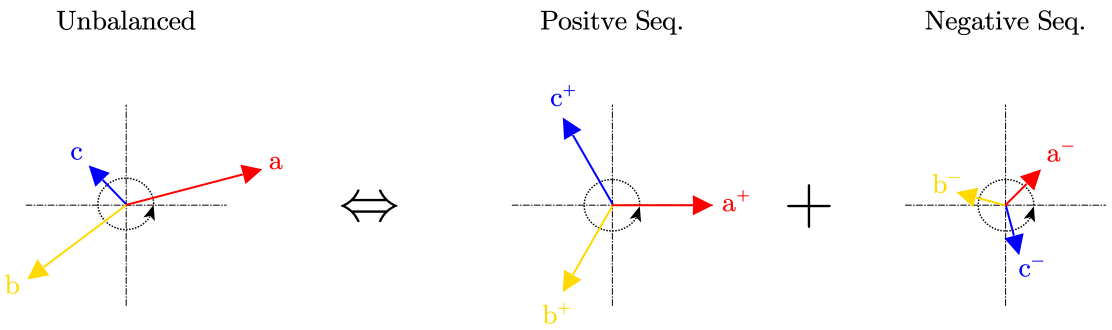

Figure 3.20: Symmetrical components decomposition of an unbalanced three-phase signal

The positive sequence component has a rotation sequence in the direction of the original signal (phase a, then b, then c), while the negative sequence component has a rotation sequence in the opposite direction (phase c, then b, then a).

It should be noted that there's a third sequence know as the zero sequence. However, all the controlled devices are connected to the grid with a delta-wye transformer. This eliminates any zero sequence components on the device-side of the transformer. Hence, the proposed control scheme ignores the existence of the zero sequence.

With that understanding in mind, the control of the unbalanced signal can be broken down into two decoupled control loops. This allows for the manipulation of the different facets of the unbalanced signal using two PI controller in place of one in the case of a balanced condition. This greatly simplifies the controller design process as both controllers are identical copies of each other, more or less. Figure 3.21 shows how a typical control loop designed for balanced condition can be adopted for unbalanced conditions.

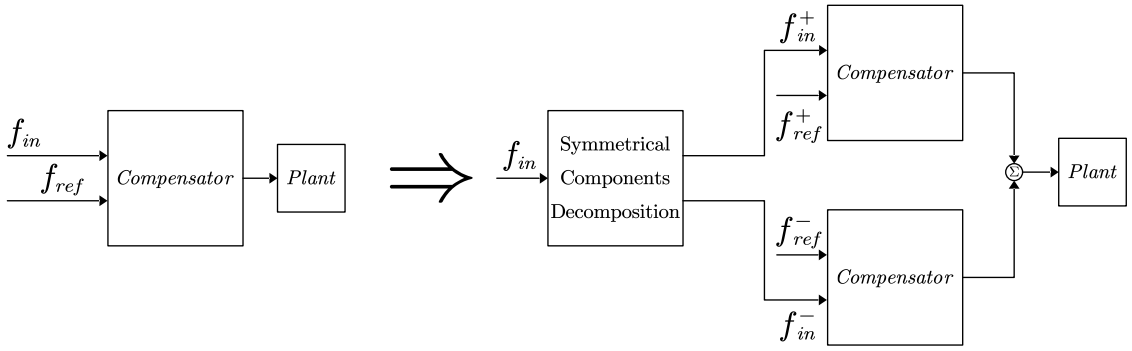

Figure 3.21: Adapting a generic controller for unbalanced conditions

Under the same purview, it is possible to breakdown the grid into superimposed grids, each for a symmetrical component. Figure 3.22 shows how a grid with an unbalanced load appears when decomposed into a grid for the positive sequence, and a grid for the negative sequence.

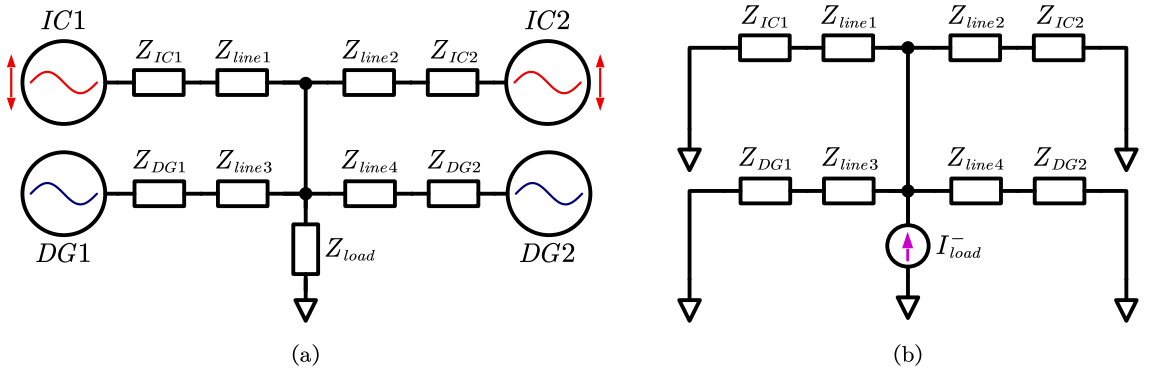

Figure 3.22: Sym. components decomposition of a grid. (a) Positive sequence. (b) Negative sequence

In this simplified MG, the DGs are grid forming and operate in voltage-controlled mode. The ICs are in current-controlled mode where they can source or sink current to and from the grid. Z_{load} is the unbalanced load.

Meanwhile, the unbalanced load appears as a current source in the negative sequence. Controllers that are designed to operate under balanced conditions make the power devices, such as ICs and DGs, appear in the negative sequence as a short circuit following their natural impedance . This negative sequence current, along with the impedances of the lines and devices, is what causes negative sequence voltages to appear at the buses of the grid. This negative sequence can cause undesirable and damaging effects, especially for three-phase motors as it is converted into mechanical vibrations and heat [102].

To eliminate the negative sequence voltage, the negative sequence current needs to be satisfied by either a DG or an IC. In the simplified AMG depicted in Figure 3.22, I_{load}^{-} will be divided over the DGs and IC inversely proportional to their respective total impedance, such that

$$I_{load,DGx}^{-} = I_{load}^{-} \frac{Z_T}{\left(Z_{line}^{x} + Z_{DG}^{x}\right) + Z_T} \tag{3.78}$$

Where $I_{load,DGx}^{-}$ is the negative sequence current flowing through a DG, Z_{line}^{x} is the total line impedance between the DG and the unbalanced load, and Z_{DG}^{x} is the natural impedance of the DG due to its interfacing filter, transformer, and other components. Z_T is the total summation of all impedances in the grid, excluding Z_{line}^{x} and Z_{DG}^{x}. Naturally, the ICs have their equivalent variables, and equation (3.78) applies to the ICs, as well.

CHAPTER 4
PROPOSED METHODOLOGY

In the previous chapter, the framework needed to implement the proposed methodology was laid down. This chapter builds on that knowledge with proposed improvement to the conventional methods with novel solutions. This way, the contribution of this work is made more apparent.

4.1 Problem Statement

Now that it is clear where negative sequence current voltage and current stem from, it is important to define the various forms of power produced by this sequence. Active power, P, was previously defined in (3.66). Under balanced conditions, each phasor is comprised of the positive sequence component only, and the definition in (3.66) is complete. But, as per (3.77), the phasors need to be expanded as [103]

$$P = \left(\overrightarrow{V^+} + \overrightarrow{V^-}\right) \cdot \left(\overrightarrow{I^+} + \overrightarrow{I^-}\right) \tag{4.1}$$

This splits the definition of real power into four terms

$$P = \overbrace{\underbrace{\left(\overrightarrow{V^+} \cdot \overrightarrow{I^+}\right)}_{P^+} + \underbrace{\left(\overrightarrow{V^-} \cdot \overrightarrow{I^-}\right)}_{P^-}}^{P^\pm} + \underbrace{\left(\overrightarrow{V^+} \cdot \overrightarrow{I^-}\right) + \left(\overrightarrow{V^-} \cdot \overrightarrow{I^+}\right)}_{P^\sim} \tag{4.2}$$

Where $P^\sim$ is the cross-sequence active power. $P^\pm$ is the in-sequence active power, which is the summation of the positive sequence active power, P^+, and the negative sequence active power, P^-. Using (3.45) to calculate the real power using the dq-frame

$$P^+ = \frac{3}{2}\begin{bmatrix} V_d^+ & V_q^+ \end{bmatrix}\begin{bmatrix} I_d^+ \\ I_q^+ \end{bmatrix} = \frac{3}{2}\left[\left(V_d^+ I_d^+\right) + \left(V_q^- I_q^-\right)\right] \tag{4.3}$$

$$P^{-} = \frac{3}{2}\begin{bmatrix} V_d^{-} & V_q^{-} \end{bmatrix}\begin{bmatrix} I_d^{-} \\ I_q^{-} \end{bmatrix} = \frac{3}{2}\left[\left(V_d^{-} I_d^{-}\right) + \left(V_q^{-} I_q^{-}\right)\right] \tag{4.4}$$

$$P^{\sim} = \frac{3}{2}\left[\left(\begin{bmatrix} V_d^{+} & V_q^{+} \end{bmatrix}\begin{bmatrix} I_d^{-} \\ I_q^{-} \end{bmatrix}\right) + \left(\begin{bmatrix} V_d^{-} & V_q^{-} \end{bmatrix}\begin{bmatrix} I_d^{+} \\ I_q^{+} \end{bmatrix}\right)\right],$$

$$= \frac{3}{2}\left[\left(V_d^{+} I_d^{-}\right) + \left(V_q^{+} I_q^{-}\right) + \left(V_d^{-} I_d^{+}\right) + \left(V_q^{-} I_q^{+}\right)\right] \tag{4.5}$$

Similar steps can be taken to for the reactive power. Using (3.57), (3.70), and (3.77)

$$Q = \left(\overrightarrow{V^{+}} + \overrightarrow{V^{-}}\right) \cdot \left(\overrightarrow{I^{+}}_{\perp} + \overrightarrow{I^{-}}_{\perp}\right) \tag{4.6}$$

$$Q = \overbrace{\underbrace{\left(\overrightarrow{V^{+}} \cdot \overrightarrow{I^{+}}_{\perp}\right)}_{Q^{+}} + \underbrace{\left(\overrightarrow{V^{-}} \cdot \overrightarrow{I^{-}}_{\perp}\right)}_{Q^{-}}}^{Q^{\pm}} + \underbrace{\left(\overrightarrow{V^{+}} \cdot \overrightarrow{I^{-}}_{\perp}\right) + \left(\overrightarrow{V^{-}} \cdot \overrightarrow{I^{+}}_{\perp}\right)}_{Q^{\sim}} \tag{4.7}$$

Where $Q^{\sim}$ is the cross-sequence real power. $Q^{\pm}$ is the in-sequence real power, which is the summation of the positive sequence real power, Q^{+}, and the negative sequence real power, Q^{-}. Using (3.45) to calculate the reactive power using the *dq*-frame

$$Q^{+} = \frac{3}{2}\begin{bmatrix} V_d^{+} & V_q^{+} \end{bmatrix}\begin{bmatrix} -I_q^{+} \\ I_d^{+} \end{bmatrix} = \frac{3}{2}\left[\left(-V_d^{+} I_q^{+}\right) + \left(V_q^{+} I_d^{+}\right)\right] \tag{4.8}$$

$$Q^{-} = \frac{3}{2}\begin{bmatrix} V_d^{-} & V_q^{-} \end{bmatrix}\begin{bmatrix} -I_q^{-} \\ I_d^{-} \end{bmatrix} = \frac{3}{2}\left[\left(-V_d^{-} I_q^{-}\right) + \left(V_q^{-} I_d^{-}\right)\right] \tag{4.9}$$

$$Q^{\sim} = \frac{3}{2}\left[\left(\begin{bmatrix} V_d^{+} & V_q^{+} \end{bmatrix}\begin{bmatrix} -I_q^{-} \\ I_d^{+} \end{bmatrix}\right) + \left(\begin{bmatrix} V_d^{-} & V_q^{-} \end{bmatrix}\begin{bmatrix} -I_q^{+} \\ I_d^{+} \end{bmatrix}\right)\right]$$

$$= \frac{3}{2}\left[\left(-V_d^{+} I_q^{-}\right) + \left(V_q^{+} I_d^{-}\right) + \left(-V_d^{-} I_q^{+}\right) + \left(V_q^{-} I_d^{+}\right)\right] \tag{4.10}$$

Ideally, the grid should maintain zero negative sequence voltage. In practice, V_{dq}^{-} is maintained very close to zero. In fact, according to ANSI C84.1 the maximum voltage

deviation from the average line voltage should not exceed 3% [104]. The IEEE [105] defines the voltage unbalance factor (VUF) as

$$\text{VUF}\% = \frac{\widehat{V^-}}{\widehat{V^+}} \times 100\% \tag{4.11}$$

where $\widehat{V^+}$ and $\widehat{V^-}$ are the voltage amplitudes of the positive and negative sequences, in that order.

In practical cases, and where the controller is doing its job appropriately, the negative sequence voltage is negligibly small compared to the nominal voltage. Therefore, any term where $\overrightarrow{V^-}$ is multiplied by a current can be neglected and approximated to zero. Using that approximation, the negative sequence powers, P^- and Q^-, become zero. Therefore, the in-sequence powers, $P^{\pm}$ and $Q^{\pm}$, are reduced to only P^+ and Q^+, respectively. The off-sequence powers are reduced to

$$P^{\sim} = \frac{3}{2}\left[\left(V_d^+ I_d^-\right) + \left(V_q^+ I_q^-\right)\right] \tag{4.12}$$

$$Q^{\sim} = \frac{3}{2}\left[\left(-V_d^+ I_q^-\right) + \left(V_q^+ I_d^-\right)\right] \tag{4.13}$$

Since it has been established that the positive and negative sequences are independent from each other, the existence of cross-sequence powers seems to contradict that fact. That is because they are not actual physical powers, but rather a metric of the discrepancy between the powers on each phase.

This concept is very similar to how reactive power does not consume actual physical power, but rather it affects the power quality of the grid, while still using up the power capacity of the devices providing it to the grid. In other words, it is possible for a power

device to provide cross-sequence *active power*, $P^{\sim}$, to the grid without consuming active power from outside the grid.

For example, an IC could sink real power from phase a, while sourcing equivalent power to the other two phases. That way

$$P_a = P_b + P_c \tag{4.14}$$

$$\therefore P_a + P_b + P_c = 0 \tag{4.15}$$

This results in $P^{\sim}$ that is greater than zero, while P remains at zero. This will, be proven in simulation in section 5.4. The same concept applies to cross-sequence reactive power.

For power devices like ICs and DG the amount of power they can deliver is called "rating". These ratings are specified in units of watts (W) for real power, and Volt-Amps (VA) for apparent power, S. The prime goal of this work is to maximize the loadability of the DGs in the HMG. To achieve that, it is important to understand how the cross-sequence powers translates to apparent power. Under balanced conditions, apparent power is defined as

$$S = \sqrt{P^2 + Q^2} \tag{4.16}$$

Analogous to that definition, the cross-sequence apparent power, $S^{\sim}$ can be defined as

$$S^{\sim} = \sqrt{P^{\sim 2} + Q^{\sim 2}} \tag{4.17}$$

To calculate $S^{\sim}$ using the dq-frame, equations (4.12) and (4.13) are plugged into (4.17)

$$S^{\sim} = \sqrt{\left(\frac{3}{2}\left[\left(V_d^+ I_d^-\right) + \left(V_q^+ I_q^-\right)\right]\right)^2 + \left(\frac{3}{2}\left[\left(-V_d^+ I_q^-\right) + \left(V_q^+ I_d^-\right)\right]\right)^2} \tag{4.18}$$

$$S^{\sim} = \frac{3}{2}\sqrt{\left(\left[\left(V_d^+ I_d^-\right) + \left(V_q^+ I_q^-\right)\right]\right)^2 + \left(\left[\left(-V_d^+ I_q^-\right) + \left(V_q^+ I_d^-\right)\right]\right)^2} \tag{4.19}$$

$$S^{\sim} = \frac{3}{2}\sqrt{V_d^{+2}I_d^{-2} + V_q^{+2}I_q^{-2} + 2V_d^{+}I_d^{-}V_q^{+}I_q^{-} + V_d^{+2}I_q^{-2} + V_q^{+2}I_d^{-2} - 2V_d^{+}I_q^{-}V_q^{+}I_d^{-}} \quad (4.20)$$

$$S^{\sim} = \frac{3}{2}\sqrt{V_d^{+2}I_d^{-2} + V_d^{+2}I_q^{-2} + V_q^{+2}I_q^{-2} + V_q^{+2}I_d^{-2}} \quad (4.21)$$

$$S^{\sim} = \frac{3}{2}\sqrt{V_d^{+2}\left(I_d^{-2} + I_q^{-2}\right) + V_q^{+2}\left(I_q^{-2} + I_d^{-2}\right)} \quad (4.22)$$

$$S^{\sim} = \frac{3}{2}\sqrt{\left(V_d^{+2} + V_q^{+2}\right)\left(I_d^{-2} + I_q^{-2}\right)} \quad (4.23)$$

$$S^{\sim} = \frac{3}{2}\sqrt{\left(V_d^{+2} + V_q^{+2}\right)}\sqrt{\left(I_d^{-2} + I_q^{-2}\right)} \quad (4.24)$$

Using the amplitude to *dq*-frame equation (3.39), (4.24) becomes

$$S^{\sim} = \frac{3}{2}\,\widehat{V^{+}}\,\widehat{I^{-}} \quad (4.25)$$

where $\widehat{I^{-}}$ is the current amplitude of the negative sequence current. It should be noted that according to the standard IEEE 1549 [106], unbalanced power, S_U, is defined as

$$S_U = \frac{3}{2}\sqrt{V_d^{+^2} + V_q^{+^2}}\sqrt{I_d^{-^2} + I_q^{-^2}} \quad (4.26)$$

Which is equivalent to what was deduced as $S^{\sim}$. Therefore, to stay consistent with the industry standards, the term unbalanced power, S_U, will be used in leu of the term cross-sequence apparent power, $S^{\sim}$.

Therefore, to control S_U, either the positive sequence voltage, V_{dq}^{+}, or the negative sequence current, I_{dq}^{-}, must be used as a control variable. However, in this case, V_{dq}^{+}, is not an option as it is primarily used to for positive sequence voltage and power regulation, which are far more important to the function of the grid than the regulation of negative

sequence current or unbalanced power. Therefore, I_{dq}^{-} should be chosen as the control variable. This should be done in a way so as not to increase V^{-}, or minimize that effect.

4.2 Roles and Modes in the Negative Sequence

Since the DGs' prime objective is active power generation, loading them with unbalanced power, or even reactive power, could limit their real power generation capabilities. In other words, to maximize the loadability of the system, the unbalanced power supplied by the DGs should be as close to zero as possible. As can be deduced in (4.26), to reduce S_U to zero, the term $\sqrt{I_d^{-2} + I_q^{-2}}$ should be reduced to zero. The only possible way to achieve that is to have the negative sequence current reduced to zero. The important question at this point is how to achieve that.

One way to control I_{dq}^{-} is to manipulate the negative sequence impedance going into the DG or IC. This can be done by having the controller emulate a virtual impedance, Z_{vir}, in series with the natural impedance of the DG or IC, as shown in Figure 4.1.

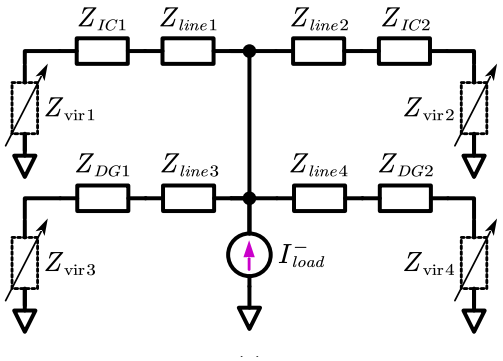

Figure 4.1: Negative sequence component of a grid using virtual impedances

This technique is used in the literature so that all DGs share the unbalanced power equally [94]. However, the goal here is to eliminate the negative sequence current through a DG,

I_{DG}^{-}. If Z_{vir} of the DGs is set to infinity, then (3.78) indicates that I_{DG}^{-} becomes zero. When that occurs, then S_U of the DGs also becomes zero, according to (4.25). This way, the DGs will appear as an open circuit in the negative sequence grid, as shown in Figure 4.2. This mode of operation will be referred to as the negative sequence open circuit (NSO) mode.

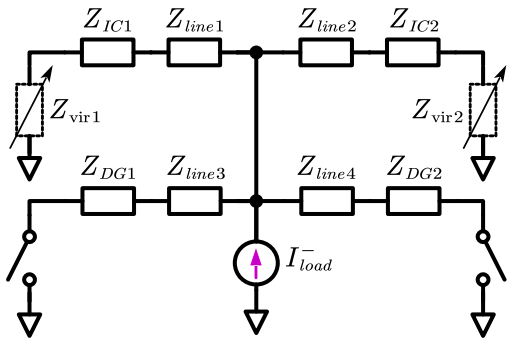

Figure 4.2: Negative sequence component of a grid with DGs in NSO mode

Consequently, all of I_{load}^{-} will be split by the ICs inversely proportional to their impedances as per (3.78). This means the entire unbalanced burden of the DGs is offloaded onto the ICs. Consequently, this frees up apparent power capacity for the DGs where it could be used for generating real power, thus increasing their loadability. This alone achieves most of the main objective of this work.

However, there is still some room for improvement. It can be seen that setting Z_{vir} of the DGs to infinity might raise another issue. First, this will increase V^{-} in the grid. This because the resistance of the path of I_{load}^{-} to the ground becomes larger. This can be proven using the simplified MG in Figure 4.1. Analyzing the layout of impedances yields

$$Z_{path}^{IC,x} = Z_{line}^{x} + Z_{IC}^{x} + Z_{vir}^{x} \tag{4.27}$$

$$Z_{path}^{DG,x} = Z_{line}^{x} + Z_{DG}^{x} + Z_{vir}^{x} \tag{4.28}$$

Where $Z_{path}^{IC,x}$ and $Z_{path}^{DG,x}$ are the total path impedance of I_{load}^{-} through a specific IC or DG, respectively. The path impedances of the DGs are in parallel, so their equivalent impedance, $Z_{\text{path}}^{\text{DGS}}$, can be determined. And similarly for the ICs, $Z_{\text{path}}^{\text{ICS}}$

$$Z_{\text{path}}^{\text{DGS}} = Z_{\text{path}}^{\text{DG1}} \parallel Z_{\text{path}}^{\text{DG2}} \tag{4.29}$$

$$Z_{\text{path}}^{\text{ICS}} = Z_{\text{path}}^{\text{IC1}} \parallel Z_{\text{path}}^{\text{IC1}} \tag{4.30}$$

The equivalent path impedance between I_{load}^{-} and ground before the proposed solution can be calculated by

$$Z_{ground}^{path1} = Z_{path}^{IC,1} \parallel Z_{path}^{IC,2} \parallel Z_{path}^{DG,1} \parallel Z_{path}^{DG,x} \tag{4.31}$$

$$Z_{ground}^{path1} = Z_{\text{path}}^{\text{ICS}} \parallel Z_{\text{path}}^{\text{DGS}} \tag{4.32}$$

$$Z_{ground}^{path1} = \frac{Z_{\text{path}}^{\text{ICS}} Z_{\text{path}}^{\text{DGS}}}{Z_{\text{path}}^{\text{ICS}} + Z_{\text{path}}^{\text{DGS}}} \tag{4.33}$$

In the NSO mode, the DGs act as an open circuit in the negative sequence component of the simplified MG, as seen in Figure 4.2. Therefore, the equivalent path impedance between I_{load}^{-} and ground *after* the proposed solution can be calculated by

$$Z_{ground}^{path2} = Z_{\text{path}}^{\text{IC1}} \parallel Z_{\text{path}}^{\text{IC1}} = Z_{\text{path}}^{\text{ICS}} \tag{4.34}$$

To prove that Z_{ground}^{path2} is larger than Z_{ground}^{path1}, equation (4.34) is divided over (4.33)

$$\frac{Z_{ground}^{path2}}{Z_{ground}^{path1}} = \frac{Z_{\text{path}}^{\text{ICS}}}{\frac{Z_{\text{path}}^{\text{ICS}} Z_{\text{path}}^{\text{DGS}}}{Z_{\text{path}}^{\text{ICS}} + Z_{\text{path}}^{\text{DGS}}}} \tag{4.35}$$

$$\frac{Z_{ground}^{path2}}{Z_{ground}^{path1}} = \frac{\mathrm{Z}_{\mathrm{path}}^{\mathrm{ICS}} + \mathrm{Z}_{\mathrm{path}}^{\mathrm{DGS}}}{\mathrm{Z}_{\mathrm{path}}^{\mathrm{DGS}}} = \frac{\mathrm{Z}_{\mathrm{path}}^{\mathrm{ICS}}}{\mathrm{Z}_{\mathrm{path}}^{\mathrm{DGS}}} + 1 \tag{4.36}$$

$$\because \mathrm{Z}_{\mathrm{path}}^{\mathrm{ICS}} > 0, \qquad \mathrm{Z}_{\mathrm{path}}^{\mathrm{DGS}} > 0 \tag{4.37}$$

$$\therefore \frac{Z_{ground}^{path2}}{Z_{ground}^{path1}} > 1 \tag{4.38}$$

$$\therefore Z_{ground}^{path2} > Z_{ground}^{path1} \blacksquare \tag{4.39}$$

In return, to minimize V^-, the ICs should offer the least resistance they can. Therefore, they must act as a short circuit. The negative sequence impedance can be calculated as

$$Z^- = \frac{V^-}{I^-} \tag{4.40}$$

A short circuit is when Z^- is equal to zero. Thus, the way ICs can emulate a short circuit, that is by forcing their negative sequence voltage, V^-, to zero. As seen in subsection 3.3.1, the voltage and current measurements are taken after the filtering inductor. This means that when the IC forces V^- to zero, that encompasses the filtering inductor where most the natural impedance of the IC comes from.

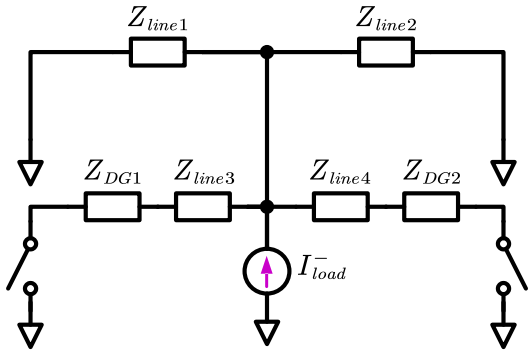

Figure 4.3: Negative sequence component of a grid with DGs in NSO mode and ICs in NSF mode

This, in practice, means that Z_{IC}^{-} becomes zero. This will be referred to as the negative sequence forced (NFS) mode. Then, the negative sequence component of the grid becomes as seen in Figure 4.3. This combination of NSO mode for DGs and NSF for ICs will be referred to as the direct negative sequence control method.

The second issue that might arise is if there is a high discrepancy between the ICs' impedances. Then, one of them might get overburdened with unbalanced power, while the other one under-contributes. If the unbalanced power and line impedance discrepancies are large enough, the overburdened IC might trip an overload protection breaker significantly before the other IC reaches its rated limit. This, in practice. reduces the effective capacity of the IC, which is undesirable. This calls for coordination method between the ICs to ensure they share the unbalanced power proportionally.

One way to force the unbalanced power to be shared between the ICs is to make Z_{vir} an order of magnitude larger than the line impedance [94].

$$\because Z_{vir}^{x} \gg Z_{line}^{x} \Rightarrow \therefore Z_{path}^{IC,x} \approx Z_{IC}^{x} + Z_{vir}^{x} \tag{4.41}$$

This way, the discrepancy due to the line impedances are negligible. $Z_{path}^{IC,x}$ becomes approximately equal for all ICs. However, the drawback to this method is that it artificially increases the path impedance for I_{load}^{-}. Consequently, this causes V^{-} to increase as well. The tradeoff is that the more Z_{vir}^{x} is increased, the lower the impact of Z_{line}^{x}, but the higher V^{-} is observed in the grid, and vice versa.

4.3 Small Signal Coordination Method

An alternative method to coordinate the unbalanced power between the ICs is proposed. This method will be referred to as the small signal coordination method (SSCM). A small three-phase sinusoidal signal can be imposed on the AC grid [96]. This small signal is chosen to have a nominal frequency, ω_{nom}^{ss}, that is different from the fundamental frequency of the MG, ω_{nom}, and its related harmonics. For example, 2.5 or 3.5 that of the nominal grid frequency. The amplitude is chosen to be small enough to not interfere, or cause issues, with loads, equipment, or other DGs. A reasonable choice of the amplitude is 0.5% of the nominal voltage of the AC grid, V_{base} [89].

As such, the small signal can be represented as its own independent sequence in the grid, as shown in Figure 4.4. This sequence shall be dubbed the small signal sequence (SSS), or the ω_{ss}-sequence. Here, the ICs are in the voltage-mode control, and are "grid" forming, as far as the small signal is concerned. The controllers of the DGs do not "see" the small signal, and as such, they appear as short circuit with their natural impedance. This is analogous to the NSN mode, but for the small signal sequence component.

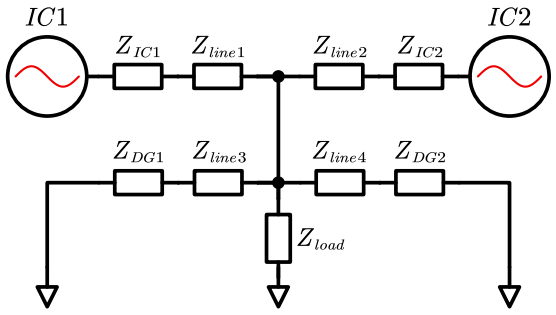

Figure 4.4: Small signal sequence component of a grid

This technique and its variations are often used in AC or DC microgrids [90]. However, to the knowledge of the author, it has never been used to coordinate the unbalanced power

between ICs. Furthermore, the proposed method is coupled with the fact that the DGs are controlled to produce no unbalanced power. In other words, in combination with the DGs operating in NSO mode.

To establish this superimposed sequence, the frequency, phase, and voltage amplitude need to be defined. The voltage, $\widehat{V^{ss}}$, is predefined as constant equal to 0.5% of base voltage amplitude of the fundamental frequency, $\widehat{V_{base}}$. Since the controllers are all designed in the in the dq-frame, then the small signal voltage reference in the dq-frame is defined as

$$V_{dq}^{ss} = \begin{bmatrix} V_d^{ss} \\ V_q^{ss} \end{bmatrix} = \frac{\widehat{V_{base}}}{0.5 \times 10^{-2}} \begin{bmatrix} 1 \\ 0 \end{bmatrix} = \widehat{V^{ss}} \begin{bmatrix} 1 \\ 0 \end{bmatrix} \tag{4.42}$$

As for the frequency, ω^{ss}, and phase, θ^{ss}, a droop controller is used to define and coordinate these variables. This is similar to what was done in section 3.2. The S_U-ω^{ss} droop relating the unbalanced power, S_U, with ω^{ss} is defined as

$$\omega_{ss}^{*} = \omega_{max}^{ss} - k \cdot S_U \tag{4.43}$$

where ω_{ss}^{*} and ω_{max}^{ss} are the reference and predefined maximum frequency of the small signal, respectively. And k is the droop coefficient. The value of k is calculated as

$$k = \frac{\omega_{max}^{ss} - \omega_{min}^{ss}}{S_U^{rated,IC}} \tag{4.44}$$

where ω_{min}^{ss} is the predefined minimum frequency of the small signal. And $S_U^{rated,IC}$ is a predefined value of how much unbalanced power an IC can provide. This can be equivalent to the Q limit of the IC, or it can be calculated like the Q limit of a DG. It is also possible to make it dynamic, if needed. For this thesis, it is a predefined value that was determined using trial and error of simulations.

The S_U-ω^{ss} droop changes θ^{ss} with time. This affects active power of the small signal, P^{ss}. This is analogous to what have been explained using (3.59). P^{ss} is calculated as

$$P^{ss} = \frac{3}{2}\begin{bmatrix} V_d^{ss} & V_q^{ss} \end{bmatrix}\begin{bmatrix} I_d^{ss} \\ I_q^{ss} \end{bmatrix} \tag{4.45}$$

$$P^{ss} = \frac{3}{2}\left[\left(V_d^{ss} I_d^{ss}\right) + \left(V_q^{ss} I_q^{ss}\right)\right] \tag{4.46}$$

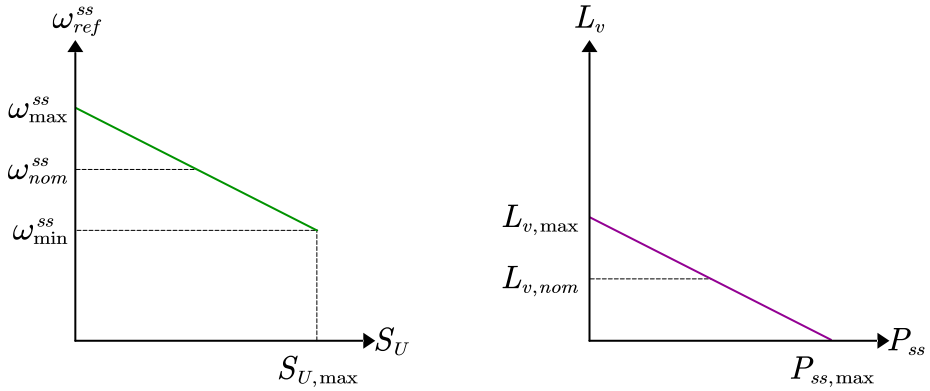

Figure 4.5: Typical droop slopes for the small signal coordination method

A second droop can then be used to relate P^{ss} with the negative sequence virtual inductance, L_v^-. This is known as the P^{ss}-L_v^- droop. The droop slope is defined as

$$L_v^- = L_{v0}^- - l.P^{ss} \tag{4.47}$$

where L_{v0} is the slope bias, and l is the droop coefficient. The value of l is calculated as

$$l = \frac{L_{v,max}^- - L_{v,min}^-}{P_{IC,rated}^{ss}} \tag{4.48}$$

where $L_{v,min}^-$ and $L_{v,max}^-$ are predefined minimum and maximum virtual negative sequence inductances, in that order. The rated small signal active power, $P_{IC,rated}^{ss}$ can be chosen based on trial and error using simulations. It is recommended that it be defined an order of

magnitude larger than the active power losses of the small signal in transmission lines. The droops mentioned in this section are visualized in Figure 4.5.

While this coordination method might not be essential to maximize loadability, it offers an extra layer of optimization for the utilization of ICs. This is especially in comparison to [94], where the unbalanced power sharing uses a single droop that is susceptible to the variation in transmissions lines between the ICs.

4.4 Proposed Modified Droop

It can be seen from Figure 4.5 that the typical L_v^- is always greater than or equal to zero. This can add to the total negative sequence impedance, which results in increased V^-. This leads to an increase in the voltage imbalance, which is an undesirable consequence. To fix this, it is proposed that L_v^- is made to always be less than or equal to zero. The leads to

$$Z_{path}^{IC,x} = Z_{line}^{x} + Z_{IC} - Z_{vir}^{x} = Z_{line}^{x} + Z_{IC} - (R_v^- + L_v^-) \tag{4.49}$$

where R_v^- is the virtual negative sequence resistance. It is used as a damping factor, and generally is tuned as needed to achieve the desired performance. This subtractive virtual impedance eliminates the disadvantage of the typical method of additive virtual impedance.

The effect of the virtual impedance is emulated by producing a negative sequence voltage. This voltage due to the virtual impedance and the negative sequence current, I^-,can be calculated by

$$\begin{bmatrix} V_{d,ref}^- \\ V_{q,ref}^- \end{bmatrix} = \begin{bmatrix} R_v & -\omega L_v \\ \omega L_v & R_v \end{bmatrix} \begin{bmatrix} I_d^- \\ I_q^- \end{bmatrix} \tag{4.50}$$

where I_d^- and I_q^- are the d and q components of I^-, respectively. By setting the bias value in (4.47) to zero, L_v^- becomes less than or equal to zero, while maintaining the same slope rate, or droop coefficient. The proposed modified droop can be seen in Figure 4.6.

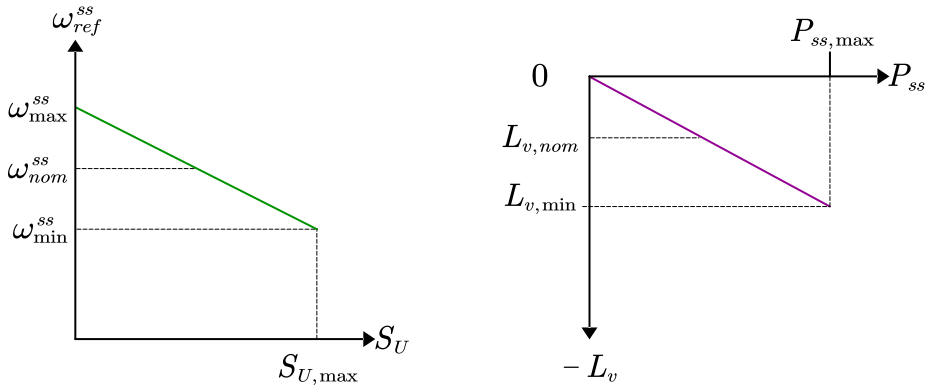

Figure 4.6: The proposed modified droop

4.5 Modified Controllers of the Proposed Method

To implement the proposed method, the controllers described in section 3.3 need to be modified to implement the proposed method. Luckily, since all control is done in the *dq*-frame, the cascaded control section in the controller design of the DG and IC can just be duplicated to accommodate for the negative sequence control and the small signal control.

For the negative sequence control, the DGs only need a current controller. This is because they operate in the NSO mode. To achieve the effect of an open circuit, the DGs should allow no negative sequence through them. That is, $I_{dq,ref}^-$ should be fixed to zero. Then, the output from the positive sequence control and negative sequence control are converted to their respective three-phase signals, V_{abc}^+ and V_{abc}^-, in that order. Then, these three-phase signals are added together and passed to the PWM block. The modified cascaded control

section can be seen in Figure 4.7. It should be noted that this replaces the conventional cascaded control shown in Figure 3.18.

As for the ICs, similar modifications are proposed. Since they need to control V^- to implement L_U^-, the added negative sequence controller contains a voltage loop and a current loop. In addition to that, a controller for the small signal needs to be added, as well.

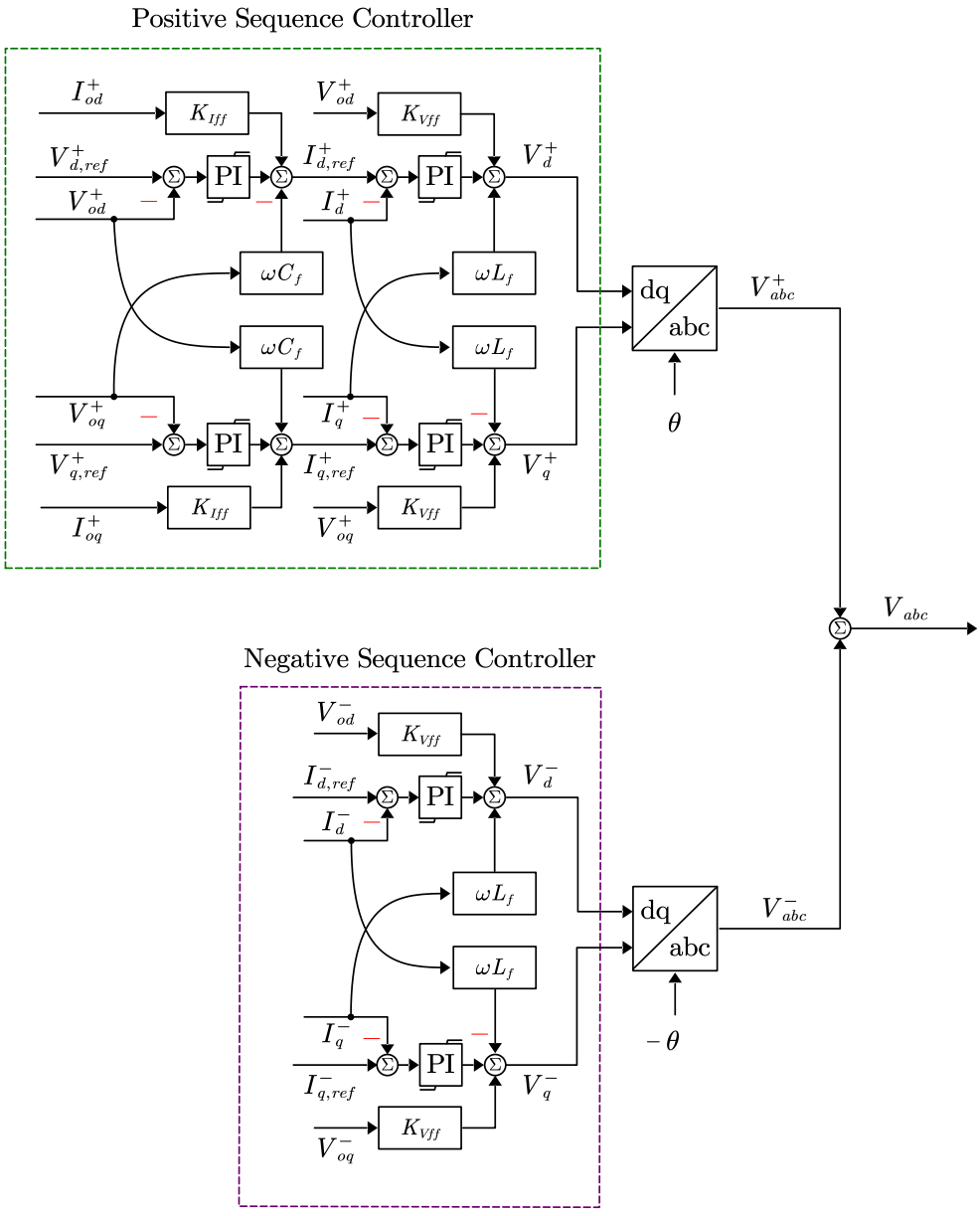

Figure 4.7: The proposed modified cascaded control for the DGs

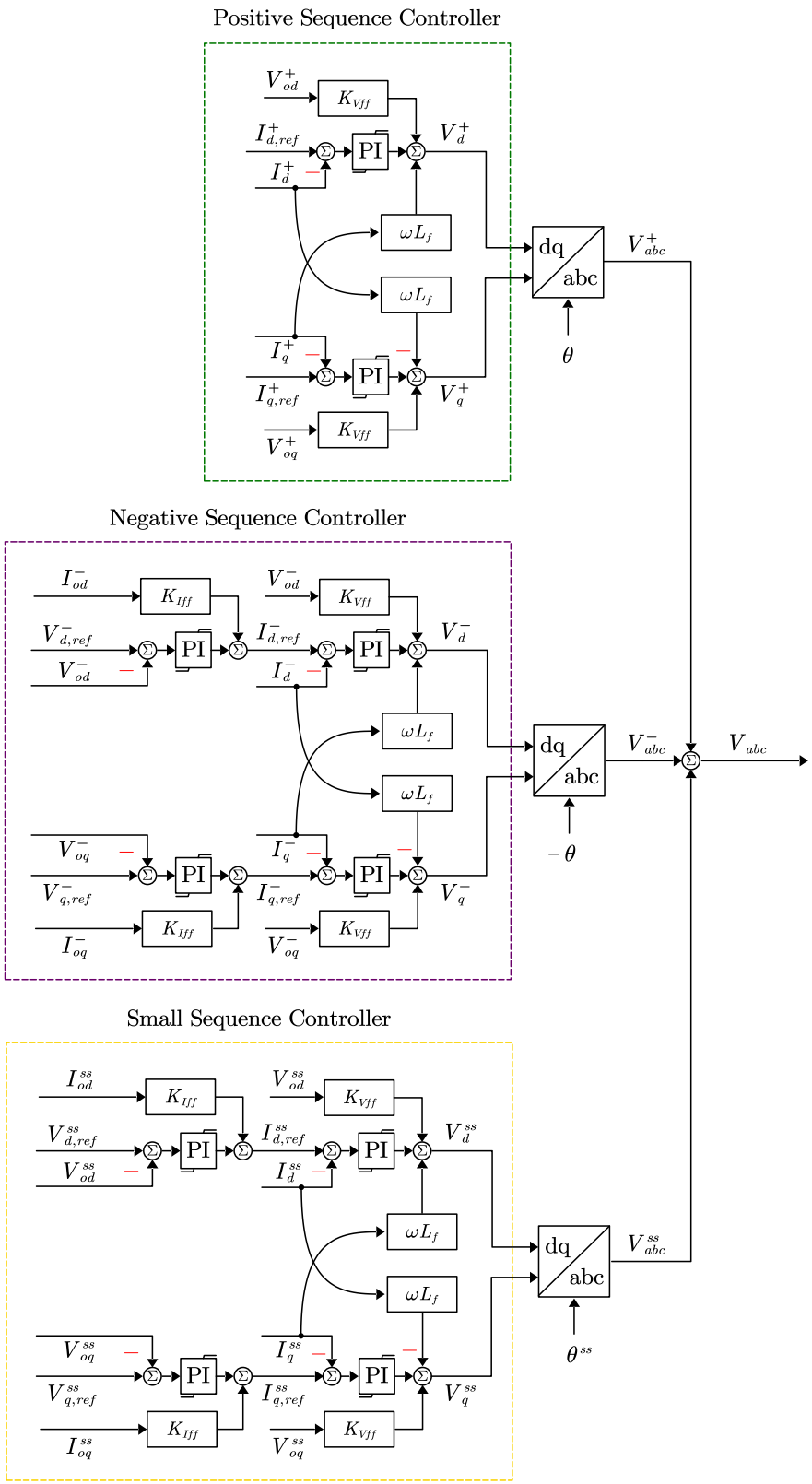

Figure 4.8: The proposed modified cascaded control for the ICs

Again, due to the dq-frame nature of the proposed method, the design of this controller is familiar at this point. In fact, the PI controller for V^{ss} is identical to that for the PI controller for the positive sequence voltage in DGs, save for different tuning parameters. The different tuning is required due to the higher frequency of V^{ss}. That would cause V^{ss} to experience different impedance values for the filters, lines, and loads in the MG. The modified cascaded control section can be seen in Figure 4.8. It should be noted that this replaces the conventional cascaded control shown in Figure 3.15.

4.6 The Triple Notch Filter

Now, the question that remains is how to separate the different sequences from one another. Conventionally [93], a notch filter is used to separate the positive and negative sequences from each other in the dq-frame. This is done as the negative sequence appears as a ripple with twice the fundamental frequency in the dq-frame of the positive sequence, and vice-versa [92]. Thus, a notch filter with the transfer function, $H_{NF}(s)$, can be used, such as

$$H_{NF}(s) = \frac{s^2 + \omega_n^2}{s^2 + 2\zeta\omega_n s + \omega_n^2} \tag{4.51}$$

where ω_n is the natural frequency of the notch filter. In this case, it is equal to twice the fundamental frequency, ω_{nom}. And where ζ is the damping ratio. The value for this variable is usually chosen as $\sqrt{2}$.

However, using the SSCM, there are always three ripples that appear in the dq-frame of every sequence. For example, for the SSS, the ripples are due to the fundamental positive and negative sequences. Since the grid for the SSS mirrors that for the fundamental frequency, it also experiences unbalanced conditions due to the unbalanced load.

Therefore, it results in a negative sequence for the small signal. Thus, the third ripple that appears in the dq-frame of the SSS is due to its own negative sequence component.

Those three ripples need to be removed for the different components to be truly separate and independent. Another way to put it is these ripples need to be filtered out so that each controller can focus on its respective sequence. Otherwise, these ripples may cause interference, or cause the different sequence to affect each other, which is undesirable.

Unfortunately, there doesn't seem to be an explicit way to implement this filtering in the literature. The default way to deal with this is to implement a low-pass filter, which should eliminate all the aforementioned ripples. However, this significantly limits the bandwidth of the controller [92].

A better approach is proposed as part of the control scheme. To selectively filter out these ripples, multiple, cascaded notch filters are used. Since there are three ripples in each dq-frame, three notch filter should be used. This approach will be referred to as the triple notch filter (TNF). However, the frequency of these ripples are variables, and as such ω_n for each of those filters needs to be determined.

Since the dq-frame is a rotating frame synchronized with the phasor of a specific sequence, an extraneous phasor's rotation speed would appear at relative speed from the perspective of the synchronized phasor. For example, assume a phasor of a sequence component rotating at ω_{s1}, and the phasor of a different sequence component rotating at ω_{s2}. In a dq-frame synchronized to ω_{s1}, the frequency of ω_{s2} would appear in a relative term, such that

$$\omega_{s2}^{s1} = \omega_{s1} - \omega_{s2} \tag{4.52}$$

where ω_{s2}^{s1} is the *in-frame* frequency of ω_{s2}. That is, the frequency of ω_{s2} as it appears in a frame synchronized to ω_{s1}.

The negative sequence appears as a phasor that rotates in the opposite direction of the positive sequence. In other words, it can be said it is rotating at negative frequency of the positive sequence. Assuming the positive sequence is ω_{s1}, and the negative sequence is ω_{s2}, (4.52) yields

$$\omega_{s2}^{s1} = \omega_{s1} - \omega_{s2} = \omega_{s1} - (\omega_{s1}) = 2\omega_{s1} \tag{4.53}$$

which agrees with the fact that the negative sequence appears as a ripple with twice the frequency of the positive sequence. Therefore (4.52) can be used to determine the in-frame frequency for any extraneous sequence components. This will help to determine the natural frequencies for the TNF. Figure 4.9 (a) shows the signal block diagram of how the TNF is implemented with the calculated in-frame frequencies. Figure 4.9 (b) shows how the TNF is represented as a single block. The primary frequency is ω_p. That is, the frequency the dq-frame is synchronized to. While ω_s is the secondary frequency. In case ω_p is the fundamental frequency, then ω_s is the frequency of the small signal. In case ω_p is the small signal, then ω_s is equal to the fundamental frequency.

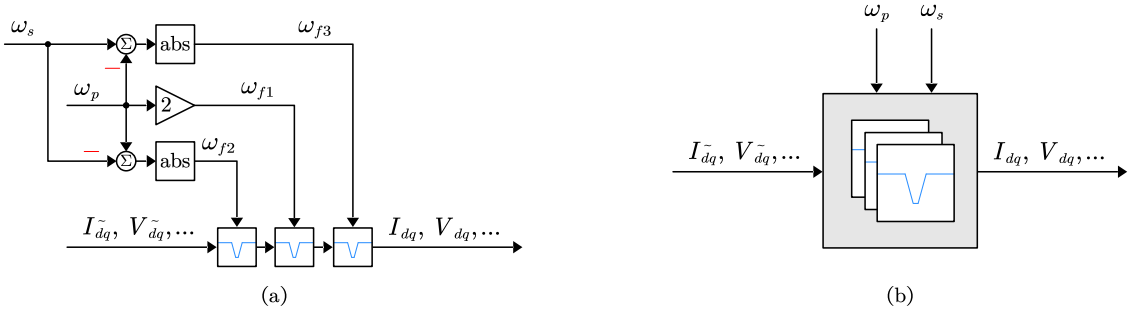

Figure 4.9: Triple notch filter (a) in detail, (b) as a single block

To understand why such lengths are taken instead of going with the default low-pass filter (LPF) approach, it is best to showcase the performance of the two approaches. One of the best ways for such showcase is to compare the step response of the two approaches

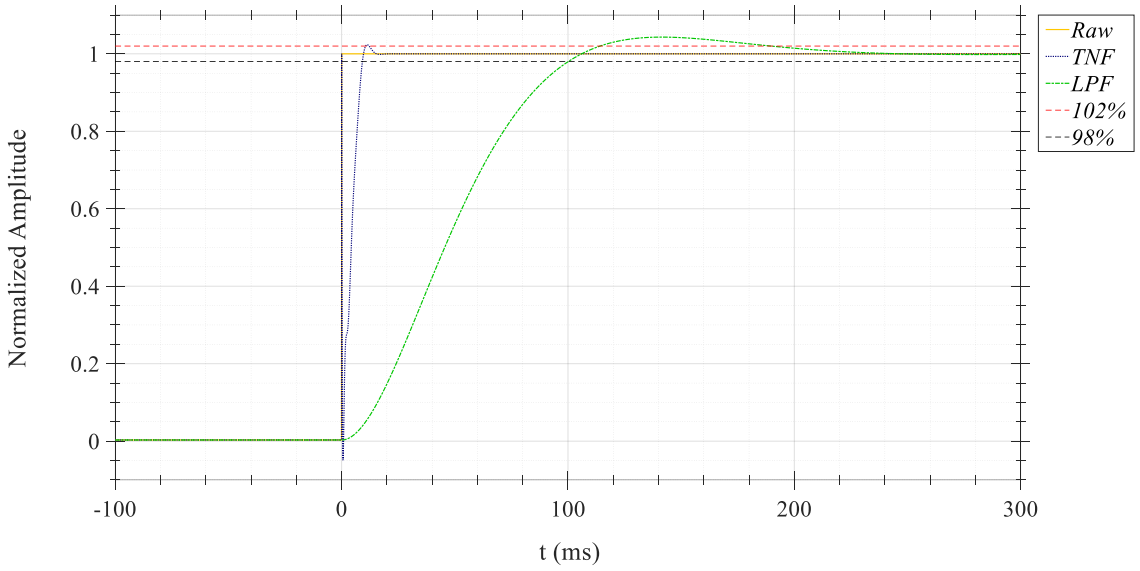

Figure 4.10: Step response of the low-pass filter and the triple notch filter

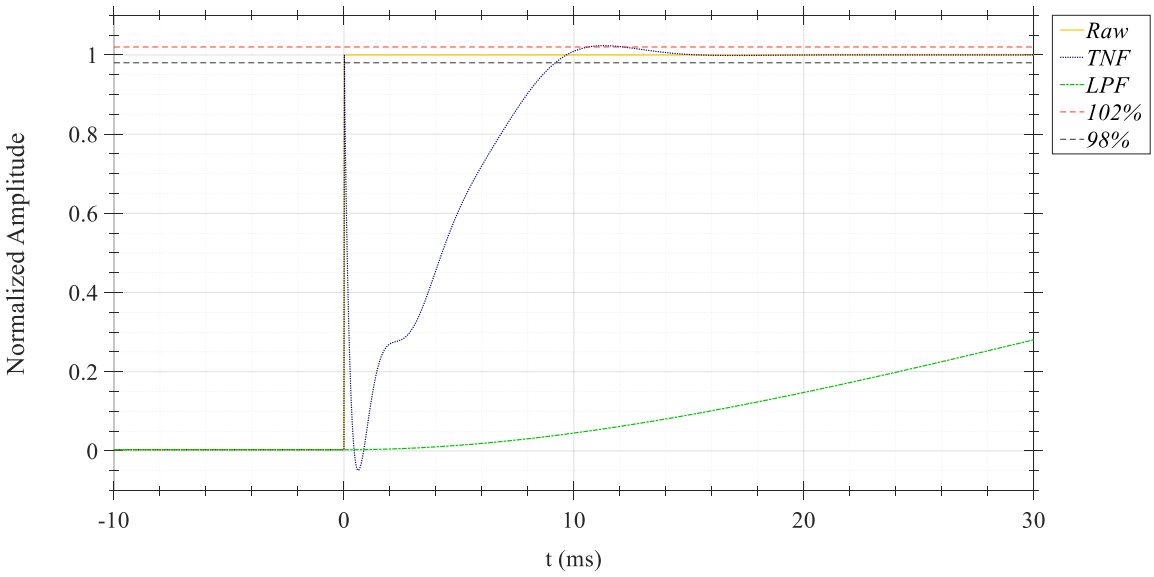

Figure 4.11: A closer look at the step response of the triple notch filter

As can be seen in Figure 4.10, the step response of the LPF is significantly slower than that of the TNF. The settling category is set to ±2%. The settling time for the LPF is 189.78 ms. Meanwhile, the settling time for the TNF is almost order of magnitude quicker. A zoomed in perspective seen in Figure 4.11 shows that the settling time for the TNF is 12.12 ms. That's around 15.66 faster than the LPF.

CHAPTER 5
PROOF OF CONCEPT

In the previous chapters, the control for proposed approach was laid out and explained in detail. To prove the claims made, and to demonstrate the advantage over the existing methods in the literature, a small test system is simulated in MATLAB/Simulink.

The results will demonstrate how large the voltage unbalance can become in case the negative sequence current was not mitigated properly. The results will also prove that the under-zero negative sequence virtual impedance provides superior mitigation of the amplitude of V^- at the load. Furthermore, it will be shown how the IC can provide cross-sequence real power, $P^{\sim}$, and unbalanced power, S_U, without consuming any significant amount of real power from its DC side. Most importantly, the accuracy of the unbalanced power sharing scheme will be showcased, along with its dynamic performance.

5.1 Test System Layout

The system consists of a DG, two ICs, transmission lines and an unbalanced load. The layout of the system is shown in Figure 5.1.

The unbalanced load, Z^u_{load}, is modeled using a three-phase impedance in delta configuration with one side removed. In other words, two phases are loaded, while the third phase is unloaded. While this case is relatively extreme and unlikely in a typical grid, it is more common in MGs. Furthermore, the extreme case is used to demonstrate the robustness of the proposed control scheme.

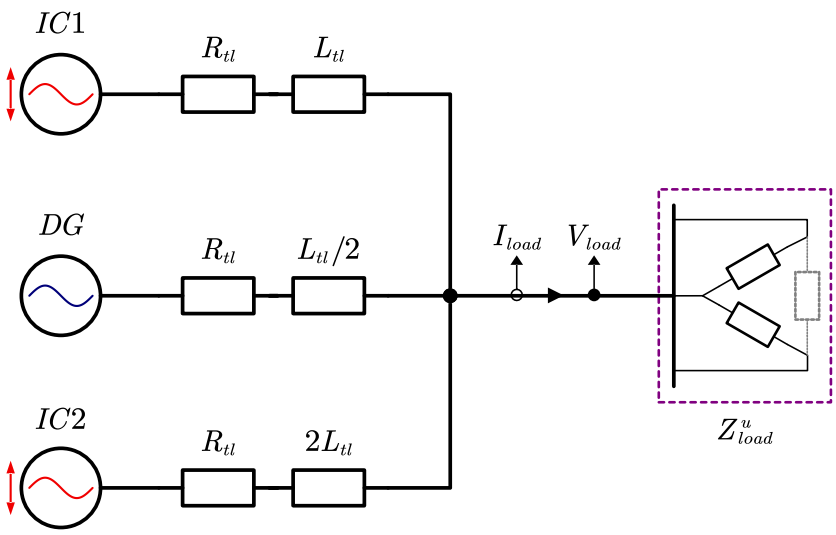

Figure 5.1: Layout of proof-of-concept system

The transmission lines are modeled as series resistor-inductor (RL) impedances. The line impedances between the load and the two ICs are made with a large discrepancy in their values. The line impedance for IC2 has twice the equivalent inductance, L_{tl}, compared to the line impedance for IC1. Meanwhile, the line impedance of the DG has half the equivalent inductance of IC1. This is to demonstrate that although the DG is significantly "closer" to the unbalanced load, the ICs are able to adequately take care of the DG's portion of S_U. It should be noted that the ICs are not connected to a DMG. Their role here is just to provide unbalanced power with no real power transfer. That is, P_{IC} is set to zero.

5.2 Perils of Mismanaged Current

An important part to achieve the goal of the proposed methodology is to have the DG operate in the NSO mode, described in CHAPTER 4. This insures the DGs produce no negative sequence current, and therefore, no unbalanced power. However, this means that if the ICs fail to compensate for I^-, V^- can become dangerously high. The simulation

begins with only the DG connected to the AMG. As proposed, I_{ref}^{-} for the DG is set to zero. Figure 5.2 demonstrate the three-phase voltages at the load bus. It can be seen that there exists a large voltage unbalance.

At t = 1 s, the IC are connected to the AMG and become active. At that point, the negative sequence controllers of ICs are not yet active. That is, the ICs are operating in the NSN mode. Even in that mode, the ICs are able to naturally reduce the voltage unbalance, as explained in theory, previously. Figure 5.3 provides a zoomed-in perspective of the waveforms. The symmetrical components of the load bus voltage are visualized in Figure 5.4. Then, it can be further seen that V^{-} drops close to zero.

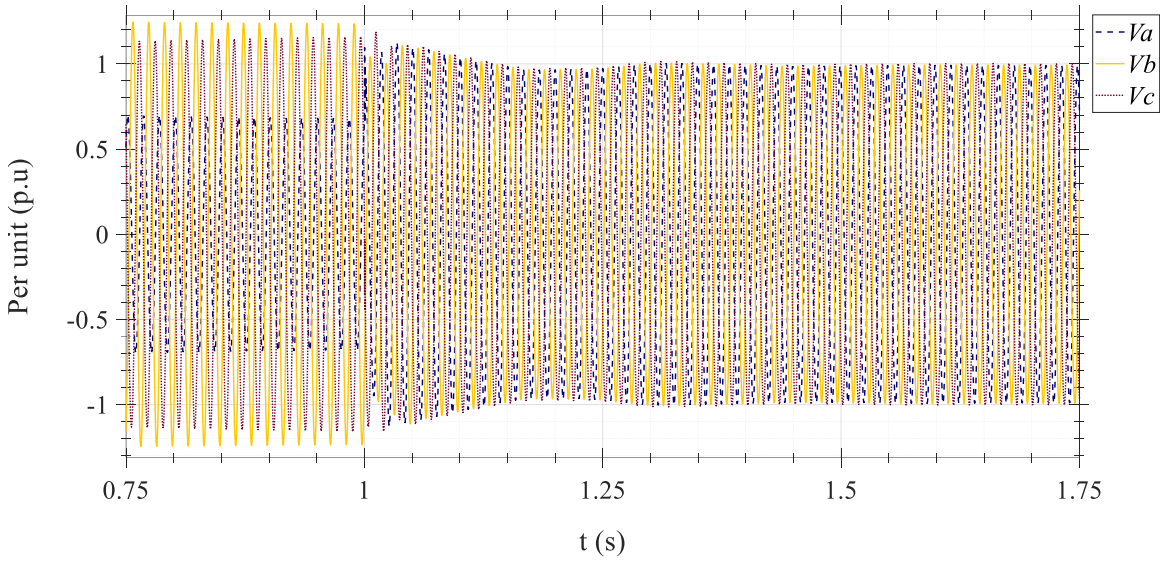

Figure 5.2: V_{abc}^{load} before and after ICs activation

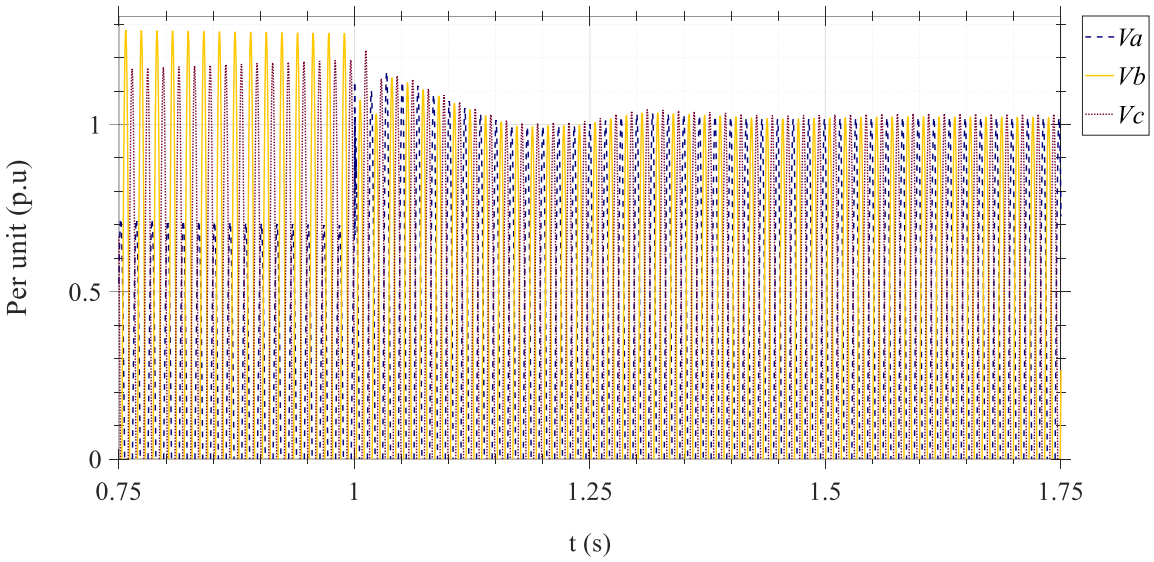

Figure 5.3: V_{abc}^{load} before and after ICs' activation, zoomed in

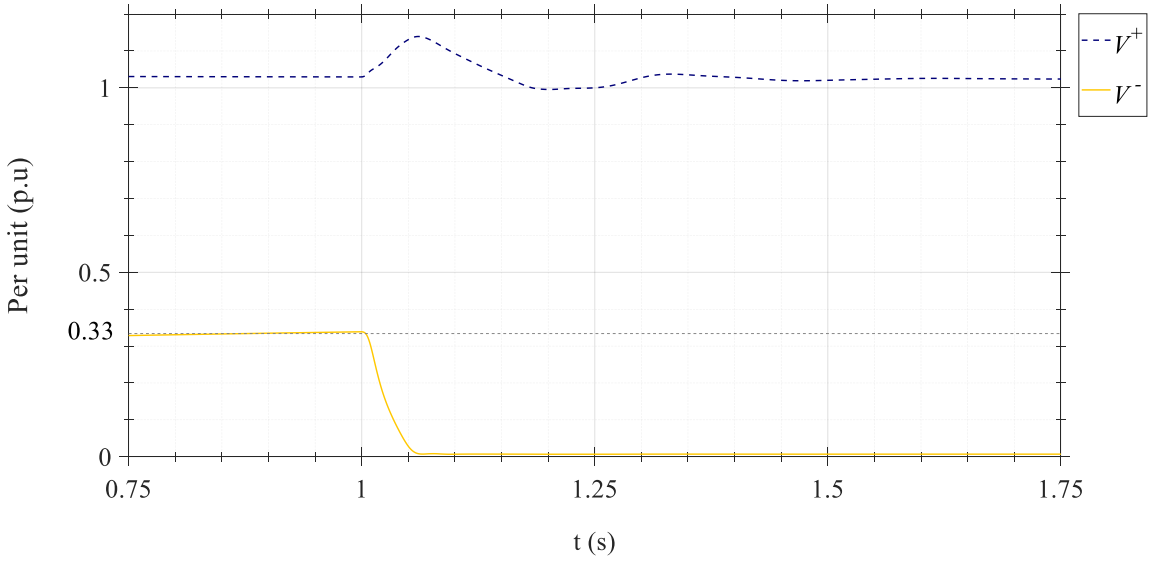

Figure 5.4: Positive and negative sequence of V_{load} before and after ICs' compensation

5.3 Minimal Impact of The Small Signal

The small signal coordination method is activated at t = 2.25 s. Figure 5.5 demonstrates the affect of, or rather the lack of, the SSCM on the load voltage. At a closer look, Figure 5.6 shows how the oscillations of the small signal are superimposed on the fundamental

three-phase waveform. As specified, the amplitude of small signal is about 0.5% of V_{base}. Figure 5.7 gives a closer look on V^+ around the time SSCM is activated. V^+ is largely unperturbed, save for a minute transitory fluctuation around the activation time.

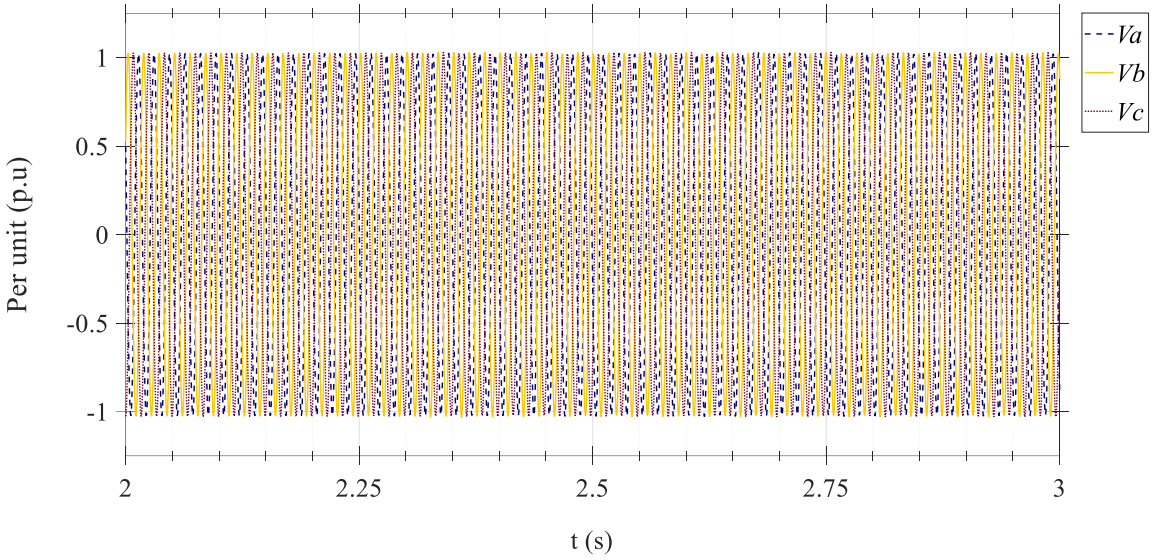

Figure 5.5: V_{abc}^{load} before and after activating SSCM

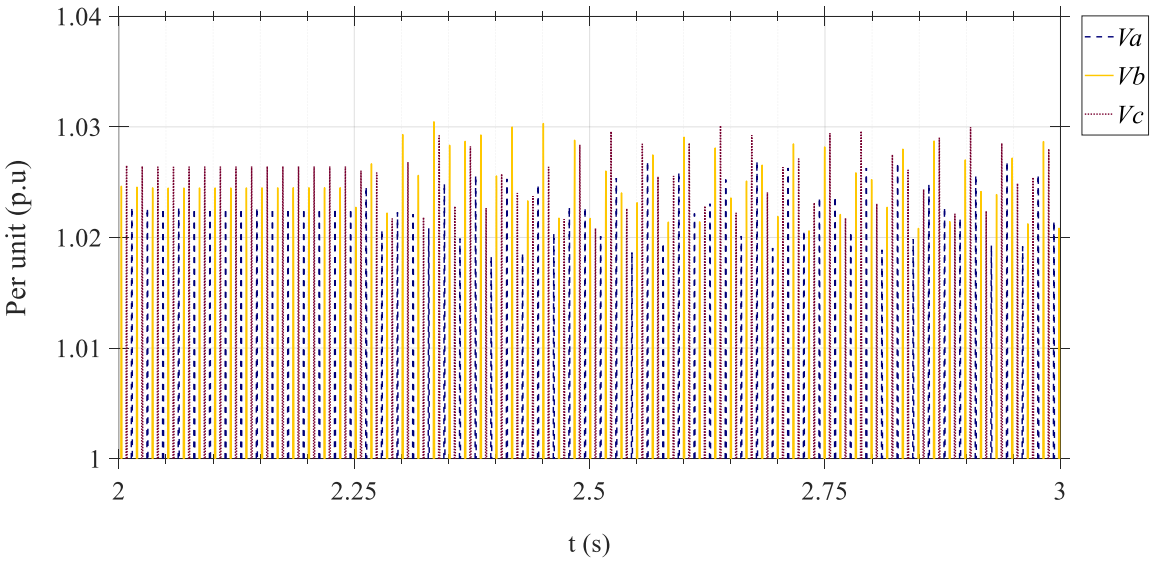

Figure 5.6: V_{abc}^{load} before and after activating SSCM, at a closer look

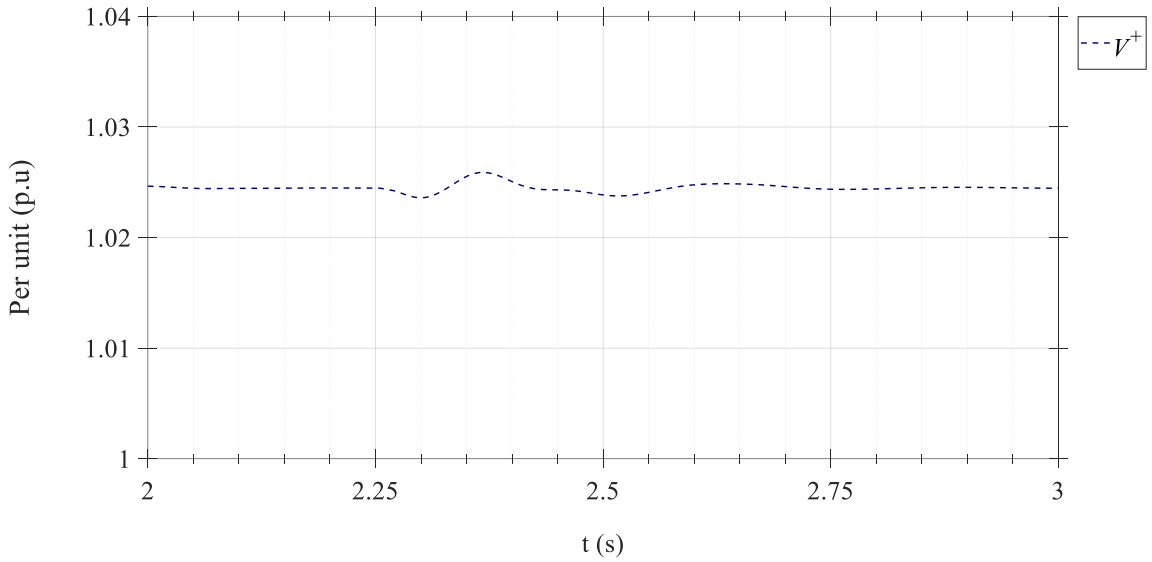

Figure 5.7: V^+_{load} before and after activating SSCM, at a closer look

5.4 Coordinated Accuracy

The purpose of the SSCM is to ensure that the ICs are proportionally burdened with the task of supplementing unbalanced power, as explained in section 4.3. The results of which can be demonstrated in Figure 5.8. The graph spans 3 events, as detailed in Table 5.1.

Table 5.1: Events details for Figure 5.8

E#	Description	Start time (s)
E1	ICs in NSN	<1.5
E2	ICs in NSF	1.75
E3	ICs in SSCM	2.25

As expected, since IC2 has greater line impedance to the unbalanced load than IC1, IC2 contributes less unbalanced power than IC1 during E1. During E1, that difference in contribution is exasperated as the effect of line impedance is more prominent when the ICs eliminate their natural impedance when in NSF mode.

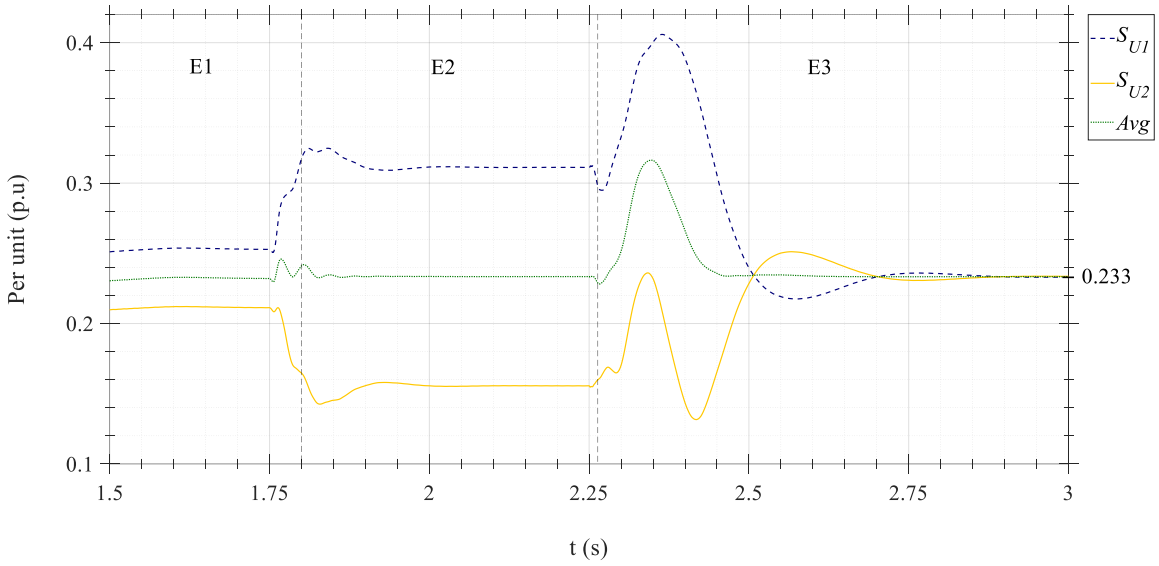

Figure 5.8: Dynamics of the proposed SSCM during events

After the SSCM is activated in E3, S_U fluctuates as the IC are adjusting their negative sequence inductance, L_v^-, in an attempt to converge into a specific value. In less than a second, the two ICs start sharing S_U equally, which should be equal to the average value of S_U between them. In this case, they converge to about 0.233 p.u. The percentage of the sharing error for IC1, $S_{U,err}^{IC1}$, is defined as:

$$S_{U,err}^{IC1} = \left(\frac{S_U^{IC1} - S_U^{IC2}}{\frac{(S_U^{IC1} + S_U^{IC2})}{2}} \right) \times 100 = \left(\frac{S_U^{IC1} - S_U^{IC2}}{S_U^{AVG}} \right) \times 100 \qquad (5.1)$$

where S_U^{AVG} is the average value of unbalanced power of IC1 and IC2. Figure 5.9 shows how the steady state sharing accuracy is worst when the ICs are operating in the NSN mode. When the SSCM is used, the sharing error becomes practically null in less than a second.

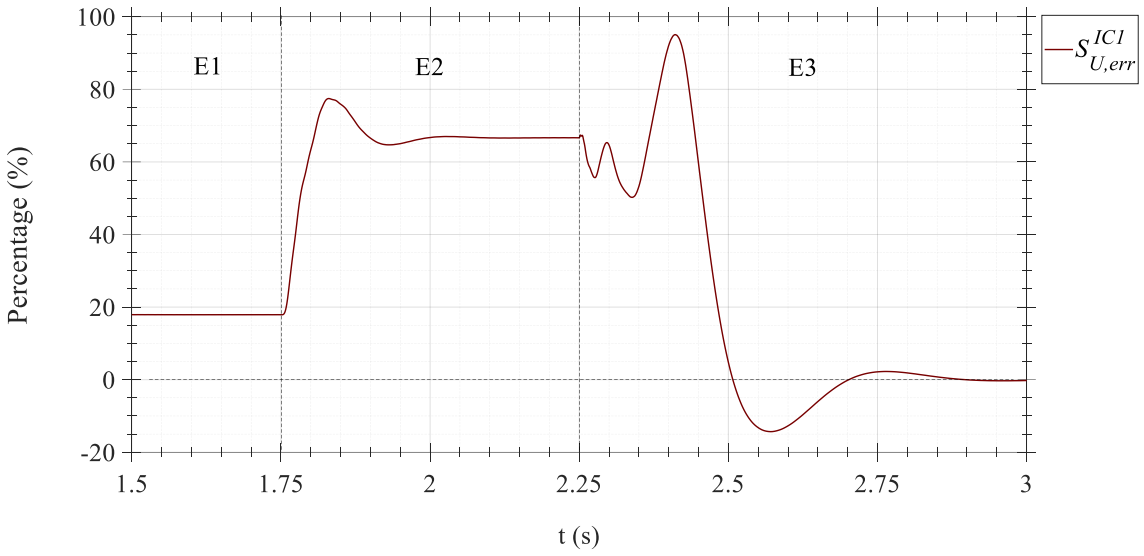

Figure 5.9: S_U sharing error percentage during events

It is interesting to see how the virtual impedances of the ICs are influenced by the coordination method to achieve its goal. Using the negative sequence output voltage of the IC, $V_{o,ICx}^{-}$, and the IC's negative sequence current, I_{ICx}^{-}, it is possible to calculate the virtual negative sequence impedance, Z_{vx}^{-}, such that

$$Z_{vx}^{-} = \frac{V_{o,ICx}^{-}}{I_{ICx}^{-}} \tag{5.2}$$

Using the dq-frame measurements of the voltage and current

$$Z_{vx}^{-} = \frac{V_{od,ICx}^{-} + jV_{oq,ICx}^{-}}{I_{d,ICx}^{-} + jI_{q,ICx}^{-}} \tag{5.3}$$

Since impedance is a complex quantity consisting of resistance and reactance, such that

$$Z_{vx}^{-} = R_{vx}^{-} + jX_{vx}^{-} \tag{5.4}$$

then, the virtual negative sequence reactance can be calculated from the dq-frame measurements as

$$X_{vx}^{-} = Im\{Z_{vx}^{-}\} = Im\left\{\frac{V_{od,ICx}^{-} + jV_{oq,ICx}^{-}}{I_{d,ICx}^{-} + jI_{q,ICx}^{-}}\right\} \tag{5.5}$$

Where $Im\{.\}$ is imaginary part operator. Using the grid's frequency calculated from the PLL, the equivalent virtual negative sequence inductance, L_{vx}^{-}, can be calculated as

$$L_{vx}^{-} = \frac{X_{vx}^{-}}{\omega} \tag{5.6}$$

Figure 5.10 shows the dynamics of the L_{v1}^{-} and L_{v2}^{-} associated with IC1 and IC2, in that order. The difference between their values, ΔL_{v}^{-}, is also plotted. The difference between the actual transmission lines' equivalent inductances, ΔL_{tl}, is added to the plot as a reference line.

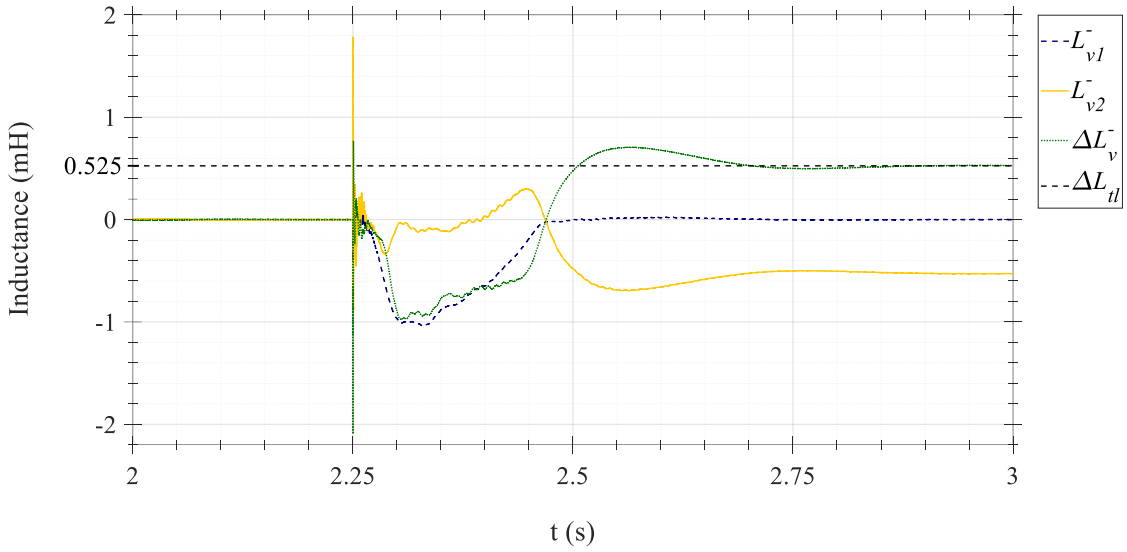

Figure 5.10: Dynamics of the virtual negative sequence inductor

It can be seen how the ICs adjust their respective L_{v}^{-} so that ΔL_{v}^{-} becomes equivalent to ΔL_{tl}. This is a natural consequence and a requirement to achieve the goal of the SSCM. Looking at it the other way around, it can be said that the solution to achieve proportional unbalanced power sharing is to eliminate the impedance difference, as theorized in

CHAPTER 3. This is achieved when ΔL_v^- and ΔL_{tl} become equal, as proved using Figure 5.8 and Figure 5.10.

Another theoretical claim made is how the unbalanced power does not transfer any average real power into the AMG. This point can be proved with Figure 5.11. The period shown is a one second snapshot of when the entire system has more than sufficiently settled and is operating in steady state. P_{DC}^{IC} is the instantaneous power of the DC source the IC is connected to. It can be seen the average (Avg) of said power is basically zero. As theorized, the DC side of the IC is used as a buffer. The root mean square (RMS) of the P_{DC}^{IC} can provide an insight to the size of the buffer required for the IC to be able to provide the unbalanced power support.

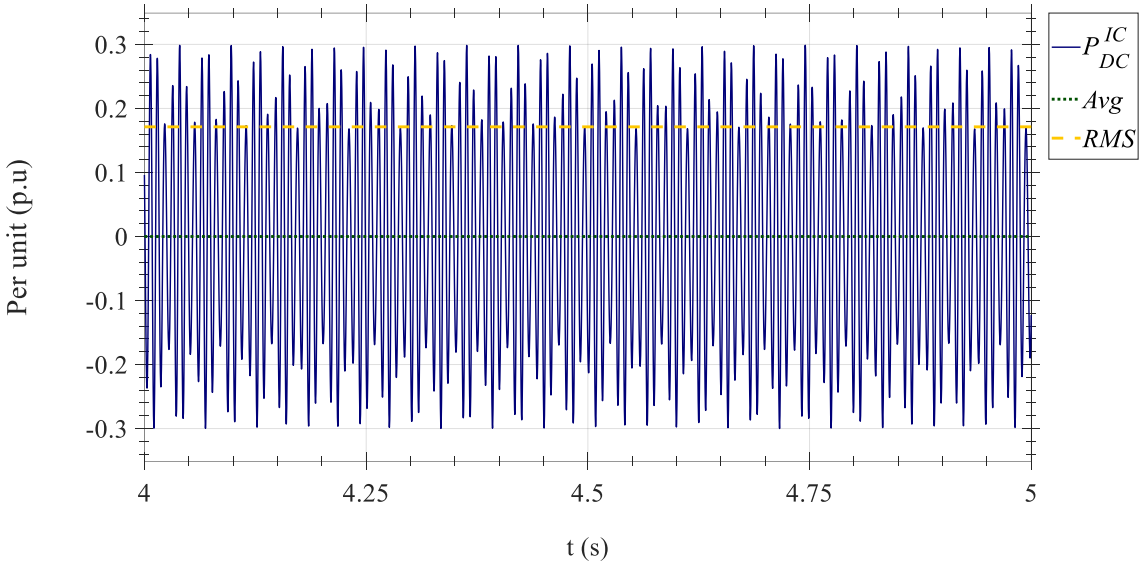

Figure 5.11: Instantaneous and average DC power of an IC vs time

5.5 Comparative Performance

The utilization of a small signal or negative sequence virtual impedance to mitigate the unbalanced power sharing is not unique to this work. The novelty of the proposed control

scheme is the application of such concepts in ICs to maximize the loadability of the HMG. Another salient feature of the proposed control scheme is the usage of under-zero P_{ss}-L_v^- droop. The unbalanced power solutions in the literature utilize droops that yield L_v^- greater than zero. As discussed in CHAPTER 4, this should lead to elevated V^- in the AMG, which is an undesirable side-effect.

The small test introduced in this chapter can also be utilized to highlight the superiority of the proposed control scheme. The following figures will span four events, as laid out in Table 5.2. To have a fair comparison, both droops to be compared start off from a point where the ICs are settled in NSF mode.

Table 5.2: Events details for section 5.5

E#	Description	Start time (s)
E1	ICs in NSF	1.75
E2	ICs using droop from literature	2.25
E3	ICs in NSF	3.5
E4	ICs using the proposed droop	4

Comparing the two droops in questions, it is apparent from Figure 5.12 that the droop presented in the literature results in twice the amplitude of V^- compared to the proposed droop. It should be noted that this test system is a relatively small AMG. Larger grids with higher impedances might exasperate this difference in amplitude. Meanwhile, the proposed droop performed better, though marginally so, than the aggressive NSF mode. The scale of the graph is in the range of 1%. However, this should not be taken lightly. As small that value may appear, it is quite impactful as far as motors are concerned. For example, the loss of motor life at 2% voltage imbalance is up to *four times* as much as it is at 1% [107].

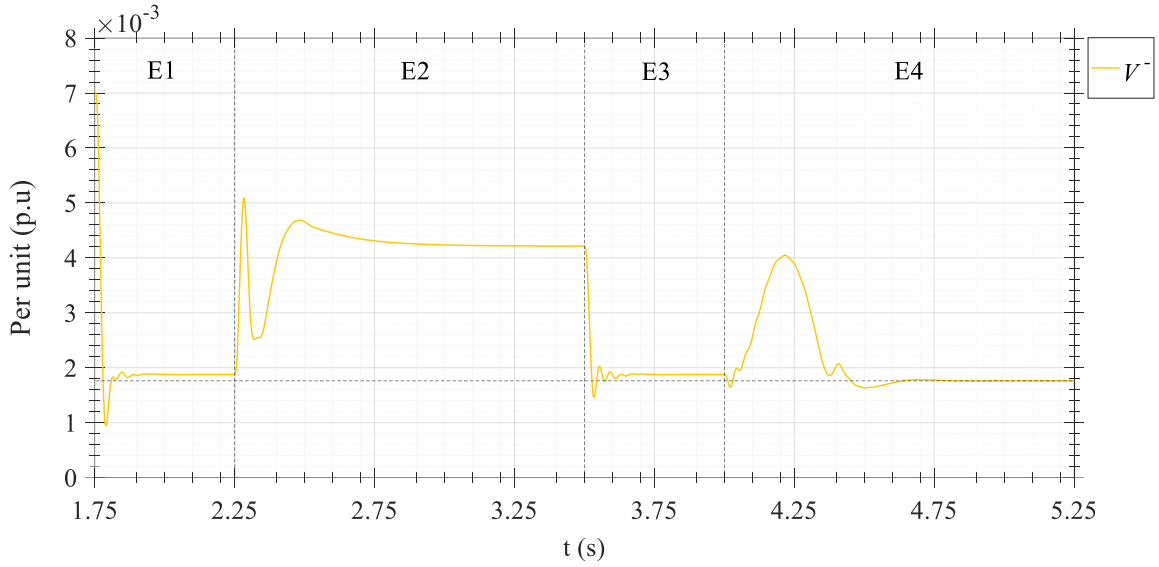

Figure 5.12: Negative sequqnce load voltage to compare control schemes

Looking at the dynamics of L_v^- for the two ICs while using the two droop methods can give a deeper insight, seen in Figure 5.13.

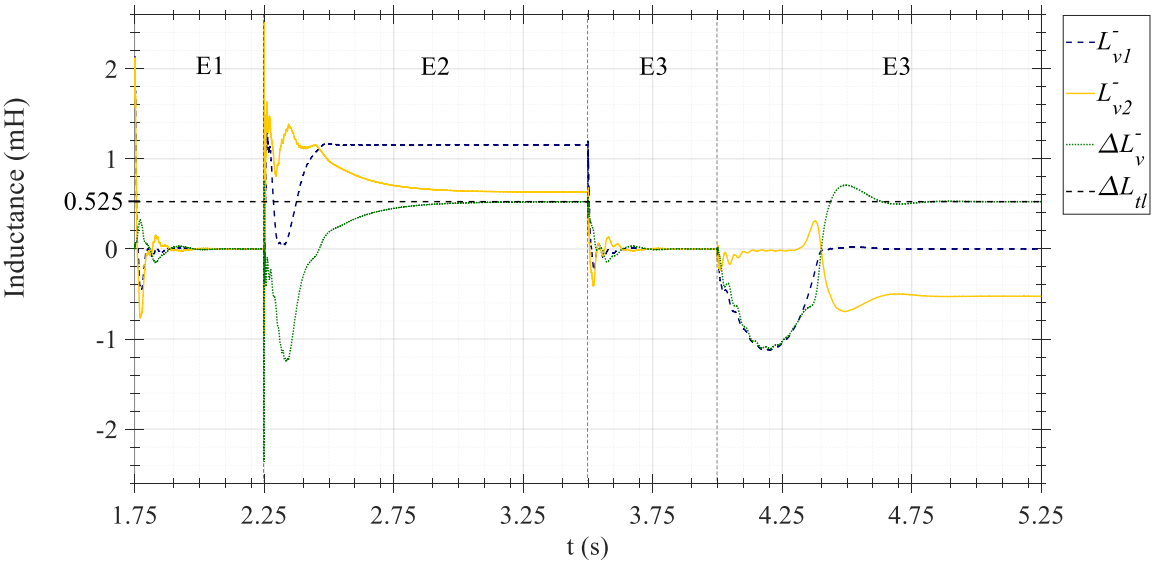

Figure 5.13: Dynamics of the virtual negative sequence inductor for different control schemes

While both droops lead to the required value for ΔL_v^-, the droop from the literature results in both ICs increasing their virtual impedance. This is as opposed to the case of the proposed droop where both values of L_v^- for the two ICs are less than or equal to zero.

Consequentially, both droops result in the convergence of S_U for both ICs, thus the unbalanced power is shared proportionally between them. This is shown in Figure 5.14.

The elevated peak value of S_U in E4 might seem concerning. However, as demonstrated in section 5.3, this has minimum impact on the AMG. This can also be seen in Figure 5.12 where the peak of V^- is well below than the steady state value of V^- using the droop from the literature. Furthermore, the S_U peak in E4 is transitory and settles down in a relatively short time.

While the ICs were modeled to have limits to their outputs, this peak was not enough to reach those limits. Even when this is about worst-case peak as the test system is very small with relatively small line impedance. In practice, it is unlikely to have line impedances smaller than in this test case. Even in the extreme case the spike caused the output current to exceed its limit, for practical reasons, protection breakers have allowance for transitory spikes and often ignore them if they pass by quickly enough.

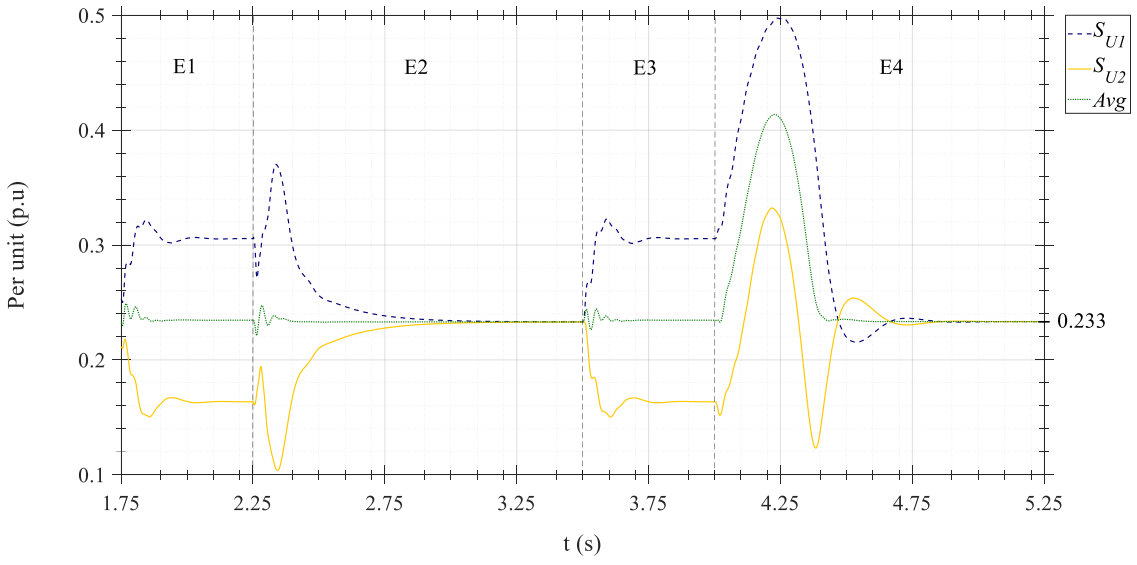

Figure 5.14: Dynamics of S_U during events utilizing different control schemes

CHAPTER 6
CASE STUDY

In the previous chapter, the dynamics of the proposed SSCM were demonstrated, with some comparisons to the alternative solutions found in the literature. This chapter will focus on the steady state performance of the proposed control scheme using a larger test system modeled as 32-bus HMG.

Since the proposed scheme is comprised of several salient features, it should be tested in a stepwise manner. That is, each test case will use the same test system, but with a new feature added each time. The results will show a base case using the conventional droop method, using the negative sequence control method, and lastly, the full proposed methodology with reactive power support. This will help to highlight the impact of each feature on the final result of the maximum loadability of the control scheme.

The performance of the complete scheme, with all the proposed features enabled, will be compared to the results from a centralized solution found in the literature [83]. This centralized solution approaches an ideal solution, so it represents the ultimate standard a control scheme could achieve.

6.1 The Layout of the Test System

To evaluate the proposed methodology, a comparable case study in the literature can be used to establish context. “Test system#1” described in [83] is adopted. For brevity, the centralized coordination method proposed in [83] will be called the Allam Coordination Method (ACM). The AMG of the test system is based on Table 9 of [108]. However, the power unbalance in the listed loads is underwhelming. Furthermore, when the power

unbalance of the total load is calculated, there is even less unbalance. In fact, there's almost zero unbalance in the total shown in Table 6.1. The deviation is a percentage showing how much a phase's loading deviates from the average loading of the three phases.

Table 6.1: Original base loads values

	Pa (kW)	Pb (kW)	Pc (kW)	QLa (kVAR)	QLb (kVAR)	QLc (kVAR)
Phase Total	1073.30	1083.30	1083.30	792.00	801.00	800.00
Deviation	-1%	0%	0%	-1%	0%	0%
Total P (kW)				3239.90		
Total Q (kVAR)				2393.00		

This is because although the loads are unbalanced individually, they are connected to the grid in such a way where their respective unbalanced phases end up balancing out the other phases of the other loads.

Therefore, to get the same amount of unbalance power as shown in the base case of "Test system#1", the AC loads need to be modified. This modification needs to preserve the total power of the loads but increase the total load unbalance. Furthermore, in practice, and according to industry standards, the maximum deviation of the power of a phase of the load from average power of the load is acceptable up to ≈ 33.3% [104].

To keep the case study within these standards and conditions, the load imbalance is set up in a way where the three-phase loads are loaded from least to most in terms of phase a, b, and c, respectively. That is:

$$P'_{a,i} = 0.7\frac{\sum_{a,b,c} P_{x,i}}{3}$$

$$P'_{b,i} = \frac{\sum_{a,b,c} P_{x,i}}{3},$$

$$P'_{c,i} = 1.3\frac{\sum_{a,b,c} P_{x,i}}{3}, \quad (6.1)$$

where $P'_{a,i}$, $P'_{b,i}$, and $P'_{c,i}$ are the modified base loads of phases *a*, *b*, and *c* of the *i*th base load, respectively. This way, the average and total base load are preserved. Yet, it creates the desired 30% imbalance, which is within the limits of the standards. The total base loads with the modified values can be seen in Table 6.2.

Table 6.2: Modified base loads

	Pa (kW)	**Pb (kW)**	**Pc (kW)**	**QLa (kVAR)**	**QLb (kVAR)**	**QLc (kVAR)**
Phase Total	755.98	1079.97	1403.96	558.37	797.67	1036.97
Deviation	-30%	0%	30%	-30%	0%	30%
Total P (kW)				3239.90		
Total Q (kVAR)				2393.00		

The DMG part of the HMG of the test system is based on [109] with the addition of some DC loads. These loads are as specified by TABLE IV in [83]. It should be noted that in this configuration, the total DC loads is slightly greater than the total maximum power of all DC generators combined. Consequently, the DMG will always be more loaded than the AMG, and hence the real power transfer will always be from the AMG side to the DMG in this case study.

6.2 Determination of the Maximum Loadability

During the design and planning phase of the grid, it is important to know how much power load the grid can handle before it becomes unstable, or before a certain condition is

violated. To determine that, the base values of the loads are multiplied by the loadability factor, λ, such that

$$S_{load} = \lambda S_{base} \tag{6.2}$$

Then, the grid is simulated using S_{load}. λ is increased until the grid becomes unstable, or a certain condition is violated. At that point, it can be said the simulation, or the grid, have failed. In general, the maximum value of λ the grid can withstand without failing is know as the maximum loadability, λ_{max}. The failure conditions in the case studies are as follows

$$S_{ph,x}^{DG,i} > S_{ph,limit}^{DG,i}, \forall x \in \{a, b, c\} \tag{6.3}$$

$$P_{DG,i} > P_{DG,i}^{max} \tag{6.4}$$

where $S_{ph,x}^{DG,i}$ is the apparent power of any phase of the *i*th AC DG. $S_{ph,limit}^{DG,i}$ is the per phase apparent power limit of the *i*th AC DG. $P_{DG,i}$ is the active power supplied by the *i*th AC DG. $P_{DG,i}^{max}$ is the maximum active power of the same DG. If either (6.3) or (6.4) are true, then the simulation is deemed to have failed.

The maximum loadability in the context of this thesis relates to the maximum loadability of the test system, λ_{max}^{system}. This is achieved when the active power generated by a DG, P_{DG}, reaches it maximum limit without violating any other conditions, like the power limit of a phase, S_{limit}^{ph}, or the total limit of DG or IC, S_{limit}^{DG} or S_{limit}^{IC}, respectively. In the ACM paper, λ_{max}^{system} for "Test system#1" was found to be 1.15. At that point, the active power generated by the DGs is maxed out, and no further power can be produced without violating the law of conservation of energy.

However, there are some slight variations between the model used for this thesis and the one used for the ACM. Therefore, the value of λ_{max}^{system} might differ slightly. However, it will be shown that the proposed methodology is able to maximize P_{DG} for all AC DGs. This means that the proposed methodology is able to achieve true maximum loadability. In other words, it will be proven that using the proposed methodology, the only thing limiting the loadability is active power limits of the DGs.

For any method tested using the system designed for the test case, the maximum λ that can be achieved before any limits are violated will be referred to as λ_{max}^{method}. When λ_{max}^{method} is equal to λ_{max}^{system}, then it can be said the method is able to achieve true maximum loadability.

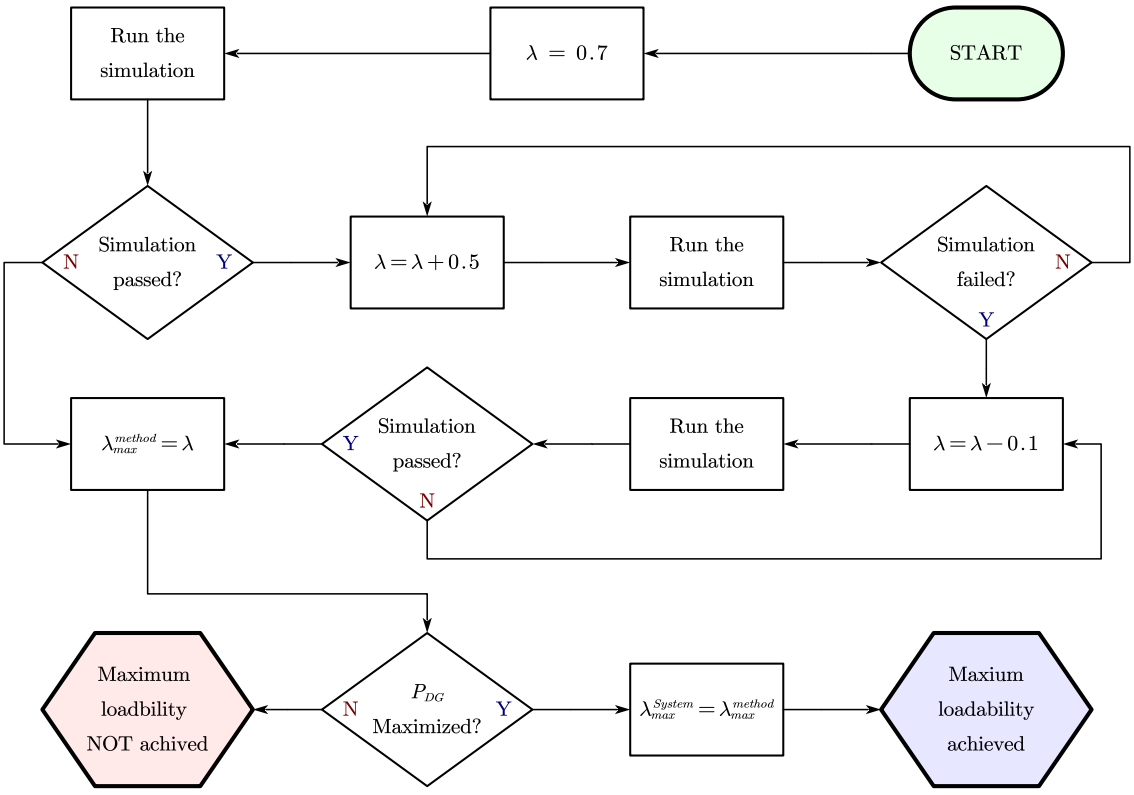

Figure 6.1: Flowchart of the process of determining the maximum loadability of a method

According to [83], the conventional decentralized droop method has a λ_{max}^{method} of 0.74. Therefore, a value of 0.7 can be used as a safe lower limit to λ.

Therefore, the solution of any test case studied here should have λ_{max}^{method} in the range of [0.7, 1.15]. Using MATLAB/Simulink, each test case is simulated starting at $\lambda = 0.7$. If the simulation passes, λ is increased by a step of 0.5. That is, the next step is to simulate the test case at $\lambda = 0.75$. Should the simulation pass, another step is added, and so on and so forth until the test case fails.

Then, λ is reduced by a step of 0.1. If the simulation passes, then that value λ is declared λ_{max}^{method}. If it fails, then the simulation is run iteratively with a reduced step of 0.1 until it passes. Then, the value of λ at that iteration is declared λ_{max}^{method} of that test case. If P_{DG} of all AC DGs is at 100%, the λ_{max}^{system} is determined to be equal to λ_{max}^{method}, and the method is determined to have achieved the maximum loadability. A flow chart depicting this process can be seen in Figure 6.1. With these rules and conditions in place, it is possible to run the case study.

6.3 Conventional Droop Method

In this subsection, the conventional droop method will be put to the test. This will create a baseline to compare the other methods with. This should yield comparable results to the base case in [83]. At that point, it reasonable to claim that the test systems are comparable.

While the conventional droop method provides adequate decentralised coordination for active power sharing, it assumes a balanced grid. However, in the unbalanced case, issues will arise due to the unequal power loaded on each phase. This can limit the generator's total power output significantly. This is because current limit protection is rated per phase.

The protection mechanism is potentially triggered due to an over loaded phase even if the other two are unloaded.

Similar to the results obtained in the centralize method's paper, the maximum loadability for the conventional droop was found to be 0.72. That is less than 3% difference from what was obtained in the ACM paper. The phasing loadability can be seen in Figure 6.2.

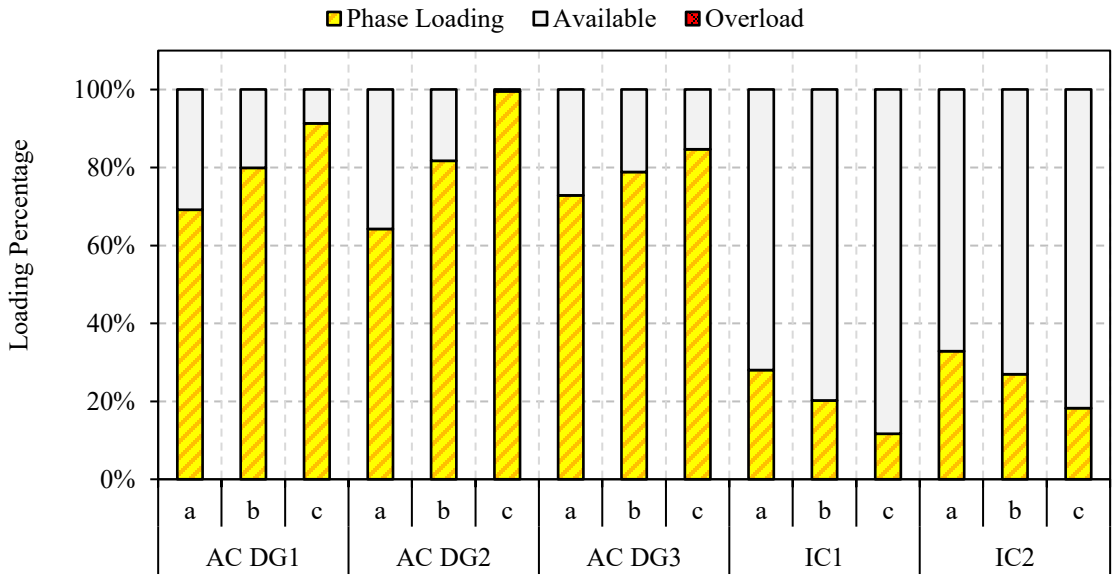

Figure 6.2: Loadability of phases at $\lambda = 0.72$ using the conventional droop method.

It can be seen that the limiting factor with this method is phase *c* of AC DG2. With any loadability greater that 0.72 for this coordination method, phase *c* would become overloaded, which can be seen in Figure 6.3. It should be noted that at this loadability, all AC DGs are loaded at 81.9%. That means using the conventional method leads to the underutilization of the DGs by 18.1%.

If phase *c* were to become overloaded in practice, this would trigger the overload protection mechanism of AC DG2, disconnecting it from the grid. If that were to happen, at that point, the other DGs would have to shoulder the burden left behind by AC DG2.

However, they would not have the spare capacity to do that. That would lead to either the grid collapsing, or some loads having to be shed. That is, some loads will have to be disconnected from the grid, which is undesirable. It should be note that this is not done in the simulation just to showcase how the overload would look like, in theory.

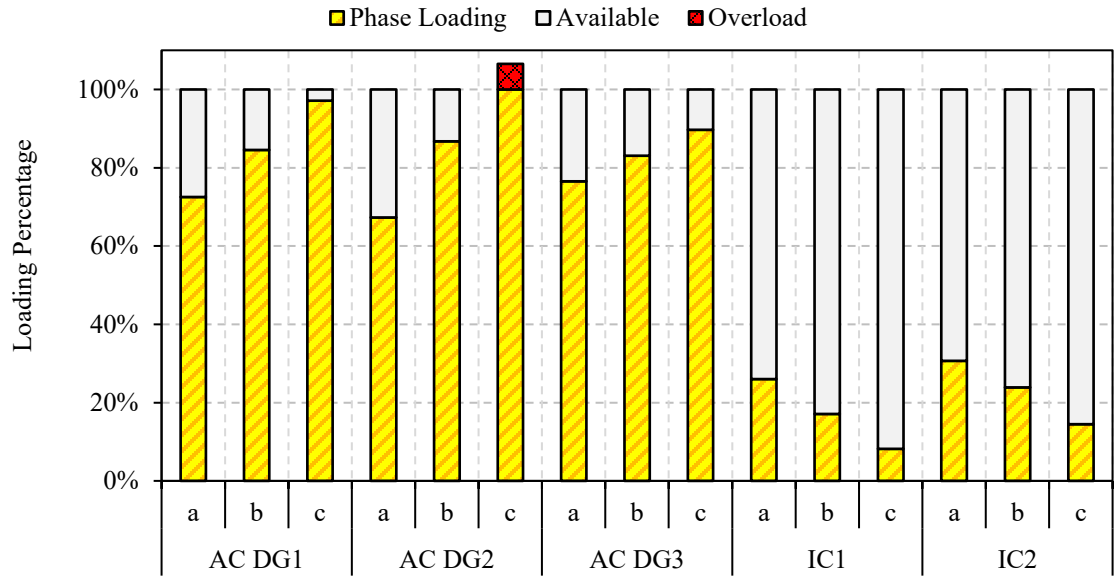

Figure 6.3: Loadability of phases at $\lambda = 0.8$ using the conventional droop method.

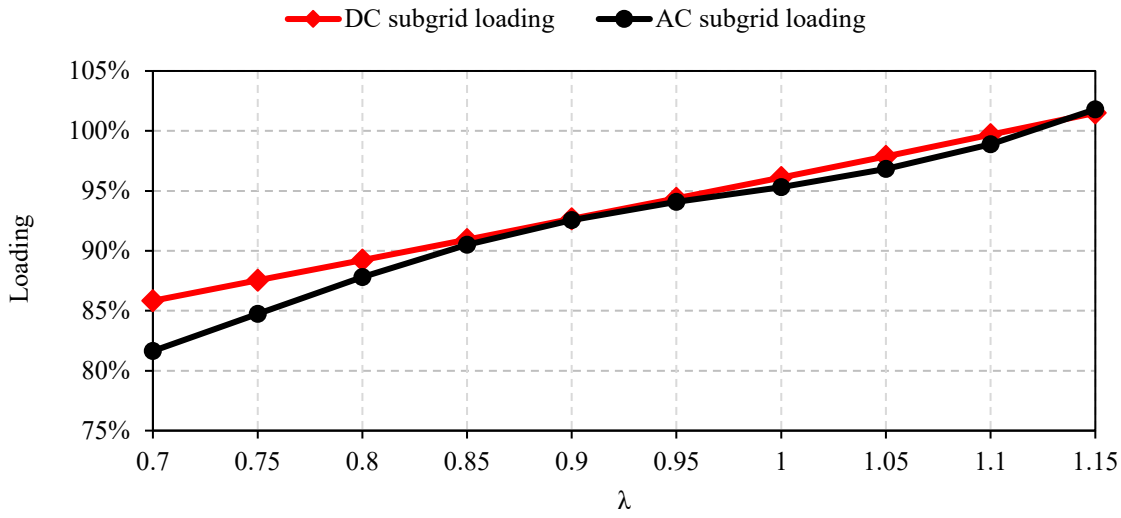

Figure 6.4 Subgrid Loadability vs lambda

To further showcase the similarity between the model used here and the one used in the ACM paper, the grids loadability versus λ is plotted in Figure 6.4. While it is not a perfect fit, this proves the models for the case study are comparable.

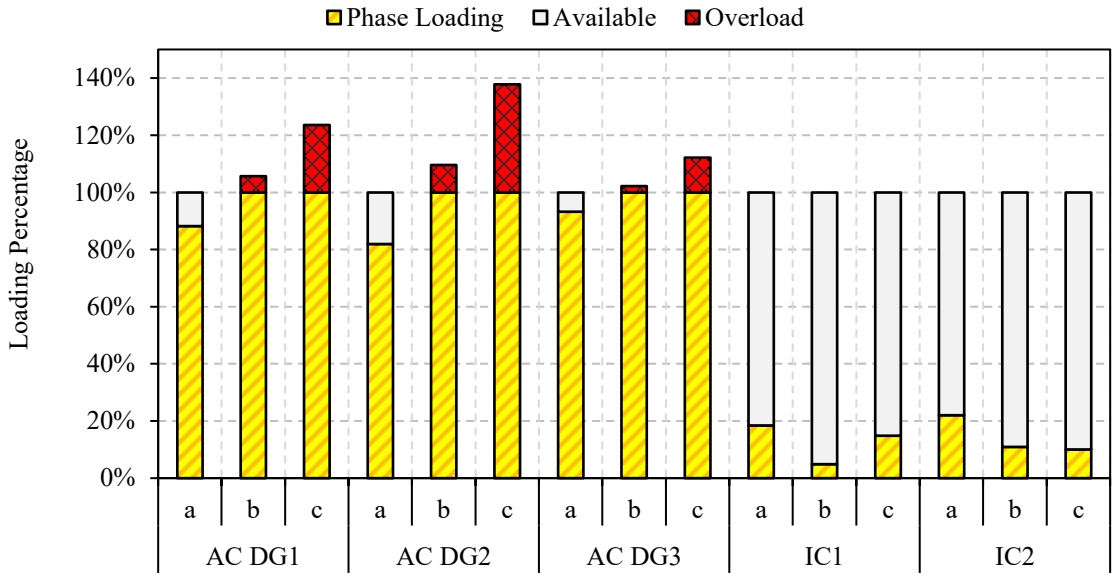

Figure 6.5: Loadability of phases at $\lambda = 1.15$ using the conventional droop method.

For further comparison, Figure 6.5 shows the phase loading the maximum theoretical loadability where $\lambda = 1.15$. It can be seen the result is comparable with that shown in ACM paper with the results for 1.15.

6.4 Improved Droop with Negative-Sequence Control

By implementing the direct negative sequence control proposed in the section 4.2, it can be seen that there is a significant improvement to the loading of the phases of the DGs, where they are almost perfectly balanced, like all things should be. Meanwhile, all of the unbalanced power is provided by the ICs, as theorized. This can be seen in Figure 6.6.

All AC DGs are producing active power at 93.8% of their limit. The discrepancy in the phase power between DGs seen in the figure is due to the reactive power sharing error using the convention Q-V droop, which is expected.

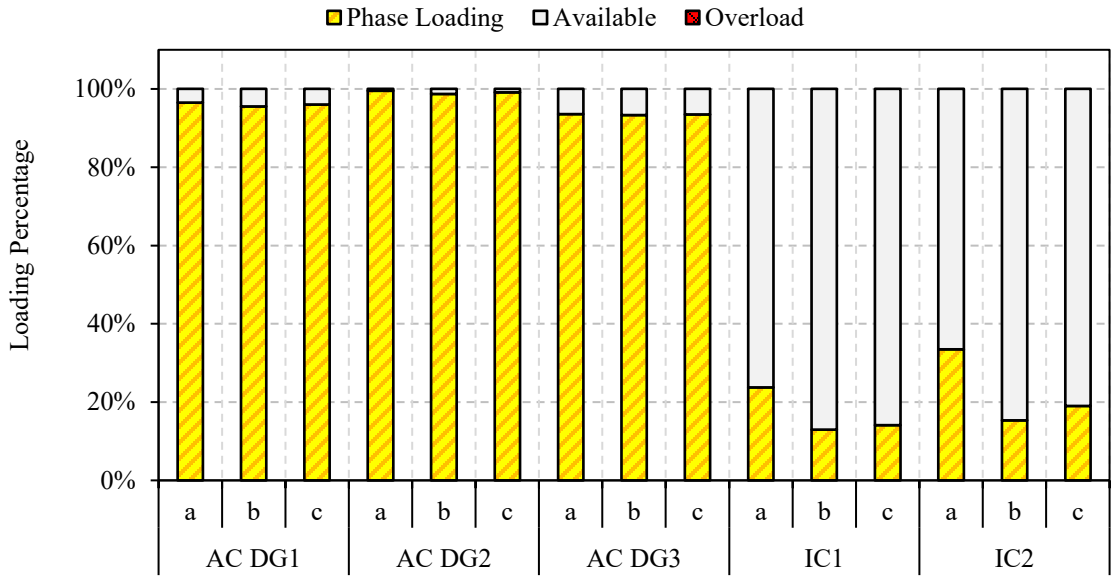

Figure 6.6: Loadability of phases at $\lambda = .99$ using direct negative sequence control method.

As for the loadability, it increased from the 0.72 of the baseline case to 0.99. This is a significant improvement, but not yet the most that can be achieved using the full proposed control scheme. It seems that the limiting factor for this method is the reactive power burden on the DGs. This is why the complete form of proposed coordination method includes reactive power support by the ICs.

6.5 Proposed Small Signal Coordination

By having the IC utilize the small signal, the unbalanced power provided by them is proportionally shared between them with minimal error, as seen in Figure 6.7.

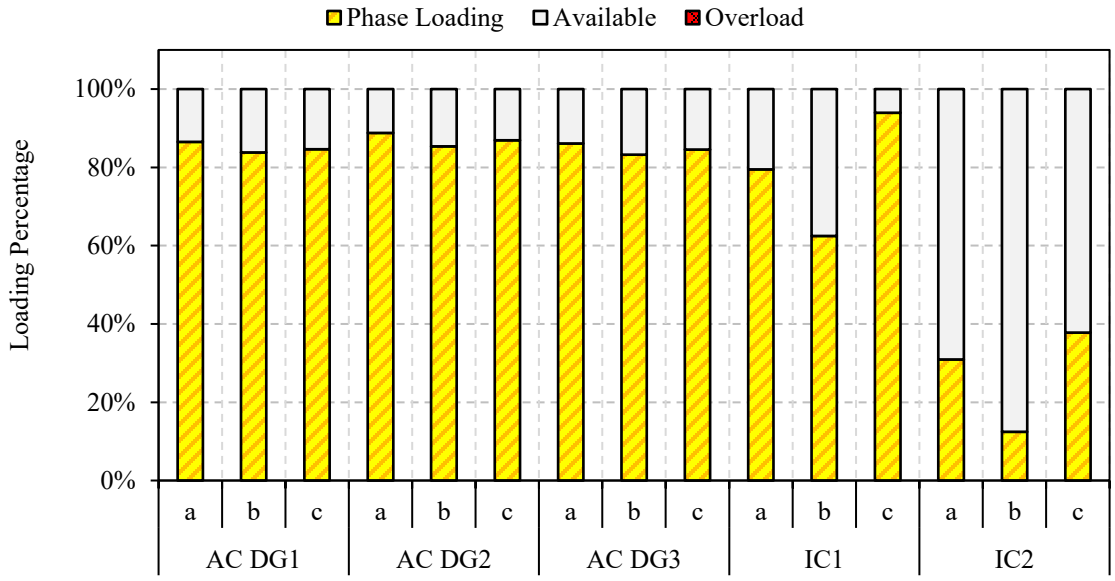

Figure 6.7: Loadability of phases at $\lambda = 1.15$ the SSCM with reactive power support.

Most of the reactive power generation is done by the ICs in this method. This is why there exists a discrepancy between the phase powers of the ICs. Using this method, λ_{max}^{method} is found to be 1.15. The only limiting factor for this case is that the AC DGs reached their P_{DG} limits. That is, all AC DGs are running at 100% of their rated active power generation. Therefore, this is also the λ_{max}^{system}. Accordingly, this means the method achieved the goal of maximizing the loadability of the system.

CHAPTER 7
CONCLUSIONS AND FUTURE WORK

7.1 Conclusions

The modernization of the electric grid to adapt to the emerging technologies of loads and power generators requires the development of robust hybrid microgrids. While centralized control schemes that facilitate communication and coordination across microgrids can optimize their operation to the theoretical maximum limit, the practical application is costly, slow to react to changes, and prone to single point failures.

A decentralized approach would fulfill the ideals of microgrids being robust, flexible, fast-reacting, and accessible to consumers and end users. The small signal coordination method can reach steady state zero sharing error in less than a second compared to the hours required for the centralized approach, while not requiring any added communication lines or added devices.

Using a under-zero droop for the virtual negative sequence inductance, the drawbacks of the conventional virtual impedance are eliminated. In fact, the proposed droop added a layer of intelligence to the elimination the negative sequence voltage, leading to a reduction of the voltage imbalance, even when compared to the aggressive NSF mode.

Furthermore, the loadability of the grid was maximized to a level comparable to that of the centralized approach. Since the proposed control schemes is utilizing a decentralized approach, this should be compared to the maximum loadability using a conventional decentralized method, which yielded a maximum loadability of only 0.72. In other words, a 59.7% increase over the conventional decentralized method. In addition to that, the ICs

were utilized for maximum grid support, like reactive power support and unbalanced voltage reduction and mitigation.

7.2 Contributions

The contributions of this work can be summarized as the following:

1. Assigning the DGs and ICs different negative sequence operation modes to eliminate any unbalanced power generation from the DGs, while shifting that burden onto the ICs.
2. The adaptation of the small-signal coordination method for the unbalanced power into a unified dq-frame control scheme for the interlinking converters, allowing them to share the burden of the unbalanced power that shifted onto them due to their operation mode.
3. The modification of the negative sequence impedance droop to yield only under-zero virtual inductance values, eliminating the disadvantage of using the virtual impedance for unbalanced power sharing.
4. Developed the triple-notch filter to for the symmetrical component decomposition and small signal extraction. This filter allows for greater bandwidth for the controller, which greatly decreases the delay and response time of the controller compared to using a low-pass filter. The step response of the proposed filter is around 15.66 time faster than a comparable method.

7.3 Future Work

While the proposed methodology yields what is practically the theoretical maximum loadability possible using a decentralized and communication-free method, there are other

aspects that could be improved upon. After all, the maximum loadability is only one part of the equation for a robust HMG. As seen in section 6.3, there are some discrepancies in the real power sharing between the AMG and DMG. This is due to the fact that the ICs can't accurately determine the loading of the DMG from the local voltage measurements. To fix this issue, methods where the real power sharing in the DMG are made into global variables. Such methods already exist in the literature [88]–[90], but it is necessary to that they be incorporated into the proposed methodology to fill its shortfalls.

Furthermore, the triple-notch is not the ideal solution for the symmetrical components decomposition as it still introduces some delay in the control loop and reduces the bandwidth of the controller. Alternative solutions in the literature exist where the components can be estimated [110]–[114] with out any filtering action. This has the potential to eliminate the requirement for the triple notch filtering, or even any filtering, ideally.

The impact of the small signal is minimized by restricting its amplitude. However, it is technically added noise to the system, where ideally only the voltage of fundamental frequency should exist. A technique that could be a candidate to replace the small signal is the adaptive virtual impedance that allows the coordination of the virtual impedance between the ICs without needing to inject a small signal [115]. Or perhaps, a novel technique could be developed where the usage of the small signal is not necessary.

Even without those improvements, it is important to create a power flow model for this decentralized control scheme. This allows for a significantly faster simulation and analysis of HMGs utilizing the proposed methodology compared to the current average model simulated using Simulink/MATLAB. The power flow model is especially important for

the design of HMG utilizing the proposed scheme, as optimization functions could be used, for example, to size the DGs and ICs.

After developing the power flow model, the proposed methodology could be rigorously tested on larger HMGs. For example, using the IEEE 123-bus test system, as used in [83], or perhaps even large HMGs.

Lastly, the proposed control scheme needs to be tested and adapted for operating in grids with non-linear loads, harmonics, and noise. Harmonics due to non-linear loads is a significant issue in modern grids, so techniques to mitigate it [116] could be a valuable addition to the arsenal of techniques used in the proposed control scheme. It might even be done in a way for the ICs to carry the burden of mitigating harmonics in the HMG, instead of relying on the DGs for that role.

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