1-1-1964

A digital controller strategy for optimization and adaptation of control systems representable in the phase plane.

Robert J. Rayzak
University of Windsor

A DIGITAL CONTROLLER STRATEGY
FOR OPTIMIZATION AND ADAPTATION
OF CONTROL SYSTEMS
REPRESENTABLE IN THE PHASE PLANE

BY

ROBERT J. RAYZAK

A Thesis
Submitted to the Faculty of Graduate Studies Through the
Department of Electrical Engineering in Partial Fulfillment
of the Requirements for the Degree of
Master of Applied Science at
University of Windsor

Windsor, Ontario
1964

ABK1166

APPROVED BY:

P.A.V. Thomas

A. C. Smith

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ABSTRACT

This thesis proposes a novel digital method for optimization and adaptation of control systems representable in the phase plane.

By continually generating its own optimum trajectories the digital controller has sufficient intelligence to discern optimum switching points and system parameter changes.

The optimum trajectory is stored in memory as error addressed to memory position by a pseudo error rate, which is determined by a difference of error over a constant sampling period. Thus, no direct measure or calculation of error rate is necessary.

Simulation studies by digital computer show that this method is a worthwhile consideration in the field of optimum adaptive controls, and awaits the completion of a digital controller being constructed to implement and further study the system.

ACKNOWLEDGEMENTS

To Dr. P. A. V. Thomas, who supervised this work and gave much helpful advice in its course, must go the author's appreciation.

Acknowledgement is also due the National Research Council for financial assistance provided for this project.

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I. INTRODUCTION

In the general field of control system theory, optimization of error responses plays an important role and a method for system optimization covering a wide set of disturbances is a most valuable consideration. Moreover, if the system can in some way detect its own parameter changes and is in this sense adaptive, it will perform optimally under a wider set of conditions and augment the value of the technique.

This study proposes a digital computer controller (DCC) method of optimization and adaptation of systems representable in the phase plane. Such a system is shown in Fig. I-1.

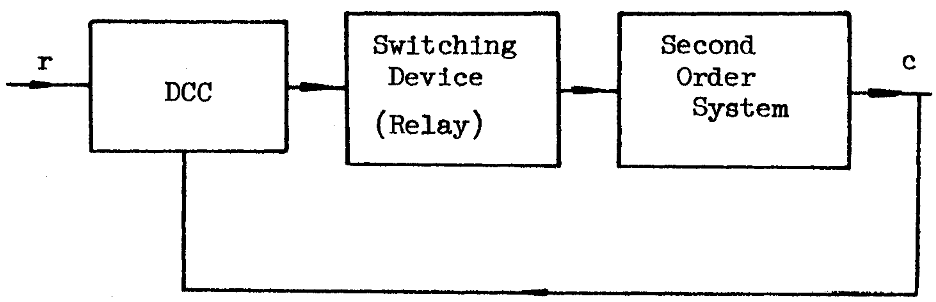

FIG. I-1 SYSTEM CONSIDERED FOR ADAPTIVE OPTIMIZATION

1. Definitions of Optimization and Adaptation.

Whereas systems may be defined to be optimum and adaptive according to many criteria, this thesis considers the terms in the following senses.

Optimization is taken to mean the reduction of error and all its derivatives to zero in the fastest possible time. That is, for a system representable in the phase plane, the system must switch once at a point corresponding to the intersection of the initial system trajectory with the optimum zero-trajectory.

Since the term "adaptation" has been given several connotations over the past years it is necessary to define adaptation in the sense used in this thesis. A system which performs to some given standard (optimally in this study) under one set of system parameters whose change would normally cause the system to deviate from this standard and which performs to the same standard after a change of the parameters is considered adaptive.

2. Some Previous Workers' Attempts at System Optimization and Adaptation.

Other workers in the field[1,2] have proposed means of optimization and adaptation. Brown's system will be discussed here since the author of this thesis attempted it initially with the aim of employing it in more complex systems (i.e., systems which are not pure-inertial).

In Brown's paper a pure inertial system is described where a linear switching function may adapt itself to the nature of the input and to slow variations of control system characteristics. However, Brown's method has some objectionable features. First, for best results, the system takes several runs before its response is optimized. In a practical system whose disturbances and characteristics (parameters) might be continually changing, optimum response might never be achieved. Second, the control method requires direct utilization of error rate in its calculations. Digital implementation of error rate must be achieved by a finite difference calculation or an encoder. The former takes considerable time and increased DCC complexity in terms of registers and the latter are not readily available.

However, other methods of achieving the goals may be readily proposed subject to considerations of practicality and generality. The author has investigated several of his own initial proposals and a few of these will be briefly discussed.

3. The Author's Preliminary Investigations.

For a pure inertia system, it can be readily shown[3] that optimum performance will occur if the system is switched at a point where the present error ϵ_s equals one-half the initial error on the error axis intersection, ϵ_o. Moreover, this criterion is independent of the system inertia and as such the response will be optimum for any value of inertia if switched where

$$\epsilon_s = \epsilon_o/2 \qquad (I - 1)$$

It was felt that perhaps such a criterion could be developed, at least empirically, for systems with the general differential equation

$$a_2\ddot{\epsilon} + a_1\dot{\epsilon} + a_o\epsilon = \text{sgn } F(\epsilon,\dot{\epsilon}) \qquad (I - 2)$$

where "sgn" means "the sign of".

Solution of the optimum switching line with the response curves of a second order damped system in the second and fourth quadrants of the phase plane readily show such a simple criterion is not analytically possible.

However, if a curve of error rate at switching time, $\dot{\epsilon}_s$, is plotted against initial error, ϵ_o, on the error axis, it is found this curve approximates an actual positive torque response curve in the phase plane. Fig. I-2 illustrates the scheme.

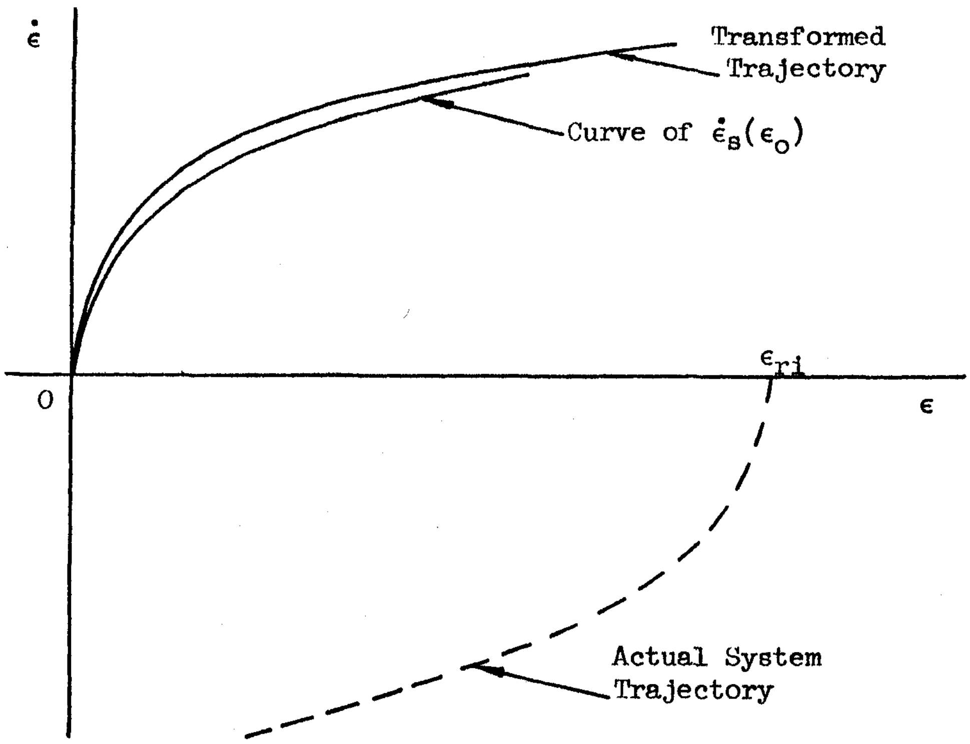

FIG. I-2 GENERATION OF OPTIMUM SWITCHING ERROR RATES

Hence, the transformations

$$\begin{aligned} \epsilon_{ri} - \epsilon_r &\longrightarrow \epsilon_o \\ |\dot{\epsilon}_r| &\longrightarrow |\dot{\epsilon}_s| \end{aligned} \qquad (\text{I - 3})$$

where subscript r refers to "response", i to "initial", and the arrow indicates "replaces" may be used to generate a curve of optimum switching points, $\dot{\epsilon}_s$ (ϵ_o).

Digital computer simulation of such a control strategy proved that the errors in switching were too large and response was sub-optimum. However, the technique of generating actual system trajectories to use in a control strategy showed promise since adaptation would be natural. That is, if the system trajectory changes, the control strategy will change accordingly.

Consider an optimum switching of a pure inertia system in the phase plane as in Fig. I-3. The subscript, o, refers to "optimum".

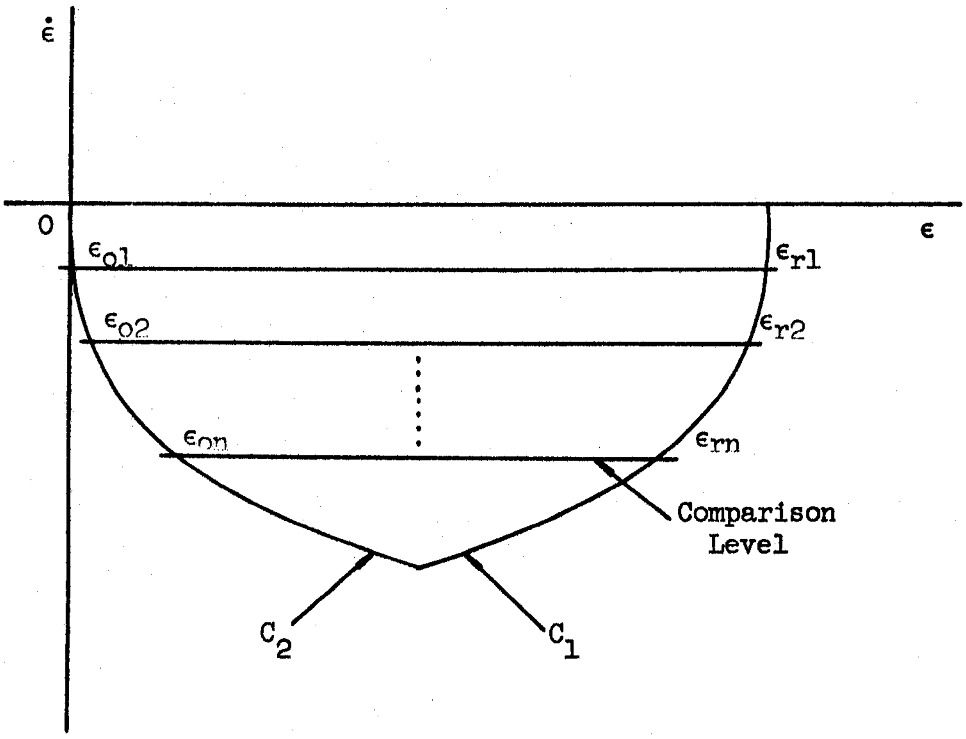

FIG. I-3 COMPARISON OF ERROR IN THE PHASE PLANE

Note that time along either trajectory is equal between the same comparison levels. That is,

$$\int_{\epsilon_{rn-1}}^{\epsilon_{rn}} \frac{d\epsilon}{\dot{\epsilon}} = \int_{\epsilon_{on}}^{\epsilon_{on-1}} \frac{d\epsilon}{\dot{\epsilon}} \qquad (\text{I}-4)$$

Hence, if a memory in the DCC is filled in with values of error on C_2 at successive sampling intervals, $T = t_n - t_{n-1}$, and compared with values of error on C_1 for successive sampling instants, the point will occur where $\epsilon_{rn} = \epsilon_{on}$ and an optimum switch can be commanded by the DCC. Again, if C_2 is continually filled into the DCC memory, the system will have sufficient intelligence to note a change in its parameters and will perform optimally under such changes.

However, for a system with inertia plus viscous damping, C_1 and C_2 are not similar and equation (I-4) does not hold. Still, if instead of addressing the memory for successive sampling times, the DCC memory is addressed in terms of error difference for successive sampling times, in effect the DCC memory stores error in terms of error rate. Hence a complete curve of $\epsilon(\dot{\epsilon})$ is stored in memory for comparison against an actual trajectory.

This concept forms the basis for the major portion of this thesis which will now deal with logic implementation and simulation of the above strategy to a second order positioning servo. It is to be noted however, that the method is in general applicable to any phase plane representable system.

II. DEVELOPMENT OF DIGITAL COMPUTER CONTROLLER LOGIC

Basically, a system represented in the phase plane will yield optimum performance when it detects its own trajectory response intersecting with the optimum trajectory and switches at this point.

Referring to Fig. II-1 it can be seen that the system will switch at point $S(\epsilon_s, \dot{\epsilon}_s)$ when the errors and error rates of the response trajectory and the optimum trajectory correspond. This procedure may be achieved in the following manner.

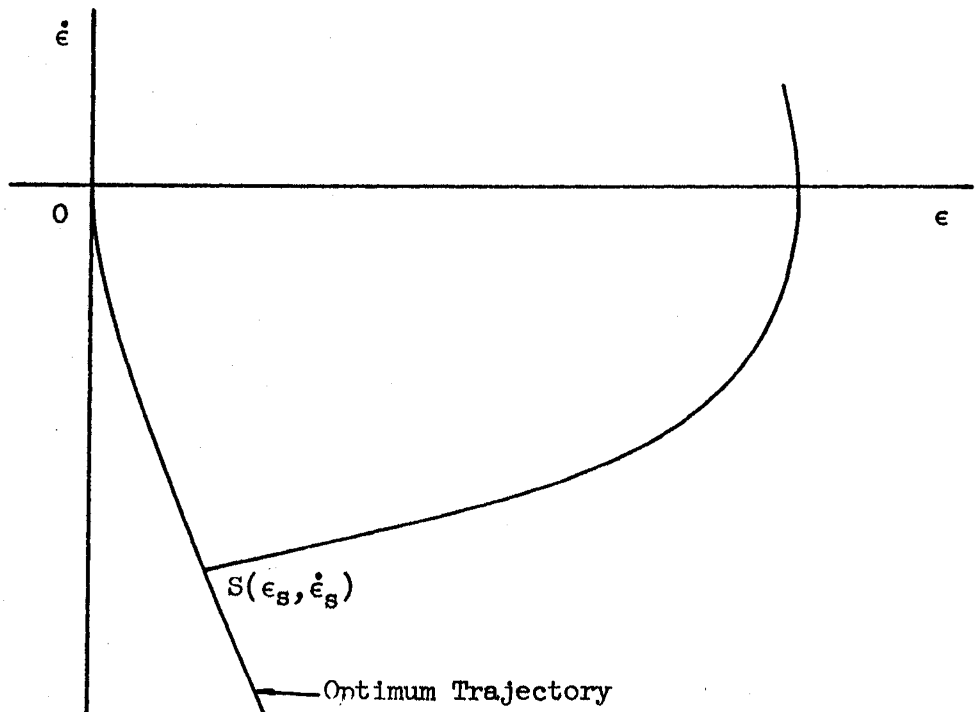

FIG. II-1 DEMONSTRATION OF OPTIMUM SWITCHING

If the optimum curve is stored in memory for comparison between an arbitrary response and itself then optimum switching will occur at an intersection. However, it is not convenient to compute or measure error rate directly by digital means. As has been demonstrated in section I of this thesis error may be compared at constant level changes in error rates up to the switching point. This concept leads to the primary decision strategy in the DCC.

It is known that error rate may be approximated by the relation,

$$\dot{\epsilon}(t) \cong \frac{\Delta\epsilon}{\Delta t} = \frac{\epsilon_2 - \epsilon_1}{\Delta t} \qquad \text{(II - 1)}$$

where ϵ_2 is the present error considered and ϵ_1 is the previous error considered. The time difference, Δt, is the time between these two values.

Now if the DCC samples error every T seconds then

$$\dot{\epsilon} \cong \frac{\epsilon_2 - \epsilon_1}{T} \qquad \text{(II - 2)}$$

However, it was noted that if the DCC samples error at a constant T then only a difference in error will define the error rate. That is,

$$\Delta\epsilon = \epsilon_2 - \epsilon_1 \longrightarrow \dot{\epsilon} \qquad \text{(II - 3)}$$

The DCC will have a memory and in lieu of storing error and error rate for comparison, error alone may be stored in a memory at the address $\Delta\epsilon$. In an actual DCC to be built ϵ and hence $\Delta\epsilon$ will be integral values. Thus, the upper bound of memory locations will be the highest integral error rate expected.

If a response error presented for comparison is denoted as $\epsilon_r(\Delta\epsilon_r)$ and an error stored in memory as $\epsilon_m(\Delta\epsilon_m)$ then the decision process for optimum switching is

$$\text{IS} \quad \epsilon_r(\Delta\epsilon_r) \leqslant \epsilon_m(\Delta\epsilon_m)\Big|_{\Delta\epsilon_m = \Delta\epsilon_r} \quad ? \qquad \text{(II - 4)}$$

where switching occurs on affirmation.

The problem now arises as to how to obtain the memory curve. Fig. II-2 shows that an optimum switching curve is the negative torque response shifted along the ϵ-axis. The various negative torque trajectory portions shown indicate that an optimum curve is given by

$$\epsilon_{opt.} = \epsilon_{act.} - \epsilon_f \qquad (II - 5)$$

where ϵ_f is the curve offset from origin and ϵ_{act} is the actual response error.

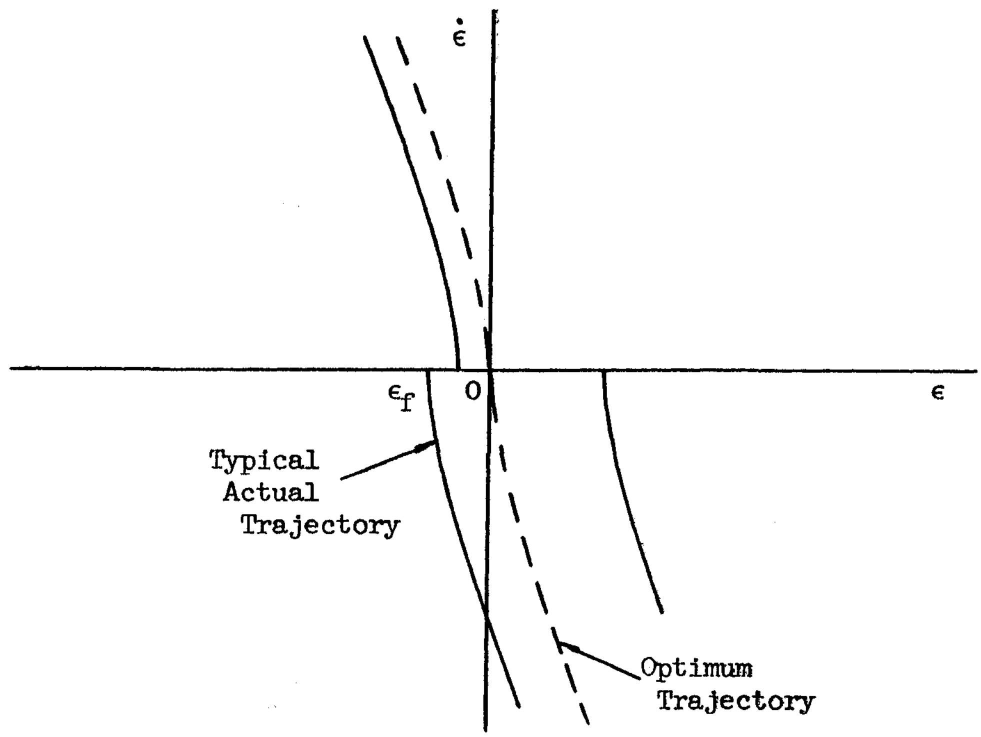

FIG. II-2 GENERATION OF OPTIMUM SWITCHING LINE

Hence an optimum response curve may be stored in memory by storing the negative torque portion of the response as $\epsilon_m(\Delta\epsilon_m)$. Comparison in Fig. II-1 is made according to equation (II-4) if

$$\epsilon_m(\Delta\epsilon_m) - \epsilon_f \longrightarrow \epsilon_m(\Delta\epsilon_m) \qquad (II - 6)$$

However, comparison may be effected in the second quadrant and another in the fourth quadrant. This is accounted for if

$$|\Delta\epsilon| \longrightarrow \Delta\epsilon \qquad (\text{ II - 7 })$$

and

$$|\epsilon_m(\Delta\epsilon_m) - \epsilon_f| \longrightarrow \epsilon_m(\Delta\epsilon_m) \qquad (\text{ II - 8 })$$

in equation (II-6).

Thus, the memory table of $\epsilon_m(\Delta\epsilon_m)$ may be stored directly from any negative torque trajectory and compared as

$$\text{IS} \quad |\epsilon_r(|\Delta\epsilon_r|)| \leq |\epsilon_m(|\Delta\epsilon_m|) - \epsilon_f|\Big|_{|\Delta\epsilon_r| = |\Delta\epsilon_m|} \; ? \qquad (\text{ II - 9 })$$

Several cases of initial conditions may now be considered in order to develop more fully the controller for table fill-in and comparison. Figs. II-3a-d show four general initial conditions (IC) and resulting responses assuming no table in memory is initially available for comparison. The points P_i (i=1,2,3,4) shown on the figures have the following meanings.

P_1, start to compare actual response with blank table.

P_2, start to fill in table after switching on sgn (ϵ).

P_3, stop filling in table and start to compare table with acutual response. Store ϵ_f.

P_4, switch optimally.

Some general conclusions may be made from consideration of these figures. First, comparison of an actual response with the optimum switching line is made only if

$$|\epsilon_2| \leq |\epsilon_1| \qquad (\text{ II - 10 })$$

that is, starting on the ϵ-axis.

Second, the table is placed in memory only when there is a switch on a change of sgn (ϵ). It will be seen later to avoid undesirable responses the table should be filled only after the first switching following initiation of the response. This may be conveniently

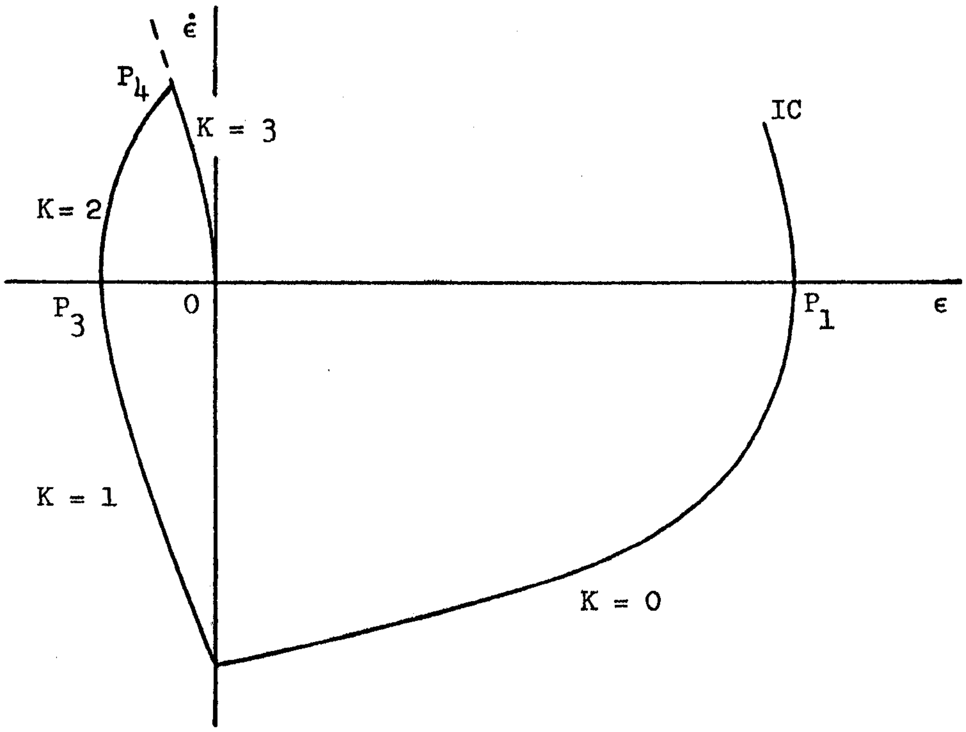

FIG. II-3a IC IN FIRST QUADRANT

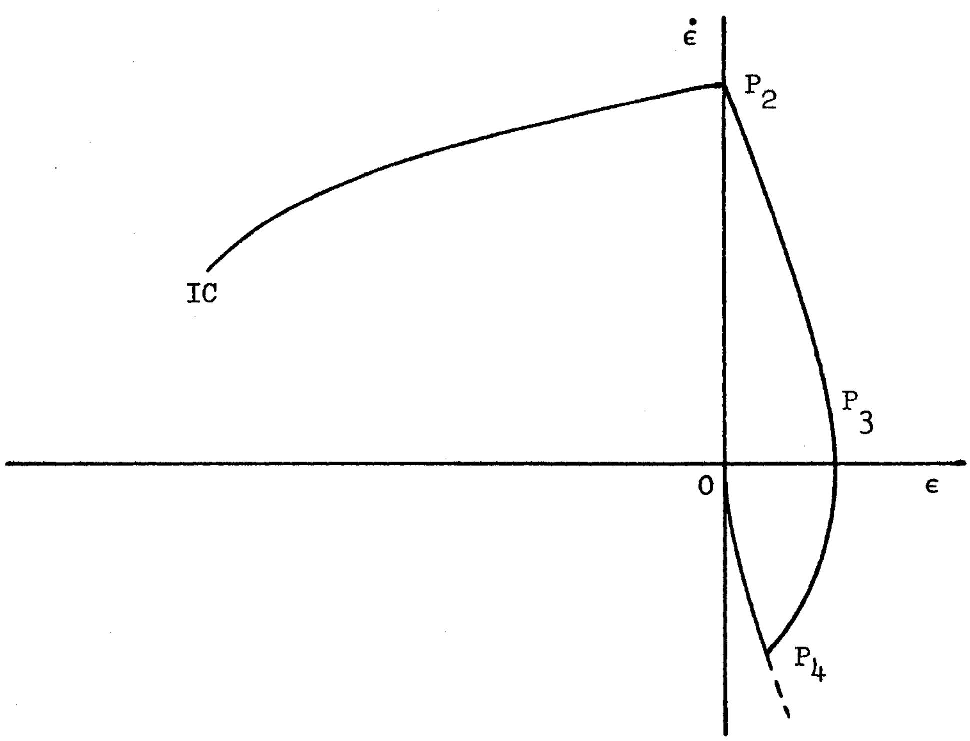

FIG. II-3b IC IN SECOND QUADRANT

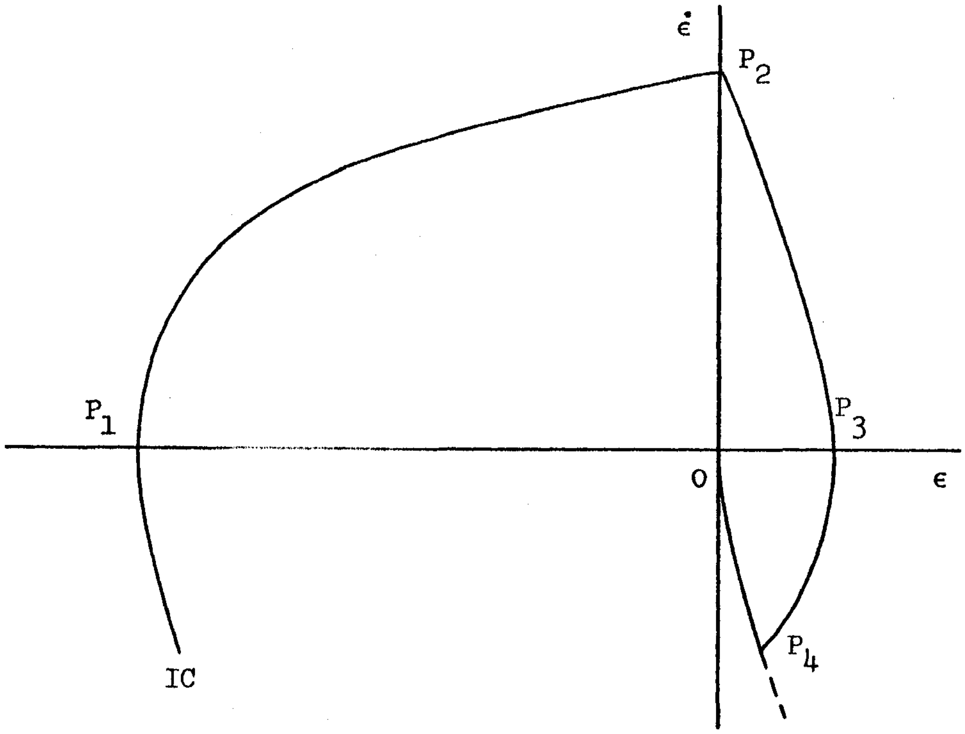

FIG. II-3c IC IN THIRD QUADRANT

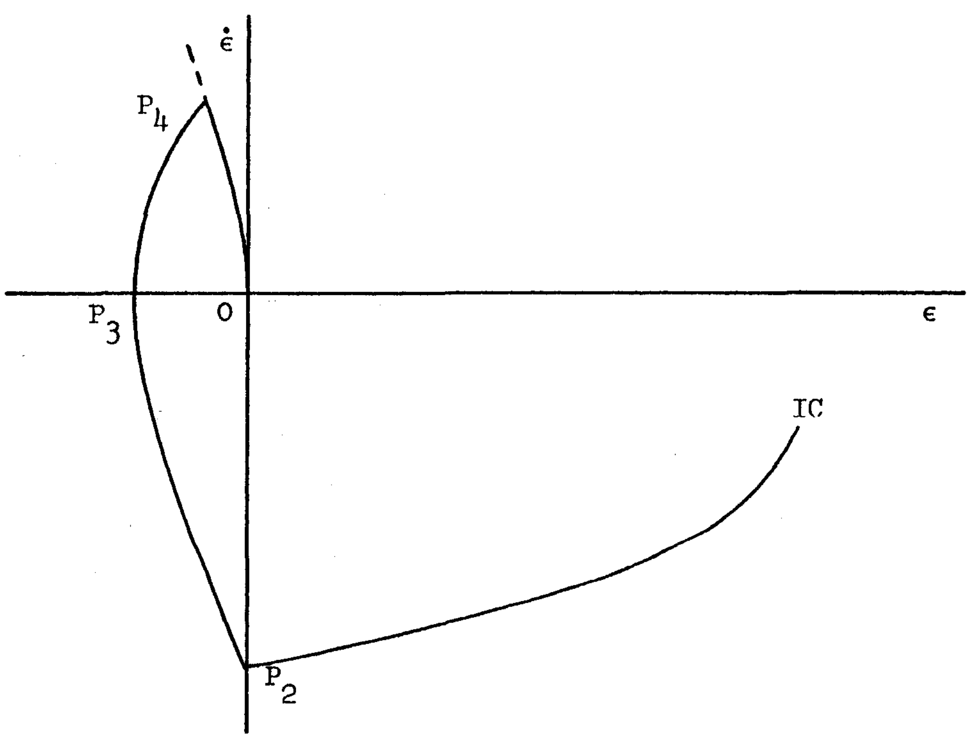

FIG. II-3d IC IN FOURTH QUADRANT

implemented by setting an index, K, on switching and not filling in the table if $K > 1$. The index K is increased by unity after each switching and is varied throughout the controller execution as will be described.

The table fill-in process will be halted for $\Delta\epsilon_r = 0$ and at this time $K + 1 \longrightarrow K$ will take account of this fact.

It is to be noted, however, that switching should occur (at P_4) after index $K > 1$ at the compare command after switching on sgn (ϵ) for an initially unfilled table in memory. In fact, $K = 3$ here. In order to not compare again, the condition $K = 3$ is set to override the compare command. The various values of K corresponding to the P_i on Fig. II-3a are given in Table II-1.

Table II-1

Position in phase plane	Index K
IC $\longrightarrow$ P_2	$K = 0$
P_2	$K = 1$
$P_2 \longrightarrow P_3$	$K = 1$
P_3	$K = 2$
$P_3 \longrightarrow P_4$	$K = 2$
P_4	$K = 3$
$P_4 \longrightarrow$ Origin	$K = 3$

It has been noted that switching on sgn (ϵ) is undesirable for $K > 0$. This may be explained by reference to Fig. II-4.

Here the system has switched late on a previous table after some change in system parameters. The negative torque trajectory follows the new parameter response. If switching on sgn (ϵ) were now allowed, the system would travel off in the third quadrant as shown.

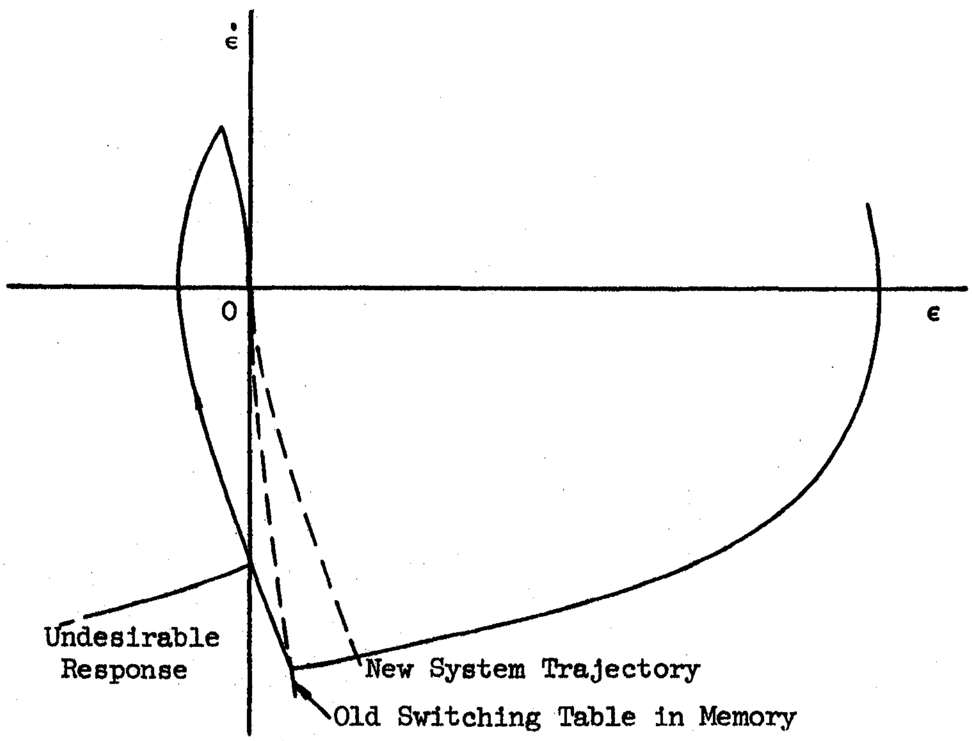

FIG. II-4 LATE SWITCHING AND POSSIBLE UNDESIRABLE RESPONSE

Hence an override must be provided so the system may proceed and switch in the second quadrant on the new optimum line in memory. Hence, the system may switch on sgn (ϵ) only if K = 0.

It is now possible to show how the system described is adaptive as well as optimum.

Since the memory will be refilled each time K = 1 the system always has a new reference, generated by itself, to compare with for optimum switching. Changes in system parameters will yield new trajectories but the system will be able to discern these changes as a new switching table. The first new response will exhibit one overshoot before switching optimally, and the next response will switch optimally, provided the table is large enough in its locations, $\dot{\epsilon}_m$. That is, if the new table is not filled for all $\dot{\epsilon}_m$ the system will adapt only up to the point of largest $\dot{\epsilon}_m$.

Another possible response on a change of system parameters is to switch early. This phenomenon in depicted in Fig. II-5, with the accompanying remedy.

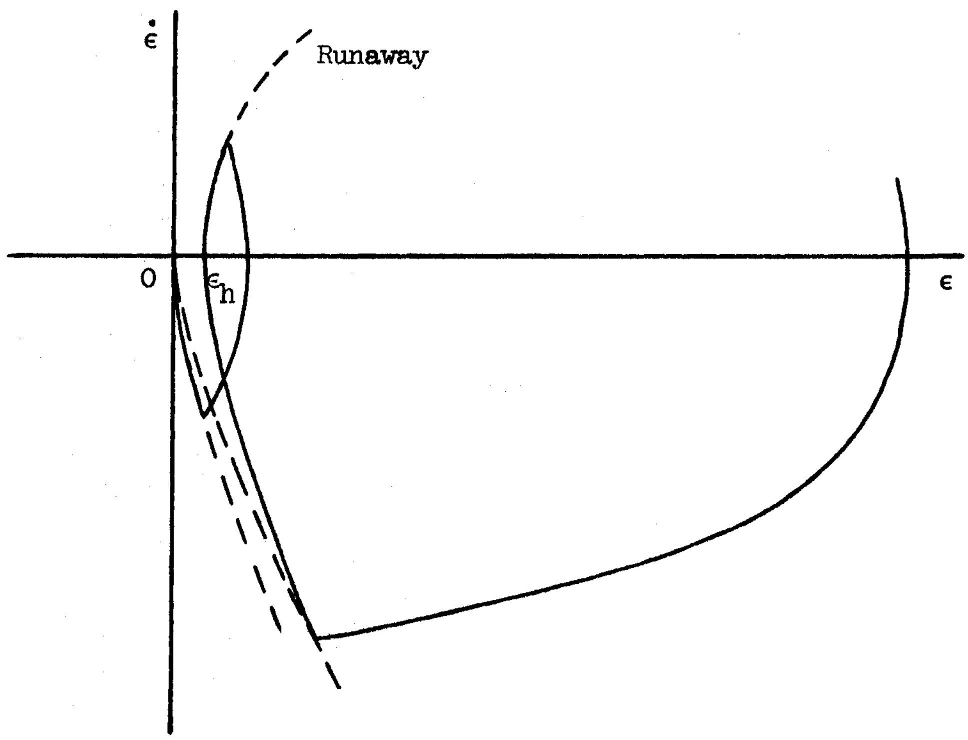

FIG. II-5 RESULT OF EARLY SWITCHING

In this case, if ϵ_f is held in a register for reference and if $\epsilon_2 > \epsilon_h$ ($\epsilon_h = |\epsilon_f|$) at some point in the response the system should switch again. To make this approach valid for negative-error portions of the phase-plane the condition $|\epsilon_2| > \epsilon_h$ is imposed. Moreover, to prevent filling in a table again or avoid the compare override (K = 3) K is set equal to 1. Since it is most convenient for DCC programming purposes to compare $|\epsilon_2|$ and ϵ_h after receipt of ϵ_2, an initial ϵ_h must be set up in the DCC. This may be an arbitrary value, larger than any expected $|\epsilon_r|$. Otherwise, a zero initial ϵ_h compared with any response error will cause a switch.

It is possible that there will be no value of $\epsilon_m(\dot{\epsilon}_m)$ corresponding to $\epsilon_r(\dot{\epsilon}_r)$, that is, this memory location will be empty. On a compare command the system will respond as if the table were blank and not switch optimally. Hence, some means must be provided to present a value of $\epsilon_m(\dot{\epsilon}_m)$ for comparison. Since the table is filled in decreasing values of $|\dot{\epsilon}_m|$ and ϵ_m the next location $|\dot{\epsilon}_{m-1}|$ may be filled with ϵ_m also. If the position $|\dot{\epsilon}_{m-1}|$ is filled on the next sample period then the old $|\dot{\epsilon}_{m-1}|$ will be replaced by a fresh correct value. In the event there is no new value filled in the table, the system will at worst switch early at this position. Perhaps more than one location might have to be filled in this manner. It is easiest to discover the table gaps by system simulation as in section IV, where it was found for this particular system and sampling time only one memory location at most was skipped.

A final consideration for logic design in the DCC is the initial switching of the relay. This is readily accomplished by checking the sign of the initial error and giving the appropriate switching signal.

The complete DCC logic has been described. The next section will consider DCC requirements to implement the logic described in this section.

III. DIGITAL COMPUTER CONTROLLER REQUIREMENTS

The overall system controller operation is given by the block diagram of Fig. III-1. The DCC samples error every T seconds, operates

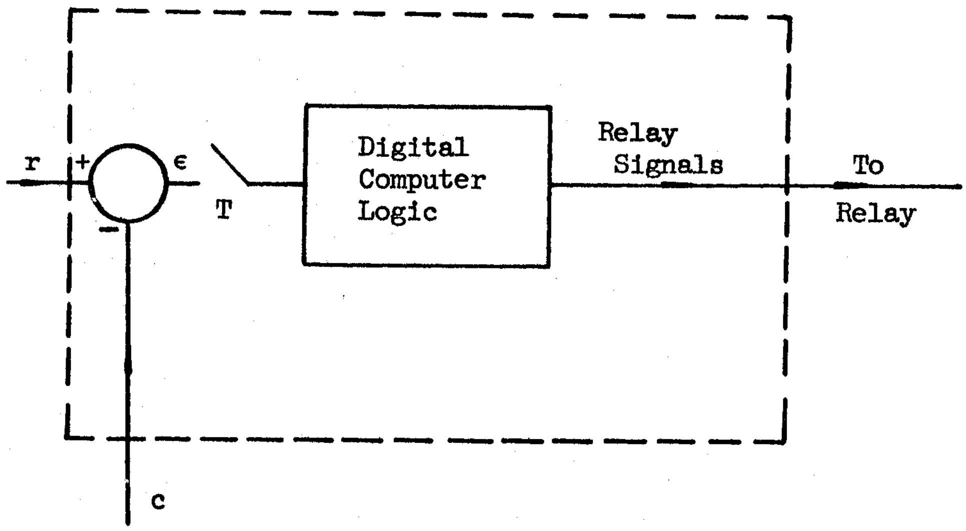

FIG. III-1 OVERALL DIAGRAM OF DCC

on this error, and signals the relay device to switch at the appropriate place in the phase plane.

1. Logic Flow Diagram.

A logic flow diagram is now considered to implement the control strategy developed in section II. A complete flow diagram is given in Fig. III-2.

Several "IS" comparison blocks are shown. For the comparisons of the form

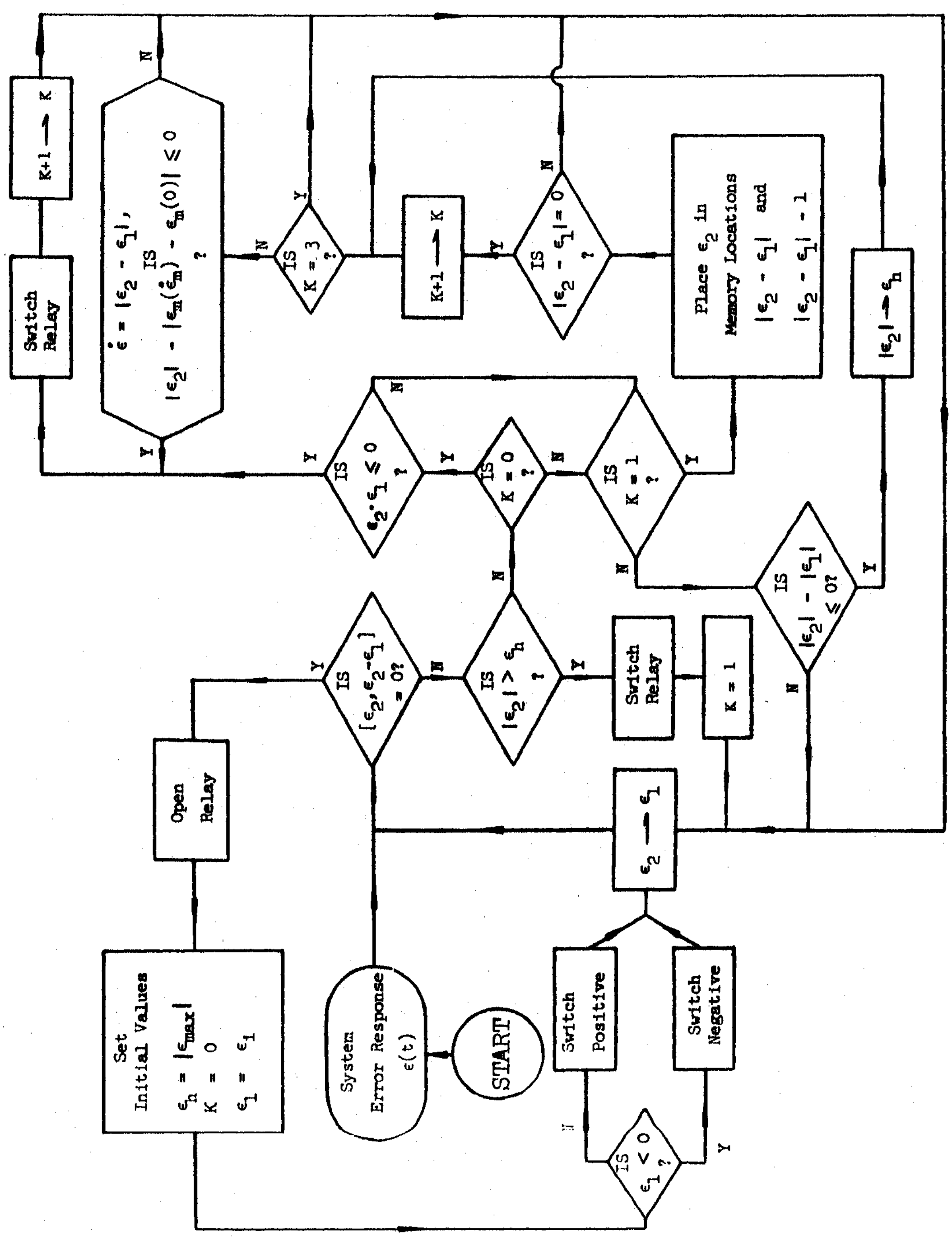

FIG. III-2 DCC LOGIC FLOW DIAGRAM

$$\text{IS} \quad (A - B) \leqslant 0 \quad ?$$

it is possible to write

$$\text{IS} \quad (B - A) \geqslant 0 \quad ?$$

This is an alternate procedure and may be used in a DCC where 0 is treated as a positive number.

Equation (II-9) may also be modified slightly for computer utilization if desired. Since

$$\epsilon_f = \epsilon_m(0)$$

the choice exists as to whether this value should be taken from memory or a register. For memories with slow access time it will be best to to place this value in a register. However, the flow diagram indicates ϵ_f as $\epsilon_m(0)$.

2. Consideration of Computer Speed.

The sample time, T, may now be taken into account. Since the present sampled error, ϵ_2, is given by a digital encoder, it is desirable to have a new error sampled only after the computer has gone through its longest logic sequence. "Longest" refers to real time, and hence the actual minimum sample time T is the longest logic sequence time in the computer, T_s. Hence, most accurate results occur if

$$T = T_s \, .$$

The type of memory and its access time is quite important in obtaining minimum T_s. A delay line memory will take at most one cycle time to reach a particular position in memory. A much improved memory would be one with immediate access.

A special purpose DCC is being built by R. Shiner to implement the logic of this thesis. The computer has a delay line memory with cycle time of 5 msec. The simulation in section IV has assumed a sampling time of 1 msec. to achieve most accurate results so as not to obscure the merits of the method. When T_s for the particular computer has been calculated the simulated sampling time should be adjusted accordingly.

The simulation also indicates the accuracy of the final values of $(\epsilon, \dot{\epsilon})$ and will help place a tolerance in the computer logic to open the relay.

The number of hold registers necessary in the computer are also indicated by the logic. It is seen that ϵ_1, ϵ_h, K, and 3 must be registered for use in the course of the programme. Ultimately a register for ϵ_2 and other values in the system might be required depending on the implementation.

3. Numbers and Coding in the Digital Computer Controller.

The actual DCC being built will use integer numbers only. Hence, the memory is addressed as integral values. The present computer has 60 locations so the absolute error rate limit is (0, 60). Error rate is measured as $\Delta\epsilon_r$ from a digital encoder whose range is (0, 1023). It is left to determine the actual addressing of $\Delta\epsilon$ in memory as a location using such a code. This may be done using this code in the simultation. For example, if $\epsilon_2 = 1010$ and $\epsilon_1 = 980$, then $\Delta\epsilon = 30$. This is not necessarily $\dot{\epsilon} = 30$ and memory location 30 should not be addressed. Instead, some scale factor should be employed.

IV. SYSTEM SIMULATION

The system described in this thesis has been simulated on a digital computer to obtain an indication of expected responses and to provide a simple means for further studies without using the actual system. Fig. IV-1 gives a block diagram of the overall system being

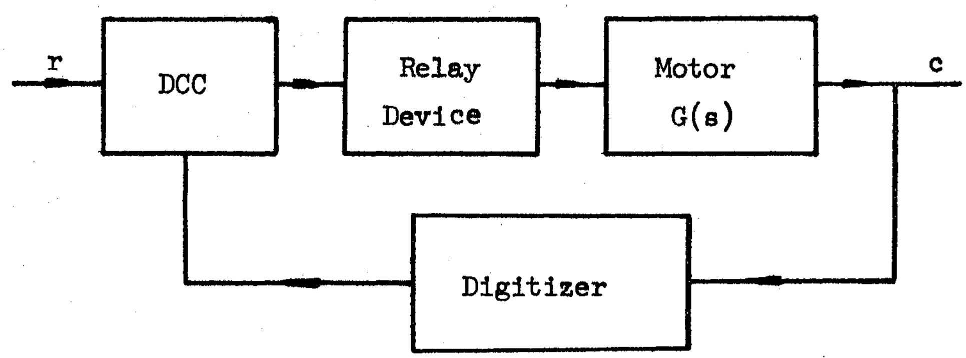

FIG. IV-1 SYSTEM UNDER SIMULATION

simulated.

In the simulation the relay was assumed to be an ideal device with states (1,-1). Some discussion on non-ideal relays and dual-mode servo operation is given in section V.

1. The Equations of Error Response.

The actual transfer function of the motor under consideration is of the form

$$G(s) = \frac{K'}{Js^2 + Ds} \qquad (IV - 1)$$

where K' is the system gain constant, J is the system moment of inertia,

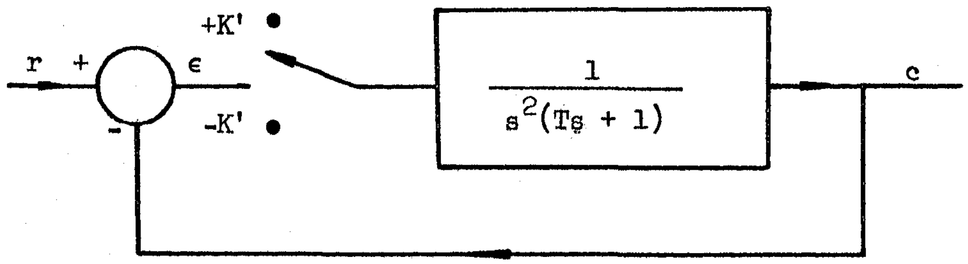

FIG. IV-2 SECOND ORDER SYSTEM YIELDING ERROR RESPONSE OF EQUATION IV-2

and D is the viscous damping of the system. No units are assigned to these parameters for convenience. For some particular system, units may be assigned to obtain responses to compare with actual responses.

For a relay system of the form in Fig. IV-2 Hopkin and Wang[4] give an error response of the following form (T is the system time constant):

$$\epsilon(t) = \epsilon(0) + \dot{r}(0)t + \ddot{r}(0)\frac{t^2}{2} \mp K't - T[\mp K' + \dot{r}(0) - \dot{\epsilon}(0)]\,(1 - e^{-t/T}) \qquad (\text{IV - 2})$$

Moreover, the system will be limited to step and ramp changes of error and it is assumed the reference is unchanged. Hence, $r(0) = \dot{r}(0) = \ddot{r}(0) = 0$, and equation (IV-2) can be written in terms of the transfer function of equation (IV-1) as

$$\epsilon(t) = \epsilon(0) \mp \frac{K'}{D}t - \frac{J}{D}[\mp\frac{K'}{D} - \dot{\epsilon}(0)](1 - e^{-\frac{D}{J}t}) \qquad (\text{IV - 3})$$

which is the response optimized here.

2. Theoretical Error Responses.

Responses of the following four types were obtained with the various initial conditions imposed to check for optimization and adaptation to parameter changes.

(a) Application of Various Step Error Changes

Step error initial conditions were applied to the system in the following sequence;

$\epsilon(0) = 3{\cdot}0,\ 2{\cdot}7,\ 1{\cdot}4,\ 2{\cdot}3,\ 3{\cdot}2,\ 3{\cdot}2,\ 1{\cdot}0.$

Time responses in the sequence of applied initial errors are given in Fig IV-3. The system parameters were not changed.

The responses indicate that the system is optimized for initial errors $\leqslant$ a previous initial error (assuming no parameter change). Moreover, the system optimizes after the first application of this type of error. If a new initial error is larger than a previous initial error imposed, the system response will first be sub-optimal (e.g. response (1)) and exhibit one overshoot, then optimal for errors $\leqslant$ this initial error (e.g. responses (2), (3), and (4)). This phenomenon is due to the fact that the switching table was not filled in to accomodate large $\epsilon_r(\dot{\epsilon}_r)$ and was empty to this response.

(b) Optimum Switching to Ramp Functions

Two similar ramp error changes, $\dot{\epsilon}(0) = 40$, $\epsilon(0) = 0$, were applied to the system for two consecutive responses. No parameter changes were allowed. These responses are given in Fig. IV-4.

From equation (IV-3) it may be seen that the phase plane trajectories will be distorted as well as shifted along the ϵ-axis for ramp error disturbances. Hence, unless the next application of ramp error were similar to the previous one, the process depicted in Fig. IV-4 would be repeated. This deficiency can be overcome at the expense of increased DCC memory by a three-dimensional table of $\epsilon_m(\Delta\epsilon_m, \dot{\epsilon}(0))$.

(c) Similar Initial Step Applications, Reduction of System Inertia

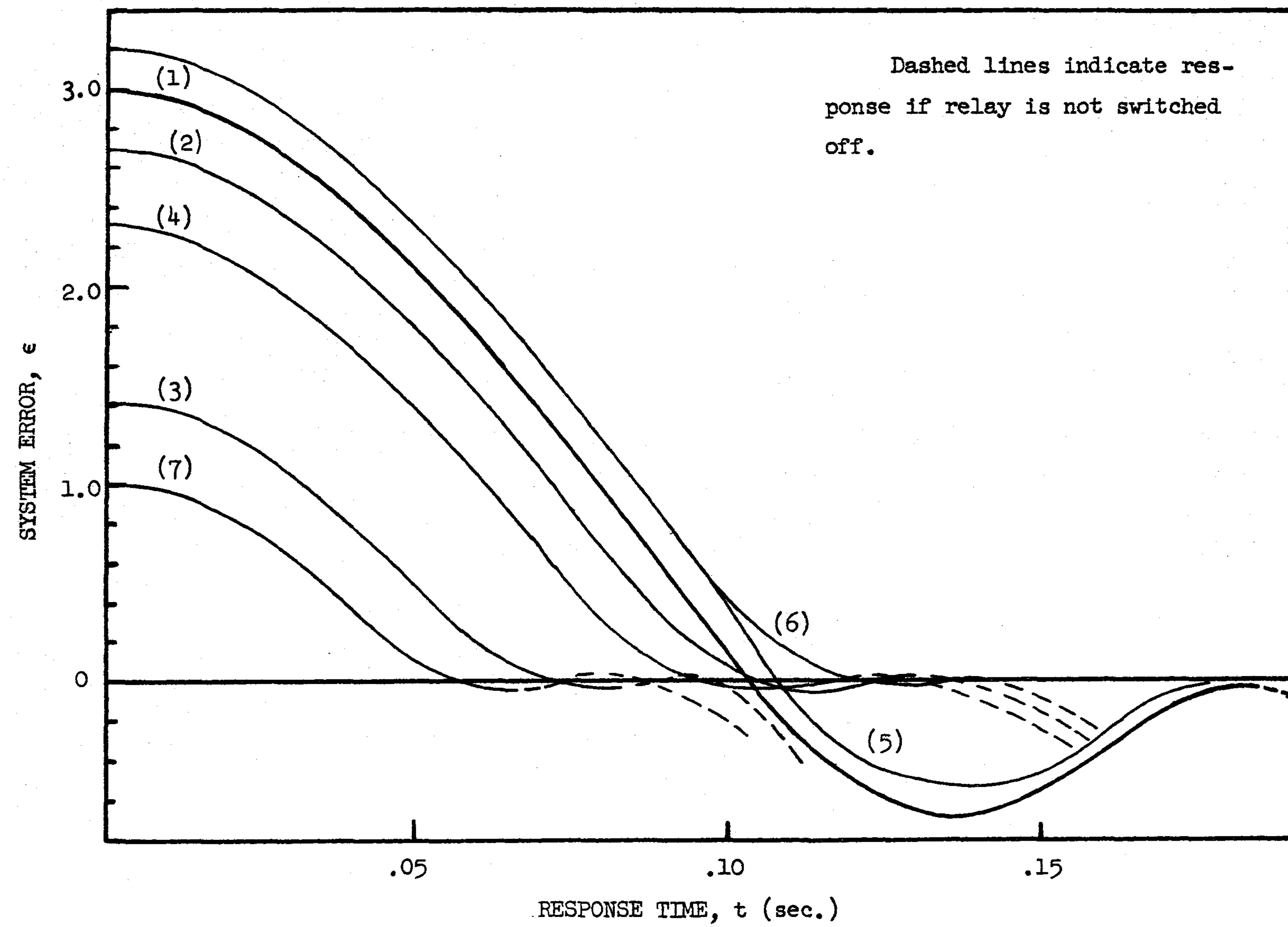

FIG. IV-3 ERROR RESPONSES FOR VARIOUS STEP INITIAL ERRORS

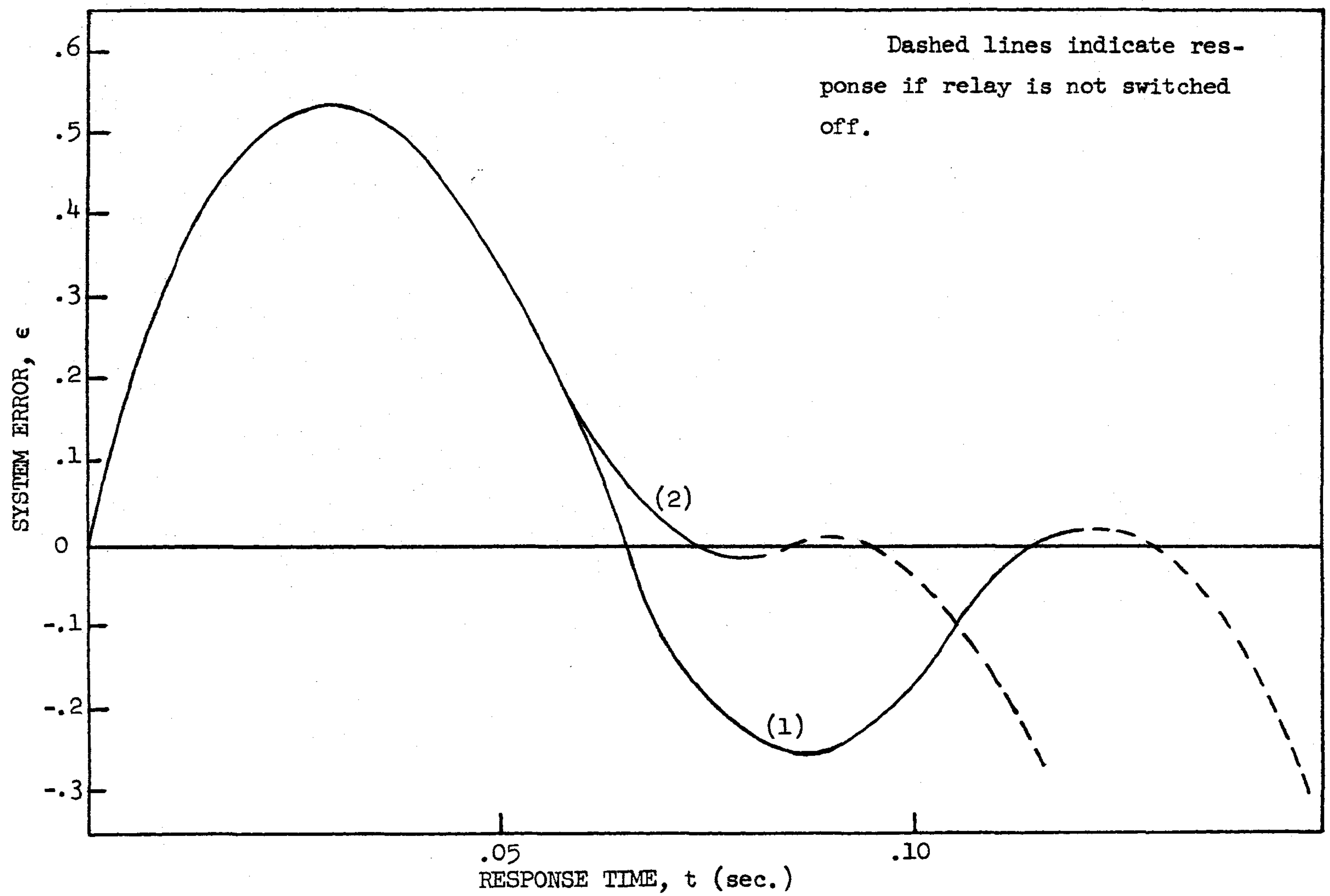

FIG. IV-4 ERROR RESPONSES FOR TWO SIMILAR INITIAL RAMP ERRORS

In this response test, the system inertia was changed after the first response is allowed to settle and two additional similar initial errors were applied. Here, the new system inertia will cause an early switch and a tendency toward system runaway. The system responses are given in Fig. IV-5 for the following initial conditions and parameters.

	$\epsilon(0)$	$\dot{\epsilon}(0)$	K'	J	D
Run 1	3.2	0.0	10.0	0.01	0.20
Run 2	3.2	0.0	10.0	0.006	0.20
Run 3	3.2	0.0	10.0	0.006	0.20

In Fig. IV-6 a phase plane representation of response (2) is given to show the effect of switching after a change of inertia ($J_{new} < J_{old}$).

In Fig. IV-6 the system switches at P_1 on the old optimum trajectory which is an early switch for the new system. At P_2 the fact of an early switch has been recognized and another switch takes place. However, the new system trajectory has been filled in memory starting at P_1, and at P_3 the system will optimally switch. If no new parameter change is effected, the system will switch optimally on the next application of an initial error ϵ such that $\epsilon \lessgtr \epsilon_1$.

(d) Responses for Initial Negative Step Error Changes, Same Inertia Change as in (c)

This final test is given to demonstrate response to negative initial conditions. The results were mirror images of those in Fig. IV-5 and are not given here.

In all the responses, a-d, it was noted that the maximum origin error was approximately 5 % of the initial error. It can thus

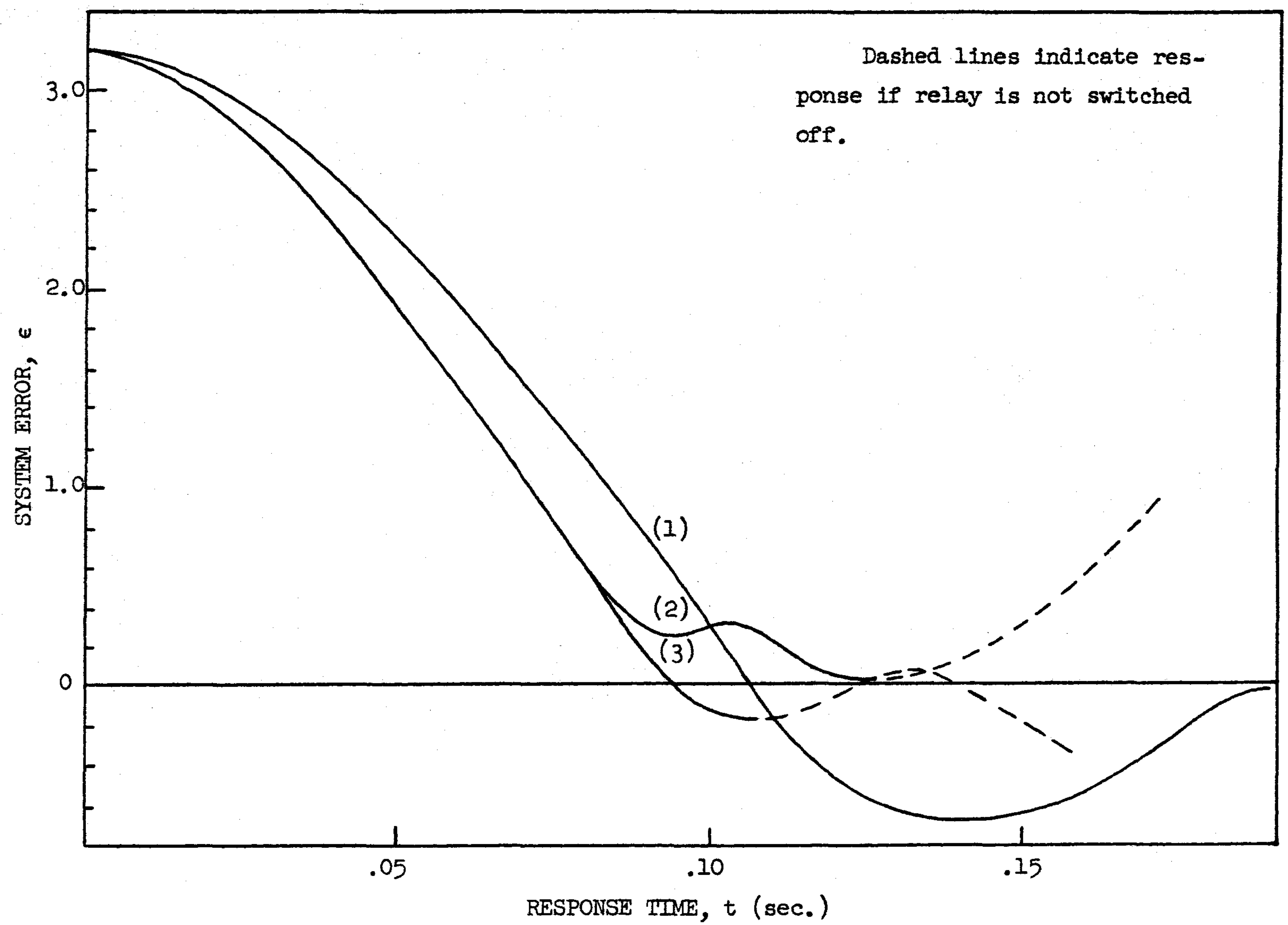

FIG. IV-5 ERROR RESPONSES FOR A REDUCTION OF SYSTEM INERTIA

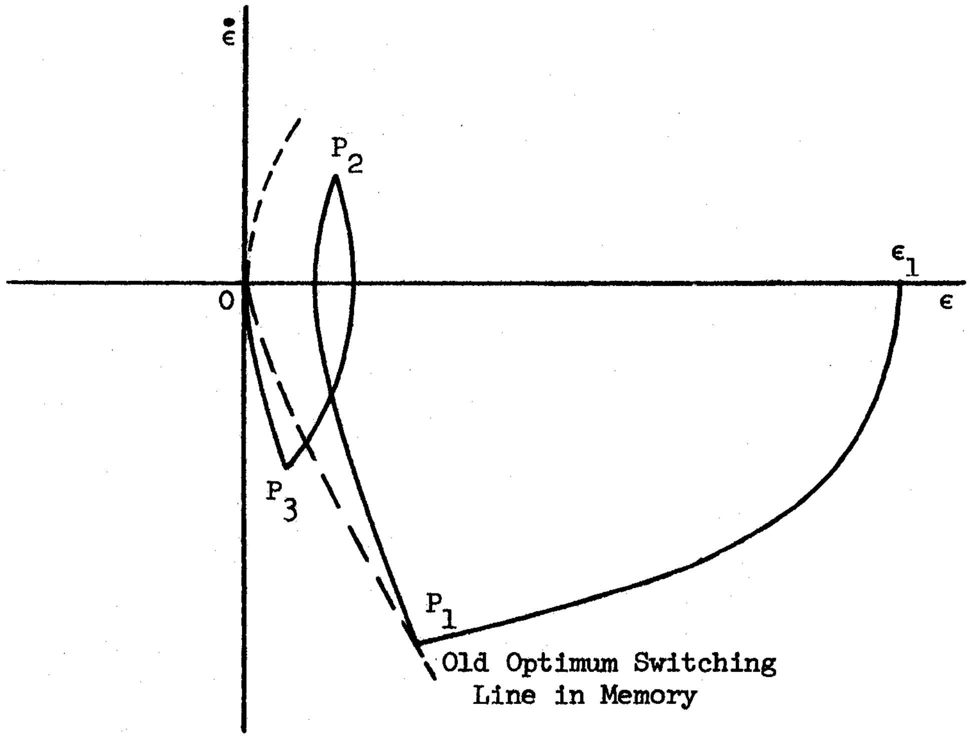

FIG. IV-6 PHASE PLANE REPRESENTATION OF FIG. IV-5

be said the responses are optimum within 5 %. These errors are due to digital measurements which takes only a finite sampling of the responses. For smaller sampling times, responses would be recognized more accurately.

There are several possible initial conditions other than those shown in a-d that might be imposed on the system. However, the responses can be predicted from the above responses as the DCC programme is general for any initial conditions of the type ($\epsilon(0)$, $\dot{\epsilon}(0)$).

V. SOME PRACTICAL CONSIDERATIONS

For the system simulated herein an ideal switching device (relay) with states (1,-1) has been assumed. Also, the relay was assumed to switch instantaneously on a control signal.

The simulated DCC acted fast enough to perform all its required logic between small sampling times but had no knowledge of response between sampling times.

1. Relay Characteristics.

In the actual system to be constructed relay characteristics will play an important role. Most relays will have the characteristic shown in Fig. V-1. The deadband, D, present represents a small amount of signal that must be overcome before the relay acts (pull-in or drop-out signal). Hence the control signal must be at least $\geqslant D/2$ to ensure proper relay switching.

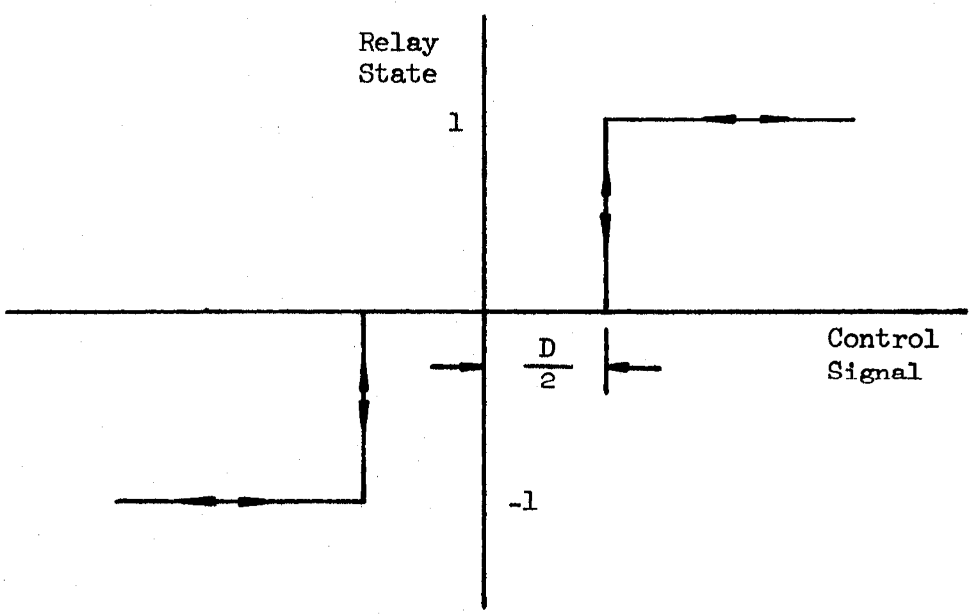

FIG. V-1 RELAY CHARACTERISTIC

It must also be decided what bounds must be placed on the origin error so that it is effectively zero, requiring an open relay. In digital computation techniques exact zero values are impractical for consideration. As the relay is under complete control of the DCC some tolerance must be built into its appropriate computation stage to open the relay. To prevent opening the relay and leaving the system at a finite point (ϵ, $\dot{\epsilon}$) in the trajectory the system could be operated as a "dual mode" system. In this scheme, the system is operated in a linear manner for some selected small error.

Also, compensation for the time required for relay switching must be made. If the relay takes τ seconds to switch over on receiving a control signal then the relay must be switched τ seconds earlier than its calculated point. This prediction is impossible to make in time so a compromise must be made on a wide range of phase plane responses. In Fig. V-2 an optimum trajectory is shown with the effect of switching late due to relay lag time τ. Ideally the relay is commanded to switch on ϵ_1. However, due to relay lag time the system switches at ϵ_2, τ seconds later. It is known however that

$$\tau_{12} = \int_{\epsilon_1}^{\epsilon_2} \frac{d\epsilon}{\dot{\epsilon}} \qquad \text{on } C_1$$

and hence $\Delta\epsilon = \epsilon_2 - \epsilon_1$ may be calculated. The system should then be switched if the error is within $\Delta\epsilon$ of the optimum curve.

2. Sampling Time.

As mentioned previously, sampling time is determined by the computation speed of the DCC. Hence, systems which may be optimized by this method must also be slow enough in their response so as to allow

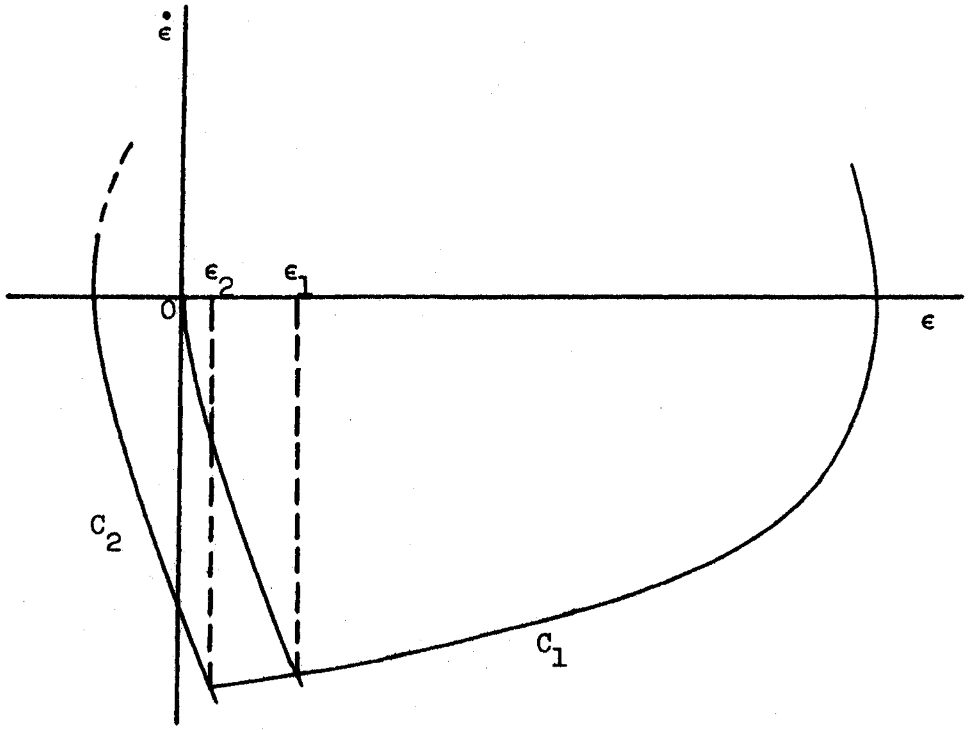

FIG. V-2 ILLUSTRATION OF RELAY-LAG RESPONSE

many sampling periods between a total response.

Since the DCC is sampling error between finite times, T, no recognition of inter-sampling time error is made. It will be assumed that the error exhibits no radical responses between sampling points.

VI. CONCLUSIONS

The method of optimization and adaptation of a phase plane representable control system by means of comparing actual error trajectories with a self-stored optimum switching line in a DCC has been demonstrated to be a useful contribution to control system development. The method is direct, requires no elaborate calculations, and does not require an actual measure of error rate. Moreover, the method has been shown by simulation to be easily implemented on a control computer for actual use.

The technique of self-storing of optimum system trajectories by addressing memory with error difference for both optimization and adaptation purposes is believed to be novel in the field.

In the future it is hoped that further studies will be performed on an actual system to provide further evaluation of the method's usefulness and functioning for disturbances of the type considered here and for random disturbances.

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VITA AUCTORIS

1940	Born on August 8, in Windsor, Ontario.
1954	Completed elementary education at Central Public School, Windsor, Ontario.
1959	Completed Grade XIII at Assumption High School, Windsor, Ontario.
1963	Graduated from Assumption University, Windsor, Ontario, with degree of B.A.Sc. in Electrical Engineering.
1964	Candidate for degree of M.A.Sc. in Electrical Engineering at the University of Windsor.