1-1-1971

A graphics terminal for a digital computer.

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A GRAPHICS TERMINAL FOR A DIGITAL COMPUTER

by

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A Thesis

Submitted to the Faculty of Graduate Studies through the Department of Electrical Engineering in Partial Fulfillment of the Requirement for the Degree of Master of Applied Science at the University of Windsor

Windsor, Ontario
1971

Approved

347115

ABSTRACT

This thesis describes the logical design and implementation of a dot generator and intensity circuit for a computer graphics terminal. Also a proposal for a vector generator is given as implementation was not successfully carried out.

Basically the dot generator allows one to draw dotted lines of various lengths at various angles on a cathode ray tube. The dots are generated by using an up/down counter in conjunction with a digital to analog converter for the vertical and horizontal deflection of the beam. Unblanking pulses are then applied to the Z-axis to intensify the dots.

The intensity circuit provides four possible intensities , dim, normal, bright or blanked. When the dot, alphanumeric or vector generators are being used, any of the four possible intensities can be chosen. In the alphanumeric mode three additional intensity levels are automatically selected for the user, to compensate for the variation in intensity which occurs when either the large, normal or small size characters are being generated.

The proposed vector generator is essentially two integrators; one for the vertical and one for the horizontal deflection. During one integration time a line of any length and at any angle could be drawn. This, unlike most systems, has the advantage that a vector the full length of the screen could be drawn in one integration time.

ACKNOWLEDGEMENTS

The author wishes to express his appreciation to Dr. P.A.V. Thomas for his supervision and suggestions. Acknowledgement must also go to the National Research Council of Canada for their financial support.

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CHAPTER I

INTRODUCTION

1.1 Desirability of a Cathode Ray Tube Display

With the broadening use of high speed computers, a need has arisen for a fast and flexible means of outputting information from the computer.[12] As a result many good alphanumeric generators[11] which output data on a cathode ray tube (CRT) at a high rate of speed have been developed and are being successfully used when a hard copy of the text output from the computer is not required. The alphanumeric generator is limited, however, by the fact that it can only produce alphanumeric text, and thus it does not fill the needs of many of today's computer users.

A terminal which is much more in demand is a graphics terminal which has alphanumeric text producing facilities. Such a terminal allows the user to view a graphic display on a CRT and allows him to interact directly with the computer via light buttons, physical switches or a light pen. This type of terminal is of great interest to the time-shared computer users for it gives each user the illusion of being the sole user of the machine and at the same time permits him to direct or modify the computation process from a remote terminal.[13] A graphics terminal is also of great use in the fields of computer aided design, computer aided instruction, data analysis and process control, because it provides for simple man-machine interaction.

As a teaching aid, computer graphics terminals are ideal. A teacher can program a series of problems into a computer and have them displayed on a graphics terminal where a student can attempt to solve them.

This has the advantage of allowing each student to work at his or her own speed and at the same time frees the teacher to assist the slower students.

In the field of computer aided design, such a terminal allows for the quick display of charts and graphs, as well as pictorial diagrams, which are of great value to the design engineer. Again the feature of such a system is the ease by which man-machine interaction can be accomplished. It is through this interaction that design changes can be displayed quickly on a CRT without holding up the engineer or computer, like a conventional line printer or plotter. Thus we see that a graphics terminal is a must for many computer users, and it therefore warrants the time and effort spent in trying to develop a good and economical graphics terminal. An attempt was made to design line generators for a graphics terminal that were more economical than those currently available.

1.2 General Aspects of the Problem

Since research had been carried out in the field of CRT displays in the Electrical Engineering Department at the University of Windsor [1][2] it was decided that work should be done to increase the capabilities of the computer terminal that was being developed. It was felt that the area of this research should be computer graphics, and as a result it was decided that a dot and vector generator, as well as an intensity control circuit, should be designed and implemented.

The dot generator was to be designed so that it could be used in a relative, rather than an absolute mode. That is, when control is transferred to the dot generator, dotted lines could be drawn only from the place where the electron beam had been positioned just previous to the transfer of control. This meant that the beam must be positioned

initially, using the vector generator. This discussion of the dot generator will be continued in the next chapter.

When the project was begun, the intensification of the beam was being achieved by using a Hewlett Packard vacuum tube amplifier which allowed only one intensity for the display. It was felt that this was not flexible enough as it was desirable to have the capability of drawing characters at three different brightness levels, as well as having a blanked mode which would allow for positioning the beam. However, this still did not allow enough flexibility, as in the A/N mode a problem arose when various size characters were drawn, since the A/N generator merely increases or decreases the size of the dot matrix used to generate characters. This naturally led to the problem of inconsistent character intensification as the character size varied. When small letters were drawn, they appeared brighter than the normal size characters, due to the increased packing density of the dots. Similarly, when large letters were drawn, they appeared dull, due to decreased packing density. Thus, compensating intensity levels had to be incorporated into the intensity selection circuits; however, a complete discussion of this will be deferred until Chapter 3.

The third part of the project involved the design and implementation of a vector generator. This generator would give the terminal the capacity of drawing blank, solid or dashed lines of any length and at any angle on the CRT. This would then give the desirable ability to draw graphs, plots or other objects. With the aid of software, this generator could be made to draw circles and sectors. A more comprehensive discussion of the design and success of this section of the project will be given in Chapter 4.

CHAPTER II

The Dot Generator

2.1 Introduction

In order to save core space and to increase the refresh speed of the display, the core circuitry was designed in such a way that once a DOT, A/N orVECTOR instruction is decoded, all the forthcoming output from the core is considered data to the designated generator. This process of outputting data to the specified generator continues until a new instruction is encountered. At this time the generator previously being used is turned off and the core output is directed to the most recently specified generator.

A second factor that had to be considered in the design of the dot generator was the spacing of the dots on the screen. This spacing is determined by the length of the registers used in conjunction with the D/A converters. In this particular case, a 10 bit register was used which allows for $2^{10} = 1024$ distinct positions along each axis. If a 10 inch square screen were used, the raster unit would be $\frac{10}{1024} \approx .01$ inch. Thus when an instruction to increment in the 1's position is given to the dot generator, dots would be placed on the screen in .01 inch increments. Provision was also made so that dots can be placed at every second or every fourth raster position, thus allowing dots to be placed at $\frac{1}{50}$ or $\frac{1}{25}$ inch intervals, respectively, on the screen. Furthermore, provision was made to generate a series of dots in the same direction using the same data word by indicating a number of repetitions.

Figure 1A is an example of a X which is an increment X in the 4's position with a repetition of 1. Thus a single dot is generated which is placed 4 raster units in the positive X direction from the original position of the beam. A single decrement in the Y 1's position is shown in Figure 1B. Here the dot is placed 1 raster unit in the negative Y direction from the original beam position. A combined displacement in the X and Y direction, as well as a repetition of 2, is shown in Figure 1C. In this case the first dot is displaced 2 raster units in the positive X direction and 4 raster units in the positive Y direction from the original beam position. The second dot is placed 2 raster units in the positive X direction and 4 raster units in the positive Y direction from the first dot.

Before an explanation of the circuit is begun, a brief explanation of the word format will be given. Figure 2 shows the bit configuration for both the instruction and the data words. From the diagram it is seen that whenever a code 42xx is encountered, the dot generator is initiated. The last two bits of the instruction word are used for intensity control and will therefore be discussed in the next chapter. The data word contains all the information for controlling the dot generator. Bits 2 through 5 inclusively, contain the number of dot segments to be generated. Bit 6 indicates if the X counter is to be incremented or decremented, and bits 7 and 8 indicate if the count is to take place in the one, two, or four's position. Similarly, bits 9 to 11 contain the required information for the Y counter.

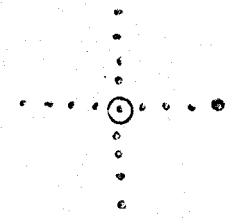


Fig. 1. A
ΔX

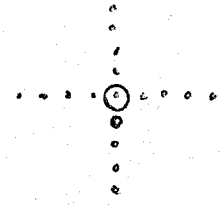


Fig. 1. B
ΔY

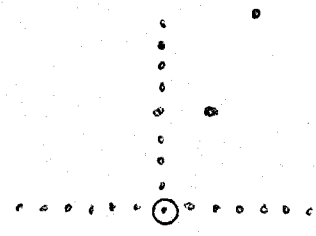
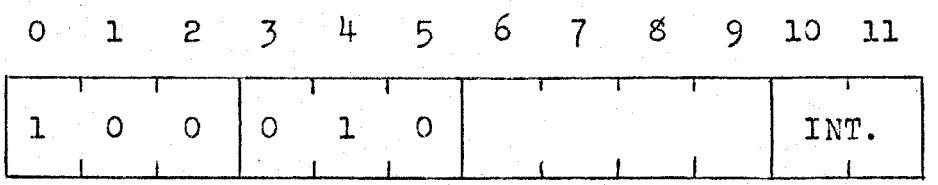


Fig. 1. C
Repeat

Figure 1
Displacement of Dots

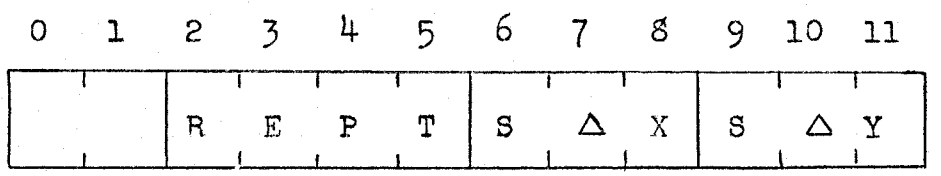
INSTRUCTION WORD

Bit Number



DATA WORD

Bit Number



REPT - 0 to 15 - Number of dots

S - 0; Count up 1; Count down

ΔX; ΔY - 00 - No Count

01 - Count in 1's position

10 - Count in 2's position

11 - Count in 4's position

Figure 2
Instruction and Data Word Configuration

Basically, the dot generator consists of a clock, down counter, (segment counter), decoding gates, an up/down counter and D/A converter[6] as shown in Figure 3. When a dot instruction is encountered, a flag is set up to indicate that the dot generator is to be initiated. Shortly after the flag is set, a "load data" pulse is sent to the generator. At this time the segment counter is loaded with the number of dot segments that are to be generated. Simultaneously with this, the decoding circuitry is loaded with the required information to indicate in what position the up/down counters are to be incremented or decremented. When all the data has been loaded the clock is initiated by the delayed load data pulse, and the production of the dots is begun. The segment counter counts until it reaches zero, and at that time the clock is stopped and a flag is set to indicate that more data is required. The process of loading data and producing dots continues until a new instruction is encountered.

2.2 Implementation

The actual circuit was constructed of Digital Equipment Corporation[3] 'R' series modules, using negative NAND logic, in which "0" volts represents a "false" and "-3" volts represents a "true". However, for the sake of clarity, the operation of the circuit will be explained, using AND/OR logic.

A diagram of the dot generator circuit using AND/OR logic is given in Figure 4. Whenever an instruction word is decoded by the core refresh circuitry, a clear pulse is sent to all the generator control flags. In the case of the dot generator, this same clear pulse is used

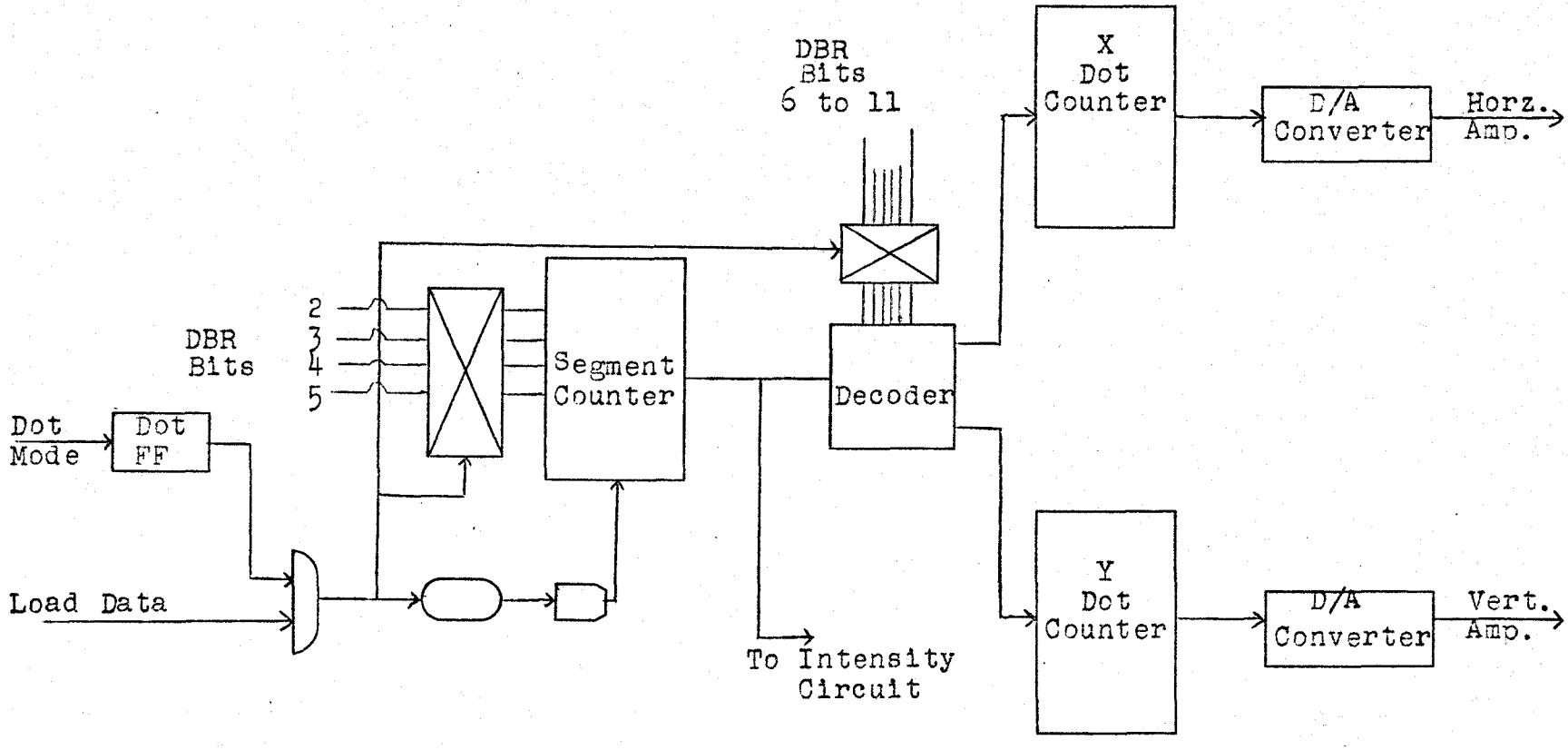


Figure 3
Block Diagram of Dot Generator

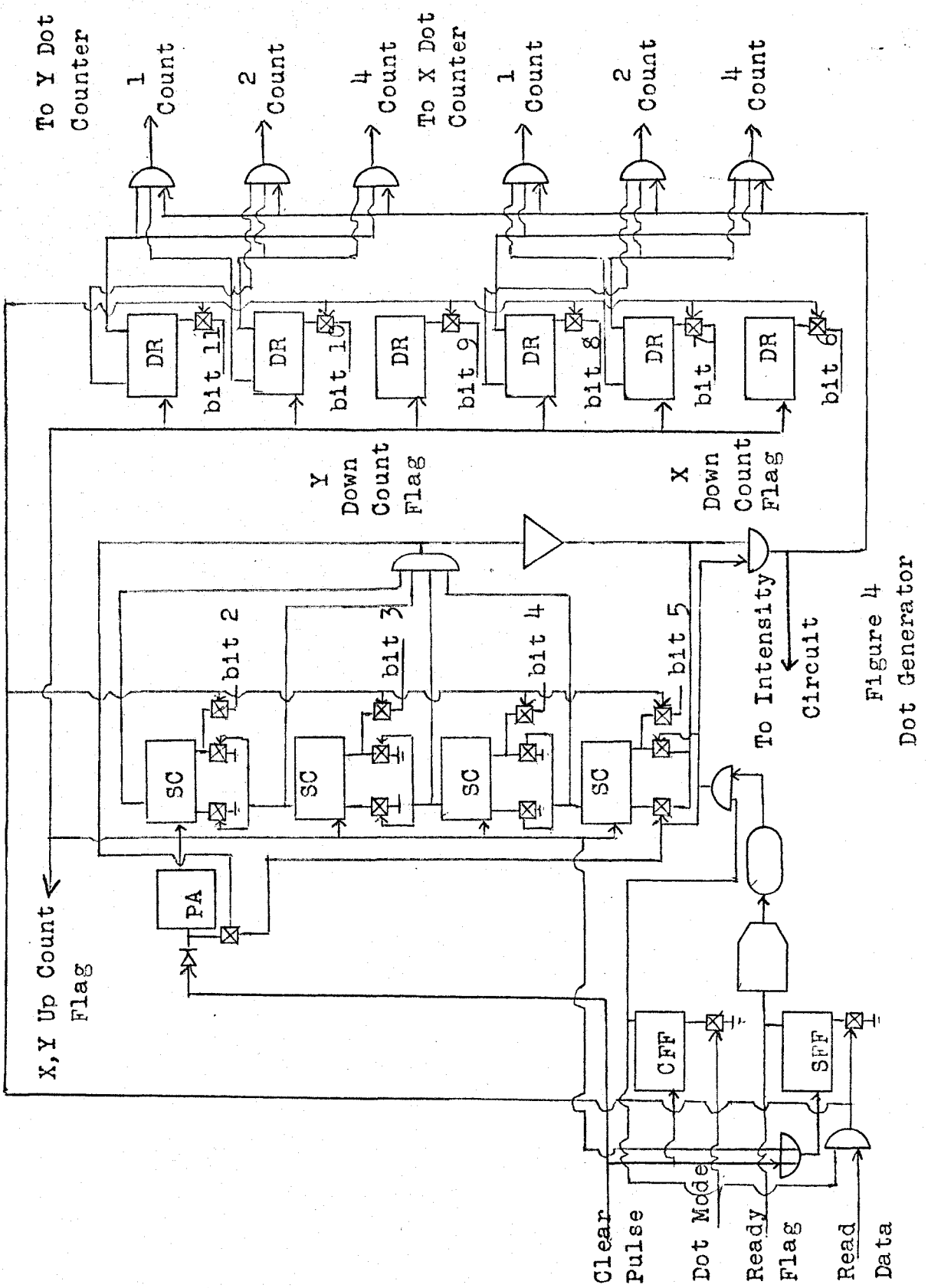


Figure 4
Dot Generator

to clear the decoder buffer register (DR) so that it is ready to receive information if the dot generator has been selected. If it is a dot instruction 1μs after the clear pulse was sent, a 100 ns pulse is sent to the dot control flip flop (CFF) setting it to the 1 state. Approximately 400ns later a read data pulse is sent to the dot generator which loads the required information from the data buffer register (DBR) into the segment counter (SC) and the decoder buffer register (DR). This same pulse also sets the data status flip flop (SFF) to indicate that no more data is required and starts the clock which initiates the segment counter.

The clock output is gated to the decoder which selects the position in which the count is to take place for both the X and Y dot counters. The decoder also indicates the direction in which the count is to take place. The decoding is done by using a series of "AND" gates for which only one in each of the X and Y directions has the proper inputs so as to turn it on.

A 10 bit up/down counter and D/A converter was also needed for the generation of A/N characters; however, in order to save duplicating the circuitry, provision was made so that the dot generator could use the same counters and D/A converters. Thus the output of the decoder is sent to the appropriate position in the A/N up/down counter. It should be noted that this same counter has been denoted as the "dot counter" when used in reference to the dot generator. Simultaneously with the sending of the pulse to the dot counter, intensity pulses are sent to the intensity circuit which produce the unblanking pulses

which are required to generate dots on the CRT. When the segment counter reaches zero, the clock is disabled and the data status flip-flop (SFF) is cleared to the "0"state, indicating that either more data should be sent to the dot generator, or a new generator should be initiated.

2.3 Results and Conclusions

An equivalent of the above-mentioned circuit using "NAND" logic was implemented and connected to the refresh core. This circuit was tested and performed as expected. A sample of the output from the dot generator is given in Figure 5. Figure 5A is a series of 3 squares. Each side of the outside square was constructed by incrementing or decrementing the counter as required, 15 successive times in the 4's count position. Similarly the inner squares were generated using 15 repetitions in the 2's and 1's count position. Figure 5B is an approximate circle which was drawn with the dot generator, indicating the flexibility of the dot mode. There are also some alphanumeric characters on the diagram to show that both the dot and A/N generators can use the same counters and D/A converters without any conflict. Figure 5C indicates that the dot generator can also produce lines at various angles. Thus it can be concluded that the dot generator has been successfully implemented since it functions as required.

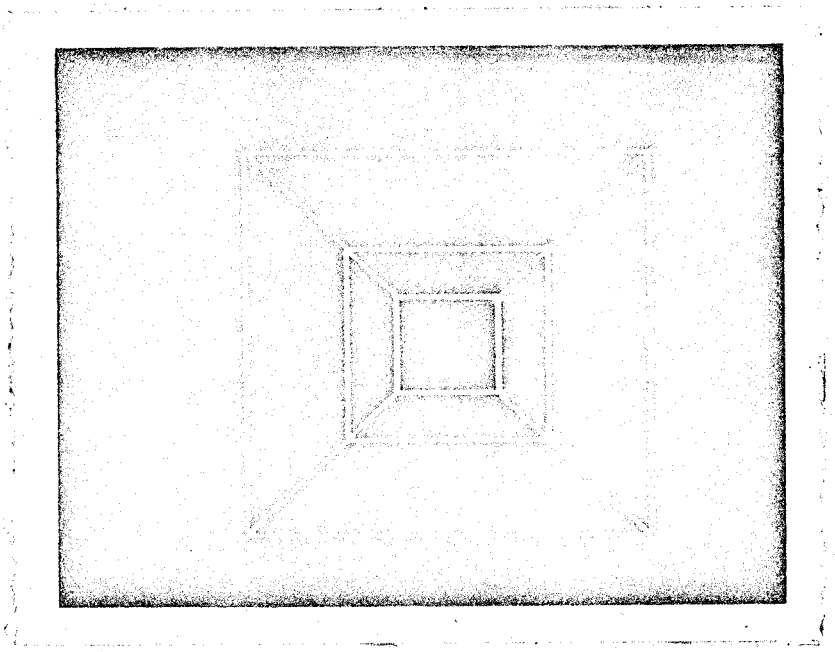


Fig. 5. A
A Grachical Display of Increments in the 1, 2 and 4 count positions

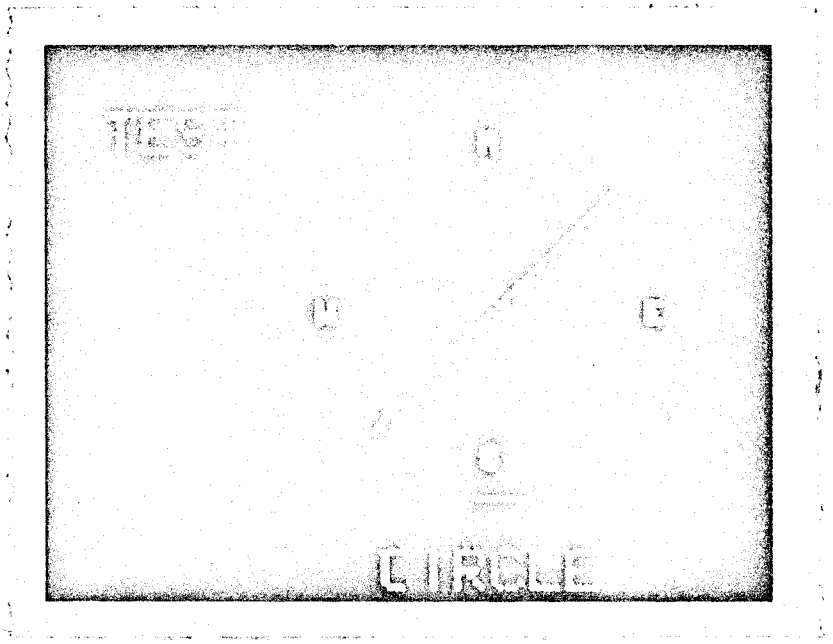


Fig. 5. B
A Graphical Display of an approximation of a Circle

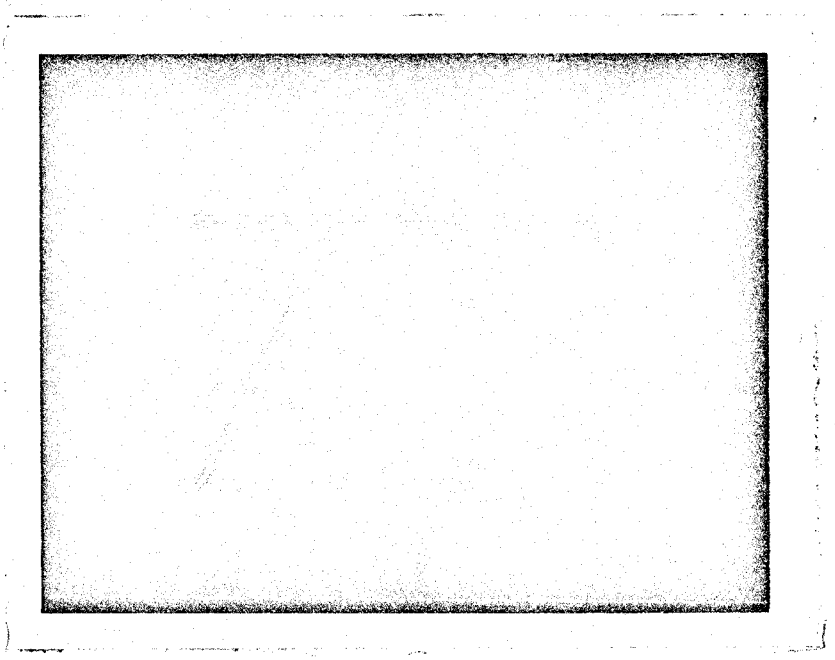


Fig. 5. C
A Graphical Display of Lines at Various Angles

Figure 5
Demonstration of Dot Generator Operation (Photographs)

CHAPTER III

The Intensity Circuit

3.1 Introduction

There are basically two methods of achieving Z-axis modulation on most display tubes. One method is to use pulse width modulation, which allows the brightness of the display to be varied by changing the width of the unblanking pulses while the pulse amplitude is held constant. When using this method, the intensity becomes brighter as the pulse becomes wider. The other method that is commonly used is pulse amplitude modulation. The pulses in this case are a constant width and the intensity is varied by increasing or decreasing the pulse amplitude. As the pulse amplitude increases, the intensity increases.

In the case of the display being built at the University of Windsor, the choice of intensification methods available was limited by the A/N generator. The generator, according to design specification, was to operate at a frequency of 2 megacycles, which means that the repetition period is 500 nanoseconds. However, due to the choice of the D/A converter that was used in the A/N generator, 300 nanocycles are required for the D/A converters to settle to their final values. This allows only 200 nanoseconds for the intensification to take place, thus effectively eliminating the possibility of using pulse width modulation, as this is not time enough to generate 3 distinct intensity levels.

3.2 Intensity Selection

From the specifications given by Tektronex Incorporated, for the oscilloscope being used for the display, it was found that negative pulses between 3 and 50 volts would brighten the beam.[4] In order to obtain three distinct intensity levels for the display, it was required that the

intensity circuit provide unblanking pulses of 3 different levels between 3 and 50 volts. This was achieved by using a voltage divider to select the required unblanking pulse amplitude. Unblanking pulses are then modulated onto this level, and resulting pulses are amplified to the required value.

Figure 6 is a diagram of the circuit used for intensity selection. A -15 volt supply already existed in the PDP-8/S computer so it was used to supply power to the voltage divider. However, the full 15 volts could not be used because the switches used in this circuit were Digital Equipment corporation "A" series electronic switches which were capable of switching a maximum of 10 volts. Thus, a 4.7K dropping resistor and a zener diode were used to provide the 10 volt supply needed to facilitate the switches. Two 5K potentiometers (P1 and P2) were then connected in series with the 4.7K resistor to ground, to complete the voltage divider.

Various potentials between 0 and -10 volts could now be selected from the above mentioned circuit. The full 10 volts was connected to one side of the single pole single throw electronic switch SW1, thus providing the potential required to create maximum beam intensification. The centre taps of potentiometers P1 and P2 were connected to one side of switches SW2 and SW3 respectively. These switches provide for the selection of normal or dim intensities. The second side of the switches are common and provide the output of the intensity selection circuit.

The potentiometers add flexibility to the system by allowing some control over the beam brightness when either the normal or dim intensities have been selected. A second advantage lies in the fact that when a new CRT is added to the terminal the same intensity selection

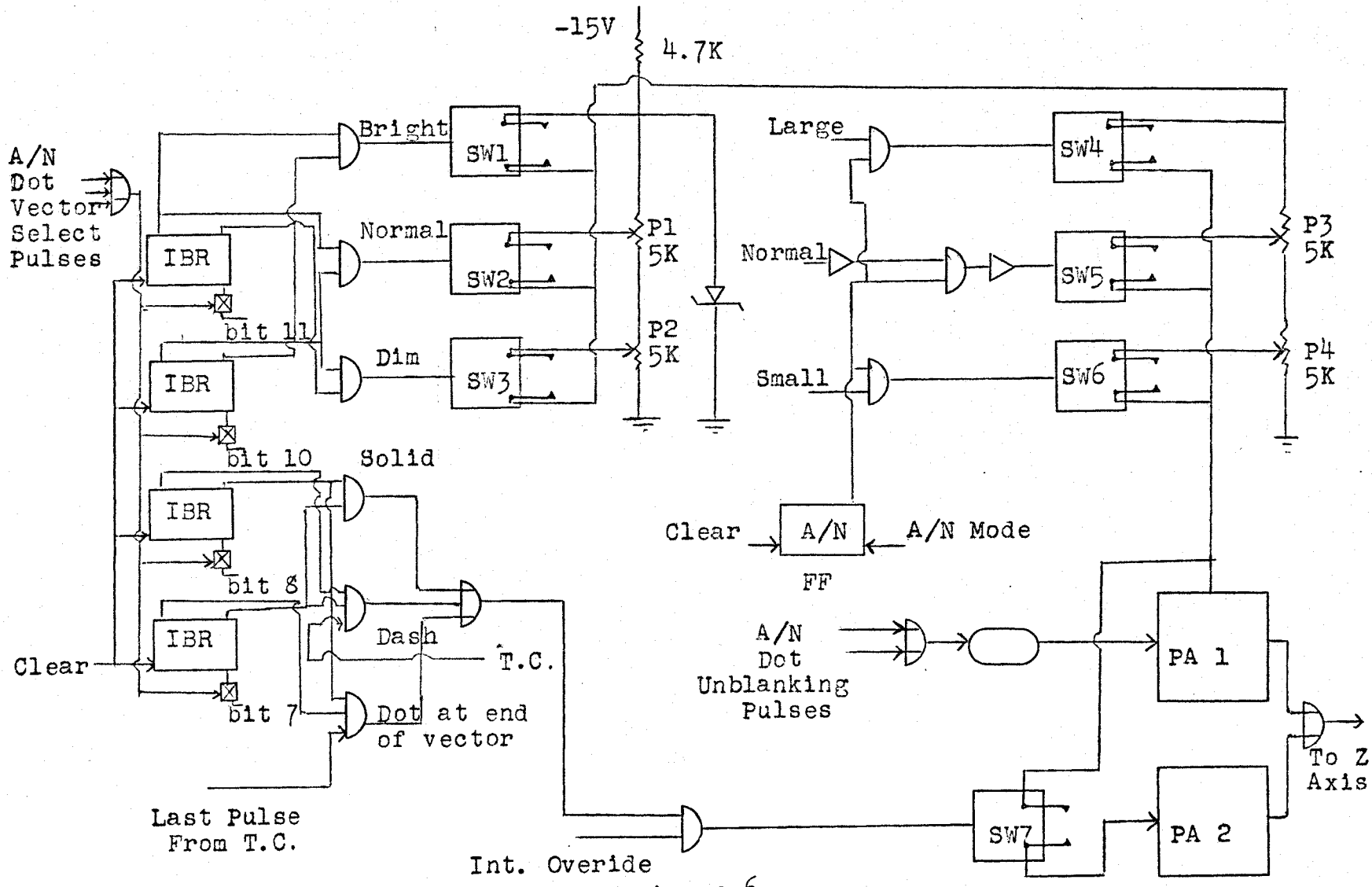


Figure 6
Intensity Control Circuitry

circuitry can be used by simply adjusting the potentiometers to compensate for the different CRT phosphor.

The actual selection of intensity takes place in the following manner. Each time an instruction pulse is sent to any of the three generators, bits 10 and 11 of the instruction word are loaded into the Intensity Buffer Register (IBR). The "AND" gates following the IBR decode these two bits according to the scheme shown in Table 1 and closes the appropriate switch (SW1, SW2, or SW3) selecting the required intensity. If a blanked intensity is chosen, none of the switches are closed, thus yielding a zero level output from the switches.

At this point in the circuit, compensation is introduced for the inconsistencies in the A/N generator. The output of the above-mentioned voltage divider does not go directly to the pulse amplifier; instead, it becomes the input to a second voltage divider that carries out the compensation for the A/N generator. Switches SW4, SW5 and SW6 in this case are controlled by the A/N generator when it is in use. If a large letter is being drawn on the CRT, SW4 is closed, applying the full output potential from the intensity selection circuit to the pulse amplifier. This causes the dots composing the letter to be brighter than normal, thus compensating for the fact that the dots are spread farther apart than normal. When normal size characters are being drawn, SW5 is closed applying the normal intensity potential to the pulse amplifier. This potential is slightly lower than that used when large letters are being drawn, as there is a voltage drop across the potentiometer P3. When small letters are drawn, SW6 is closed, thus causing a smaller than normal intensity pulse to be created. This has the effect of

Intensity Bits 9 and 10

Bits 9 and 10	Intensity
00	Normal
01	Dim
10	Bright
11	Blanked

Vector Selection Bits 7 and 8

Bits 7 and 8	Vector Type
01	Dot at Tip of Vector
10	Dash Line
11	Solid Line

Table 1
Identification of Bit Positions

reducing the brightness of the letter being drawn, which otherwise appears to be very bright due to the increased packing density of the dots.

Provision was also made so that the normal switch SW5 is closed when any generator other than the A/N generator is in use. The A/N status flip flop (A/N FF) was used to achieve this end. Whenever the A/N generator is in use this flip flop is set to the "1" state, thus giving the A/N generator control of the compensation network. However, when the A/N generator is not in use, the A/N flip flop is cleared to the "0" state, thus effectively blocking the signals from the A/N generator. Switch SW5 is also forced to close and switches SW4 and SW6 are forced to open if they were closed previously. In the case of the A/N and dot generators, the unblanking pulses from the generators are sent directly to the pulse amplifier (PA 1), where they are modulated with the selected intensity level, thus creating the required unblanking pulses. A further description of the pulse amplifier will be given in the next section of this chapter.

It should be noted that additional information is required by the intensity circuit when a vector is being drawn. Thus, whenever a VECTOR instruction is given, bits 7 and 8 of the instruction word are also loaded into the IBR. These bits contain information pertaining to the type of vector to be drawn. The coding of these two bits is given in Table 1.

The operation of the vector pulse amplifier (PA 2) is slightly different from the operation of the DOT, A/N pulse amplifier. The output of the intensity control circuit is connected to one side of an

electronic switch (SW7). The other side of the switch is connected to the input of the vector pulse amplifier. This switch is operated by trigger pulses from various points in the vector circuitry, depending on what type of vector is being drawn. These pulses are then amplified to the required level by the vector pulse amplifier.

The most commonly used vector is the solid line. Intensification of this type of vector is achieved by closing SW7 and holding it closed for the full length of time that the vector is being generated. This creates one unblanking pulse which brightens the beam throughout the full displacement of the beam, thus creating a straight line. A second type of vector is the dashed line. Intensity pulses for this type of vector are produced by using the output of bit 1 of the "timer counter" to operate the switch. A more detailed description of the "timer counter" will be given in the next chapter. By using the output of the counter as trigger pulses, the switch is repeatedly closed for a period of time, and then opened for the same period of time, thus creating a dashed line, as the pulse amplifier is continually being turned on and off. The last type of vector is a blanked vector that has a dot at the end of it to indicate where the vector ended. Intensification of this type of vector is achieved by blanking the Z-axis until the vector is complete, and then one intensity pulse is sent to the Z-axis, creating one dot at the end of the vector. The last pulse from the "timer counter" is used to create this unblanking pulse by momentarily closing switch 7.

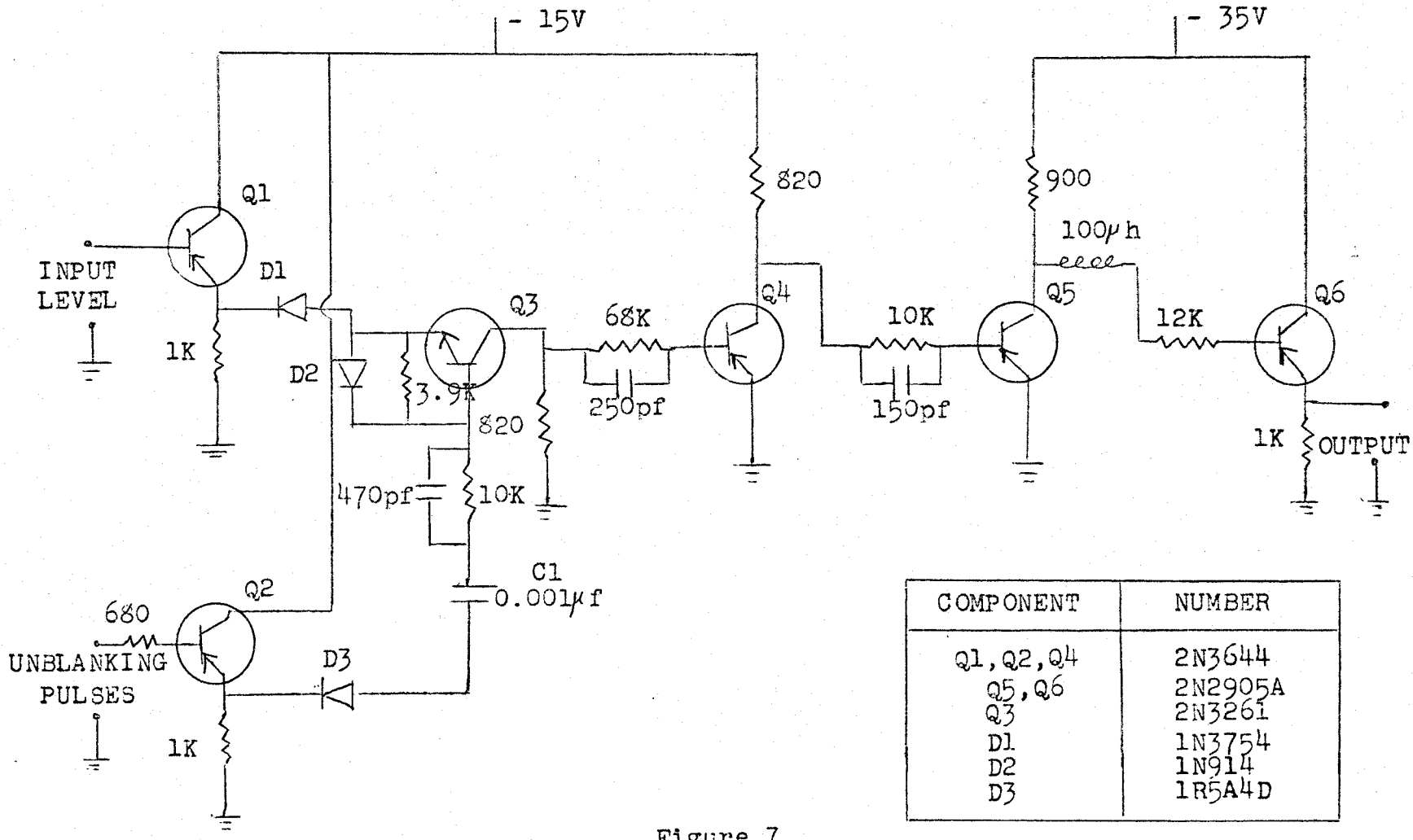
One further feature of the intensity circuit remains to be mentioned. This is the intensity override feature which is available only

when the vector generator is in use. This circuit allows blanked vectors to be drawn by the vector generator even though an unblanked intensity has been specified by the intensity circuit. Bit 1 of the second data word for the vector generator controls the use of this option. If this bit is a 1, the output of the intensity selection circuit is overriden, and a blanked vector is drawn. This option was incorporated for the convenience of the programmer, as it allows one to switch from blanked to unblanked intensities without giving a new instruction each time this is done. An added advantage lies in the fact that this feature also saves core space as extra instruction words are not required for changing intensities.

3.3 Pulse Amplifiers

(i) Dot and A/N Pulse Amplifier

A schematic diagram of the pulse amplifier that was designed for the DOT and A/N generators is given in Figure 7. Transistors Q_1 and Q_2 and their associated emitter resistor each form emitter followers which were built to prevent loading of the intensity selection circuit, and the trigger circuits, respectively. Once the desired intensity level has been selected by the intensity control circuit, a corresponding D. C. voltage is applied to the base of transistor Q_1. Since this transistor is in the emitter follower configuration, this D. C. voltage is transmitted to the emitter of transistor Q_3, and also to the base of this transistor through the 3.9 K resistor. Since the base and emitter of this transistor are at approximately the same potential, this transistor is biased off and does not conduct. Diode D 1 was included in the



COMPONENT	NUMBER
Q1, Q2, Q4	2N3644
Q5, Q6	2N2905A
Q3	2N3261
D1	1N3754
D2	1N914
D3	1R5A4D

Figure 7

Dot and A/N Pulse Amplifier

circuit to provide isolation between the emitter follower (Q_1) and the transistor switch (Q_3).

Trigger pulses which are created by the appropriate generator are applied to the base of transistor Q_2 and are transmitted to the base of transistor Q_3 through the coupling capacitor C_1. These trigger pulses are positive going pulses which turn transistor Q_3 "on", causing it to conduct. This causes a pulse to be applied to the base of transistor Q_4, which in conjunction with transistor Q_5, makes up a pulse amplifier. Transistor Q_6 and its associated emitter resistor constitute another emitter follower which provides isolation between the pulse amplifier and the Z-axis of the oscilloscope. The emitter of transistor Q_6 is connected to diode D2, shown in Figure 8, which is one half of a diode "OR" gate, which in turn is connected to the Z-axis of the oscilloscope.

(ii) Vector Pulse Amplifier

The pulse amplifier used by the vector generator is slightly less complicated than the dot and A/N pulse amplifier. The reason for this lies in the fact that the intensity level and unblanking pulses are modulated in the intensity selection circuitry, so that the pulse amplifier merely amplifies the pulses to the required potentials. Figure 8 is a schematic diagram of the pulse amplifier used by the vector generator. Transistors Q_1 and Q_2 and their associated circuitry comprise the actual amplifier. Transistor Q_3 and its associated emitter resistor are connected in the emitter follower configuration to provide isolation between the pulse amplifier and the Z-axis. Diode D 1 is the second half of the diode "OR" gate emntioned earlier, which combines the two pulse amplifiers

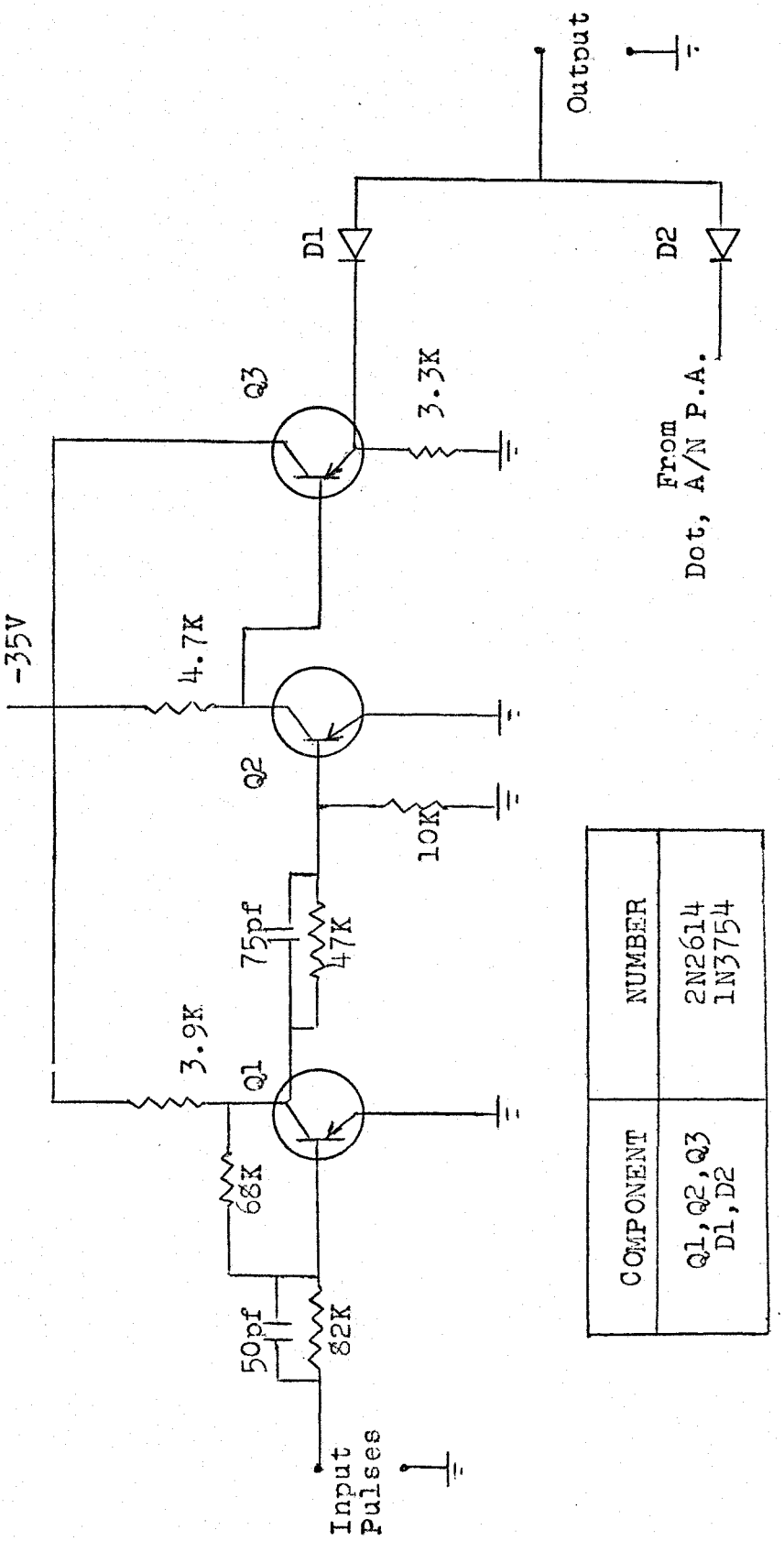


Figure 8
Vector pulse Amplifier

so that they can be connected to the Z-axis.

3.4 Results and Conclusions

The above mentioned pulse amplifiers were constructed and mounted on Digital Equipment Corporation "blank modules" to facilitate rack mounting. An equivalent of the diagram shown in Figure 6 was constructed using "NAND" logic, and this circuit along with the pulse amplifiers was connected to the computer terminal that was being built.

The intensity selection circuitry was tested and found to operate properly. That is, when instructions were given to select NORMAL, DIM, BRIGHT or BLANKED intensities, the appropriate circuitry was initiated. Also, when the A/N generator was being used, the compensating circuits were selected as expected. However, it was found that when 50 volt unblanking pulses were used, the display tended to defocus, making the display blurry. A clear display was obtained by reducing the intensity pulses to 30 volts. However, this reduction eliminated the possibility of having three distinct intensity levels for the present time, since approximately 20 volts was required to intensify the beam with such a short pulse. This meant that there was only a 10 volt change between the dim and bright intensity levels, and this was not enough to create three distinct brightness levels. Since the selection circuit operates as expected, only a few changes will have to be made to obtain the three level intensification when a display tube on which the astigmatism may be adjusted, is obtained.

Solid lines, dashed lines and blanked lines with a dot at the top were successfully displayed on the CRT, thus indicating that the vector

intensification circuits are operating properly. The intensity override circuit was also tested and found to operate as expected. Whenever bit 1 of the Y coordinate data word was a 1, a blanked vector was drawn, no matter what intensity had been chosen by the intensity selection circuitry; and whenever that bit was a 0, the intensity selection circuit had control of the brightness. Thus it is concluded that the intensity circuits were successfully constructed.

CHAPTER IV

The Vector Generator

4.1 Introduction

There are basically two methods commonly used to generate a vector. One method uses primarily digital circuitry, while the other uses primarily analog circuitry. The digital method produces vectors by use of a binary rate multiplier (BRM).[5] The BRM operates on the principle that if a fixed time is allowed to generate a vector, the ratio of the beam velocity in the Y direction to the beam velocity in the X direction is the slope of the line. A simple 4 stage binary rate multiplier is shown in Figure 9. The operation of this circuit can best be explained by use of an example which in this case will be a line with slope 5/8.

In order to draw a vector, a series of pulses must be sent to the position counters which cause the beam to be displaced. The input pulse train is sent directly to the X position counter and also to the BRM, which produces the pulses that are sent to the Y position counter. Since this line is to have a slope of 5/8, the binary equivalent of this slope which is 1010, is loaded into the proportion selector. This in turn enables the "AND" gates which are connected to the "0" side of the BRM flip flop 1 and flip flop 3. Thus as the input pulses increment the BRM counter, the "0" to "1" transitions of FF1 and FF3 are transmitted via the AND gate and combining "OR" gate to the Y position counter. Since only two of the AND gates associated with the BRM are enabled by the proportion selector for every 16 input pulses, only 10 pulses are output by the BRM. Thus a line with slope 5/8 is generated as shown in Figure 10.

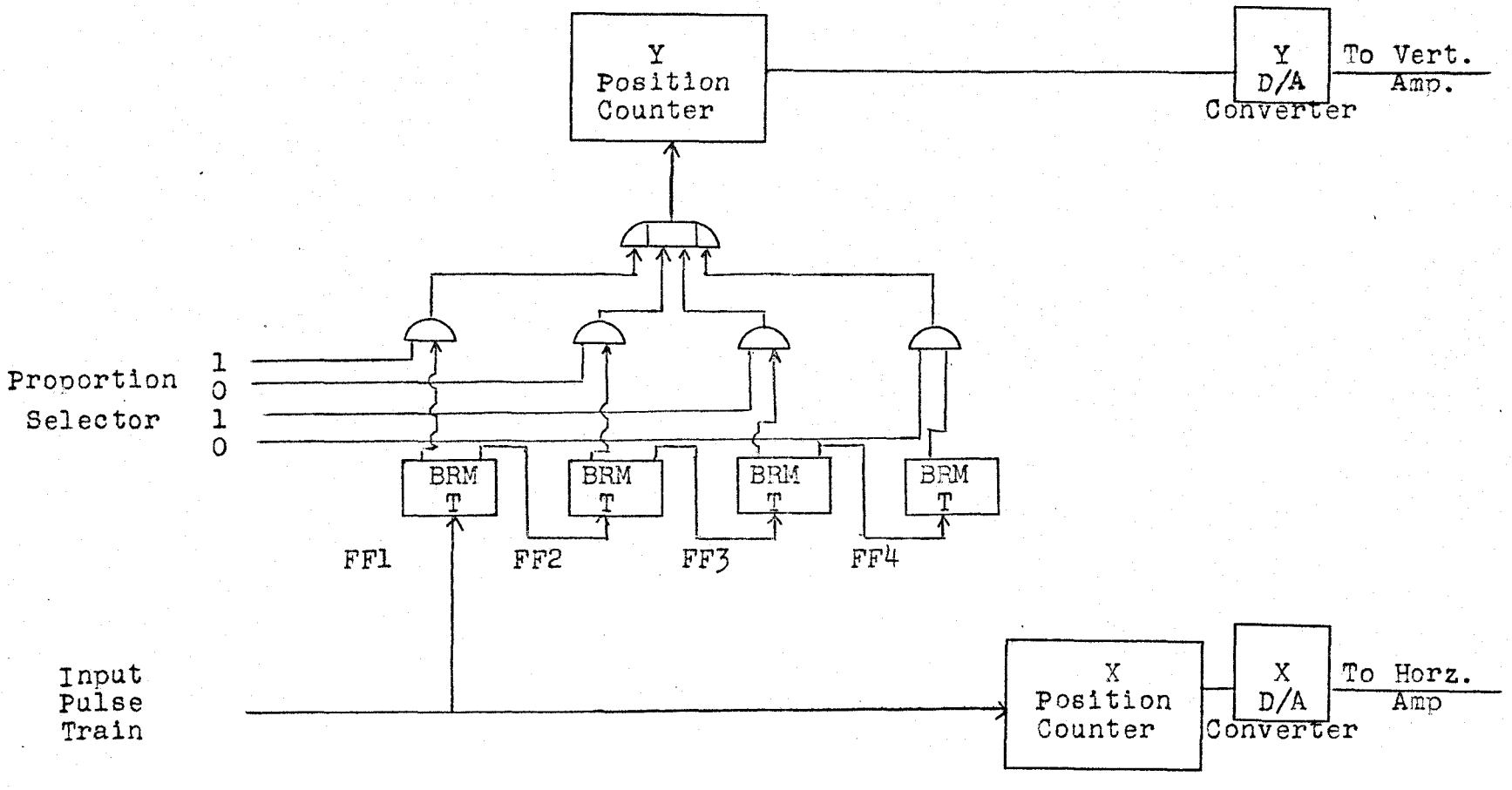


Figure 9
Binary Rate Multiplier

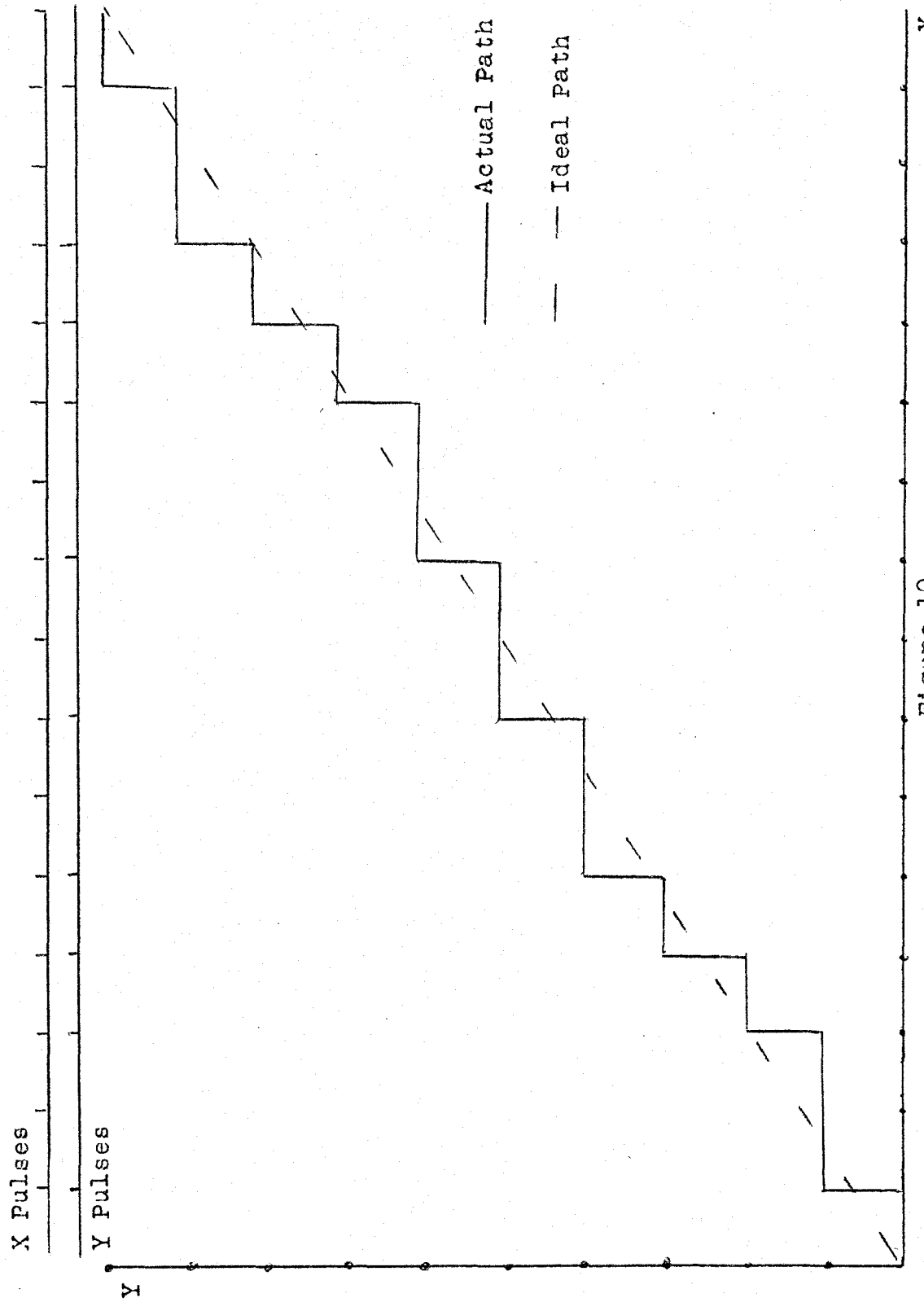


Figure 10
BRM Output

A close examination of Figure 10 reveals that the BRM generates a staircase that only approximates the ideal straight line, and herein lies one of the inherent faults with this method of vector generation. A second problem is the error introduced when the slope of the line is converted into a fractional binary number in order to be compatible with the proportion selector. The resolution of the slope value which is applied to the proportion selector circuitry depends on the BRM counter size, since each bit of the slope value is associated with one stage of the counter. However, in most cases, this is not too serious a problem, for if a 10 bit register is used, it represents an error of .1%. One other problem that arises in this type of vector generator is the fact that it tends to be slow, since a series of counters are used to generate the vector. The slowness of the BRM is its most important fault.

Because of the above mentioned reasons , it was decided to use analog techniques rather than digital. However, a certain amount of digital circuitry was required since the data output from the core is in digital form. This data must be changed to analog form and this is performed by using the D/A converters mentioned in Chapter II. Due to the fact that 10 bit registers were used in conjunction with the D/A converters, 2 data words were required by the vector generator. The first data word is the X coordinate word and contains the information required by the X deflection circuitry, while the second word contains the information required by the Y deflection circuitry. Each word contains the coordinate of the end point of the vector relative to the origin which is located at the lower left hand side of the CRT. These coordinates are changed from absolute to relative coordinates by the analog circuits.

A more complete description will be given in the next section of the thesis.

4.2 Analog Vector Generator

(1) Control Circuit

Figure 11 is a diagram of the vector control circuitry. This circuit directs the loading of the X and Y D/A converter registers, and also controls the opening and closing of many of the switches used in the analog circuit. Previous to sending the mode selection pulse, a clear pulse is sent out by the core circuitry. This pulse clears the control, status, load and clock control flip flops (CFF, SFF, LFF and CCFF). This pulse has initialized the system so that the TRUE side of all the flip flops are in the "0" state.

If the vector mode has been selected, a pulse is sent to the control flip flop (CFF) which sets this flip flop to the "1" state. Approximately 400ns later the load data pulse is received which sets the status flip flop (SFF) indicating that no more data is required. This pulse is also transmitted through "AND" gate number 1 to PA 1, which produces a pulse that loads the temporary X register and also clears the SFF, indicating that more data is required. This same pulse is delayed until the temporary X register has been loaded , and then is used both to complement the load flip flop (LFF), and to clear the X and Y D/A converter registers. About 8μs after the SFF has been cleared a second load data pulse is received. This pulse sets the SFF to indicate that no data is required and is also transmitted through "AND" gate number 2 to PA2 which produces the pulse used to load the X and Y registers and clears the temporary X register. The pulse produced by PA2 is delayed and sent to the clock control flip flop(CCFF) which initiates the clock. As before, a complementing pulse is sent to

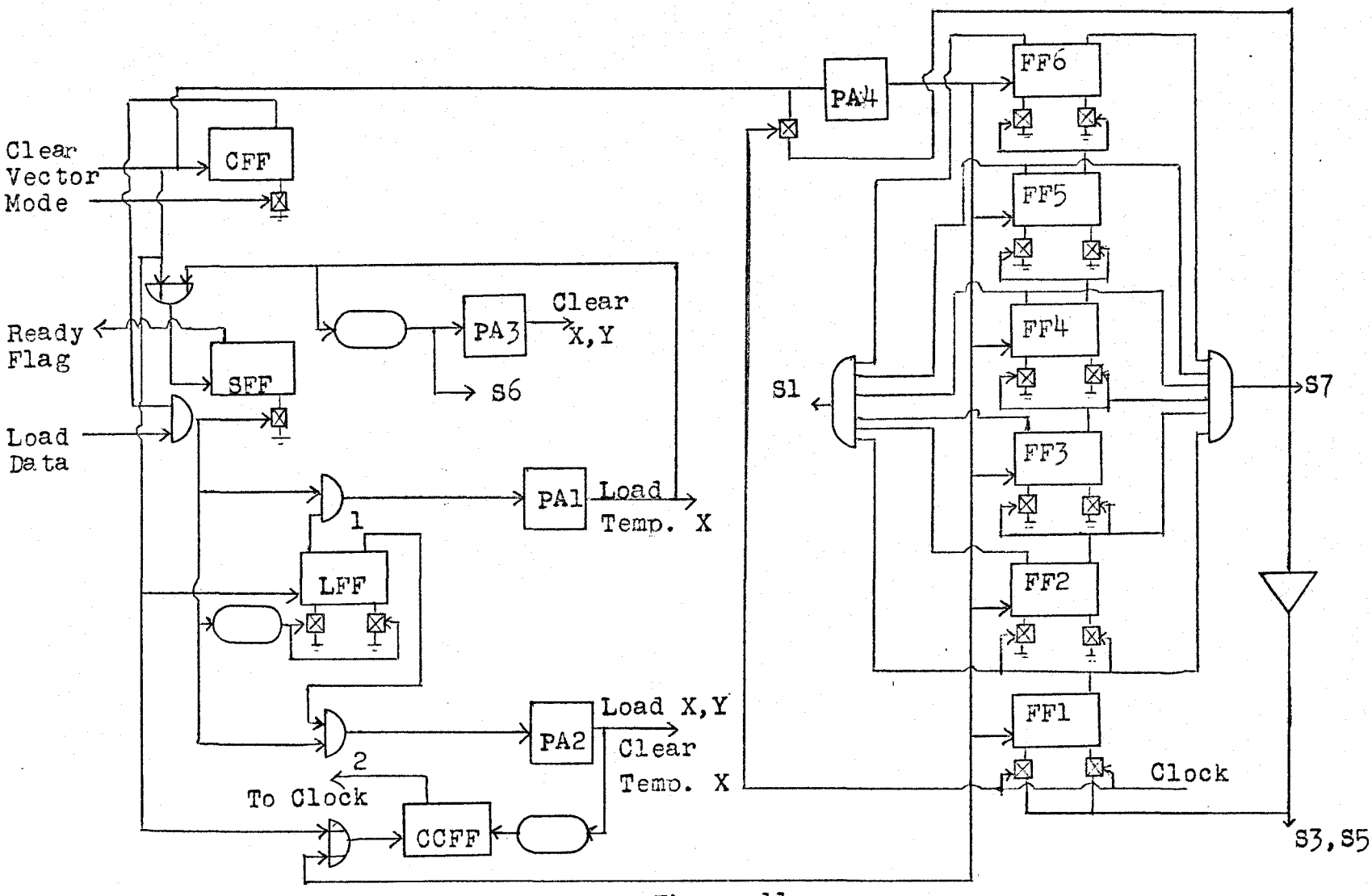


Figure 11

Vector Generator

the LFF so that it is again ready to load the temporary X register.

At this time the clock begins sending out pulses at a rate of 375 KHz. These pulses increment the timer counter which is a 6 bit counter consisting of FF1 to FF6. The counter is designed so that it resets at a count of 39 and stops the clock by setting the CCFF to the 1 state. We should note that the timer counter controls most of the switches used in the analog circuit, and also controls the length of time that the integrators are allowed to operate. Since the counter is pulsed at a rate of 375 KHz, it takes approximately 104μs to complete its count. This is the length of time that the analog circuits are in operation each time a vector is drawn.

(2) Analog Circuit

A diagram of the analog circuit (7) (8) (10) that was used by the vector generator is given in Figure 12. This circuit was built in duplicate, as separate circuits were needed for the X and Y deflection plates. However, both circuits functioned identically and operated concurrently. A truth table for the switch operation is given in Table 2, and the switch timing diagram is given in Figure 13. Since the operation of the circuit is identical for both the dot and A/N generators, only the A/N generator will be discussed in the following explanation of the circuit. Initially, we will assume that all the capacitors are discharged and that none of the generators are in operation. With the circuit in this state, all switches will be opened, except S7.

If a vector instruction is now received, switch S6 is closed for 7μ seconds to sample the integrator output. Due to the inverting

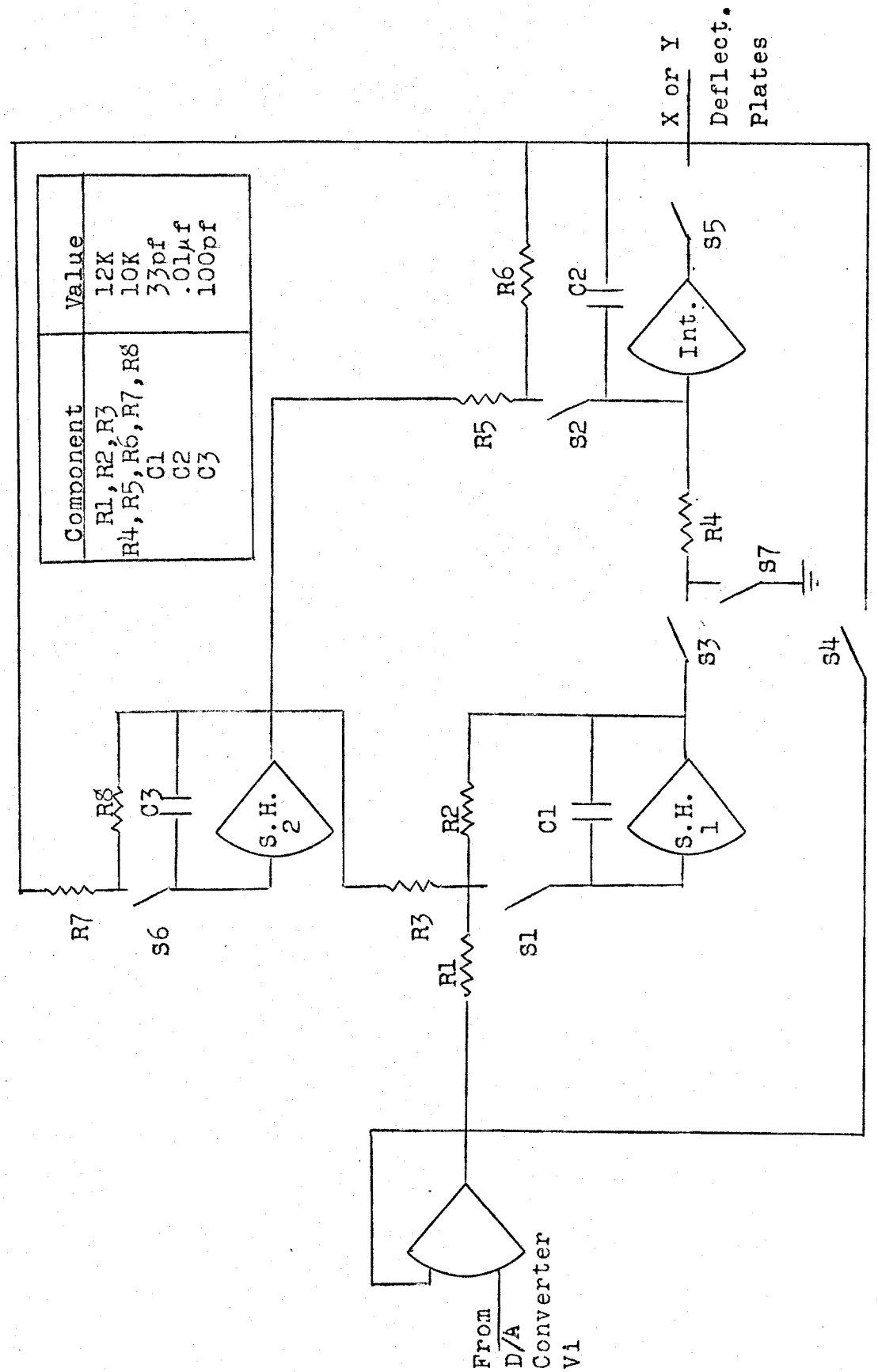


Figure 12
Analog Circuit

Switch

Mode: Switches 1 Closed 0 Open	S1	S2	S3	S4	S5	S6	S7
A/N or Dot	0	1	0	1	0	1	1
Output Sample	0	0	0	0	0	1	1
Previous to Vector Generation	1	0	0	0	0	0	1
Vector Generation	0	0	1	0	1	0	0
$\overline{\text{A/N, Dot, Vector}}$	0	0	0	0	0	0	1

Table 2
Switch Operation

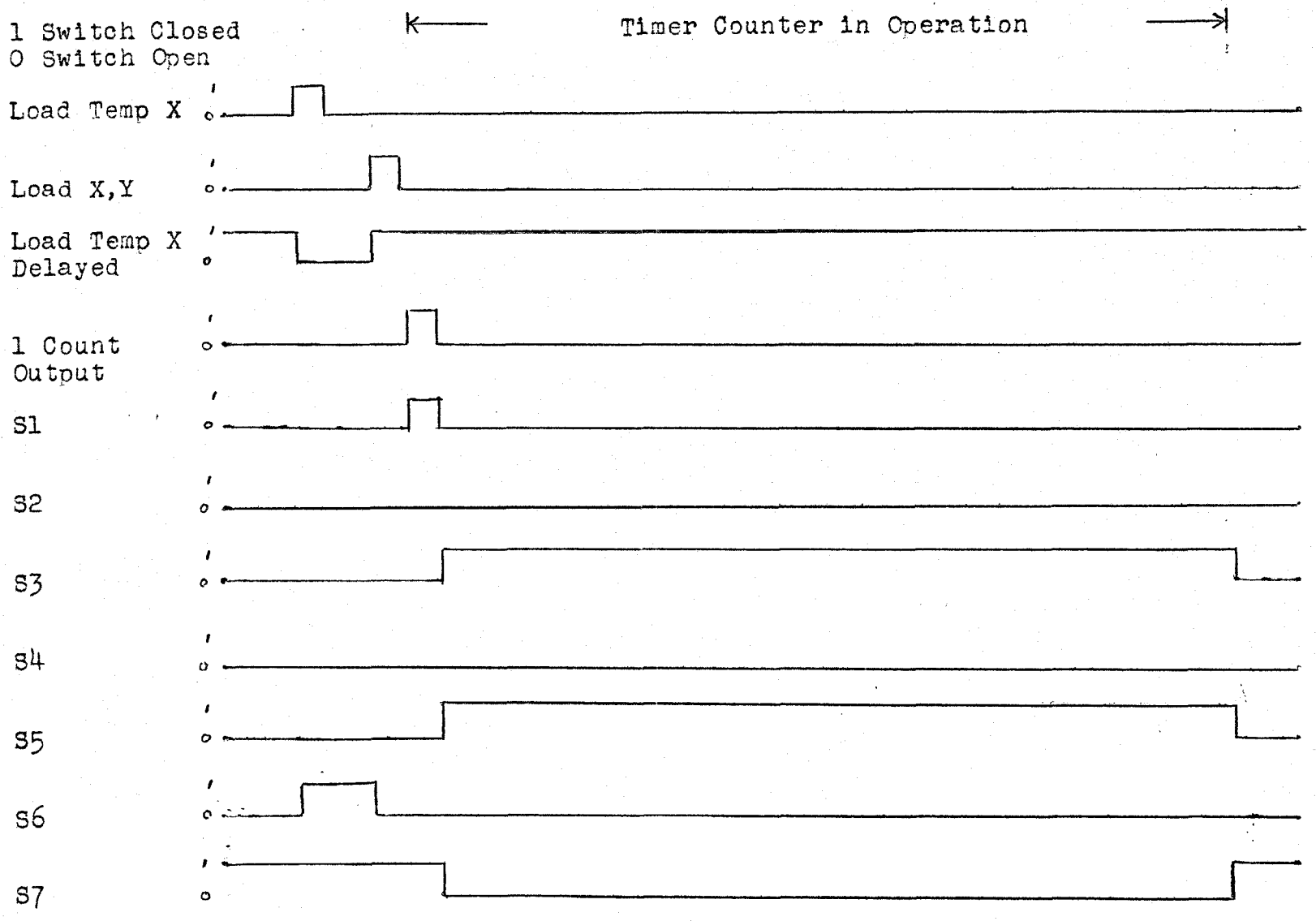


Figure 13
Switch Timing

property of the operational amplifier, the output of the Hold 2 circuit will be the negative of the integrator output. Shortly after the sampling is complete, a D. C. potential Vi will be output by the D/A converter and will appear across resistor R1. The timer counter now begins counting, and the 1 count is gated to switch S1, forcing it to close. Since resistors R1, R2 and R3 are of the same value, the potential Vi from the D/A converters is summed with the potential output from the Hold 2 circuit, and the resultant is stored across capacitor C1. Since all capacitors were assumed to be initially discharged the value Vi will be stored across C1. Due to the inverting property of the operational amplifier, the output from the Hold 1 circuit will actually have the value of -Vi. As the counter continues beyond the count of 1, switches S1 and S7 open again and switches S3 and S5 close. These switches remain closed until the timer reaches a count of 39, at which S3 and S5 open and S7 closes. It takes the timer counter 100μs to reach this count, thus the switches are held closed for 100μs. The time constant of the integrator circuit was also chosen to be 100μs so that when the switches are opened, the output of the integrator will be exactly the negative of its input. That is, the final output potential from the integrator circuit will be Vi. During the time that the integrator is in operation the beam of the CRT is being displaced on the screen, since the integrator output is connected directly to the deflection plates. It is during this integration time that the beam is normally intensified to produce the required vector.

In order to continue the explanation of the circuit we will assume that the next word from the core is an instruction word requesting

the use of the A/N generator. Because the next word is an instruction word, the vector generator will not clear the D/A converter registers. Instead, it leaves them as they were; thus the output of the D/A converter remains the same as when the vector was drawn. When the A/N generator begins operation, switches S2, S4 and S6 close. Now the D/A converter is connected directly to the deflection plates of the CRT. The A/N generator does not clear the D/A registers as does the vector generator. Instead it continues from the position where the D/A is presently located. While the A/N generator is in operation the Hold 2 circuit is also in operation. This circuit follows the change in output potential from the D/A converter and updates the integrator circuit which follows at a slower rate. At the end of the character generation, switches S2, S4 and S6 open. At this point the circuit has been updated to the new potential produced by the D/A converters while the A/N generator was in use. We will call this new potential Vn. Thus the output of the integrator circuit will be Vn and the output of the Hold 2 circuit will be -Vn.

We will now assume that the next instruction is a vector instruction. The operation of the circuit is much the same as was described for the first vector instruction, except that the capacitors are not discharged. As before, switch S6 closes to sample the integrator output and a new DC potential Vi will be output by the D/A converter, which is the potential that corresponds to the end point of the vector to be drawn. At this time the timer begins counting and the 1 count closes Switch S1. The output of the Hold 2 circuit is summed with the output of the D/A converter and the result is stored on capacitor C1. Since the output of the Hold 2 circuit is -Vn as mentioned previously, the potential output

of the Hold 1 circuit will actually be -(Vi - Vn). We should note that Vi - Vn is actually the potential difference between where the beam is presently and the end point of the vector. As before, when the count continues beyond 1, switches S1 and S7 open and switches S3 and S5 close. These switches remain closed for 100μ seconds allowing the integrator to integrate from its initial potential to the final potential of Vi. Again, as before at the end of 100μs, switches S3 and S5 open and S7 closes. The circuit is now ready either to have more data sent to the vector generator or to track the changes brought about by the A/N generator.

If a series of vectors are to be drawn, the circuit operates just as was described for a vector following the generation of an A/N character. Thus there is no need to discuss this situation. As was mentioned previously, the operation of the circuit when the dot generator is in use, is identical with the operation of the circuit when the A/N generator is used.

4.3 Results and Conclusions

Success was not achieved using the circuit shown in Figure 12, as the vector generator did not always produce the correct output for a given output. In order to isolate the problem, switches S2, S4, and S5 were removed as well as resistors R5 and R6, as these components were used only in conjunction with the DOT and A/N generators to update the integrator circuitry. The remaining circuit which performs the actual vector generation is shown in Figure 14. Since this is the part of the circuit that was malfunctioning, further testing was carried out on this circuit.

With a given input voltage, Vi, of two levels (0 and -5V) the correct display deflection output voltage, Vo, from the integrator could

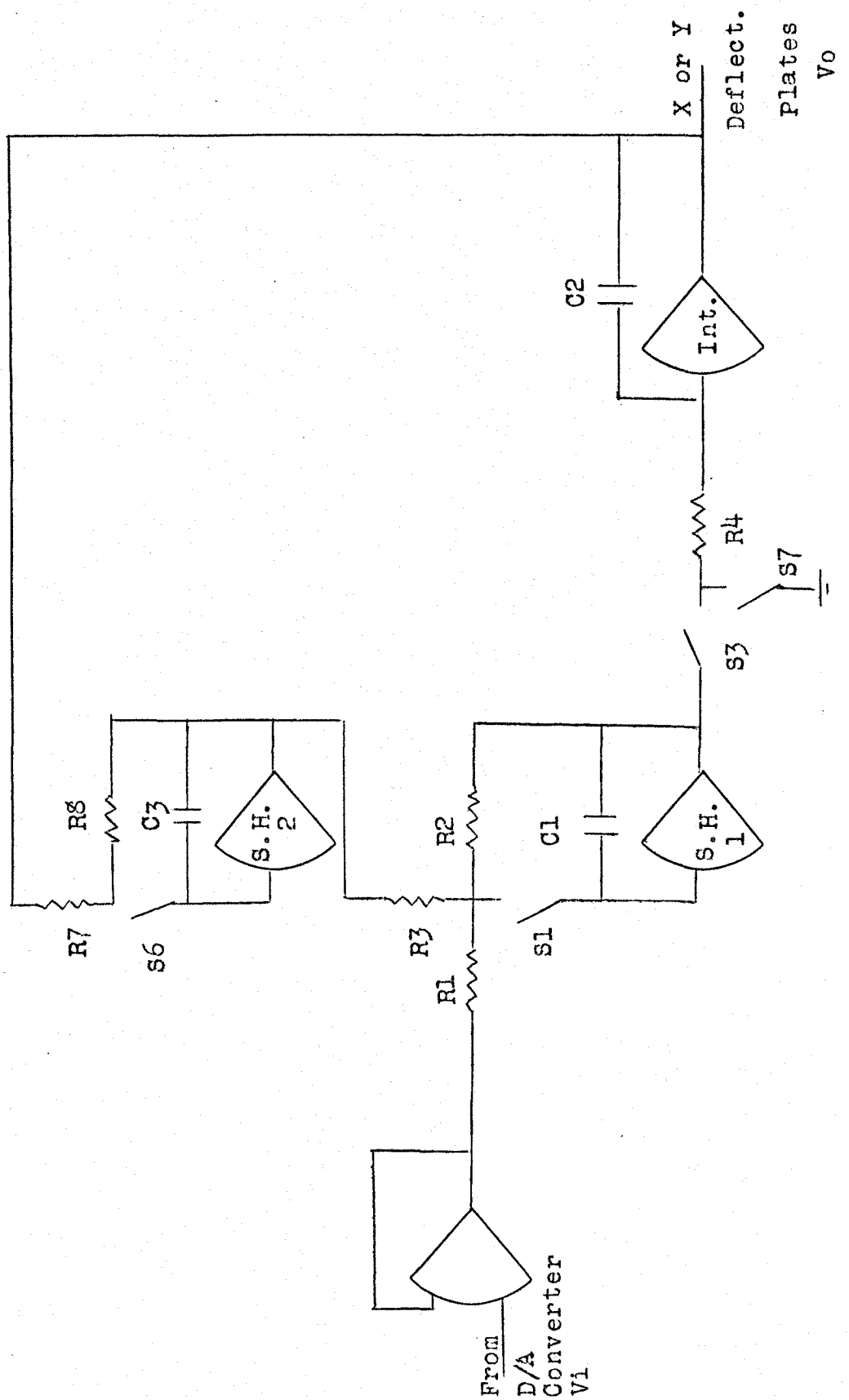
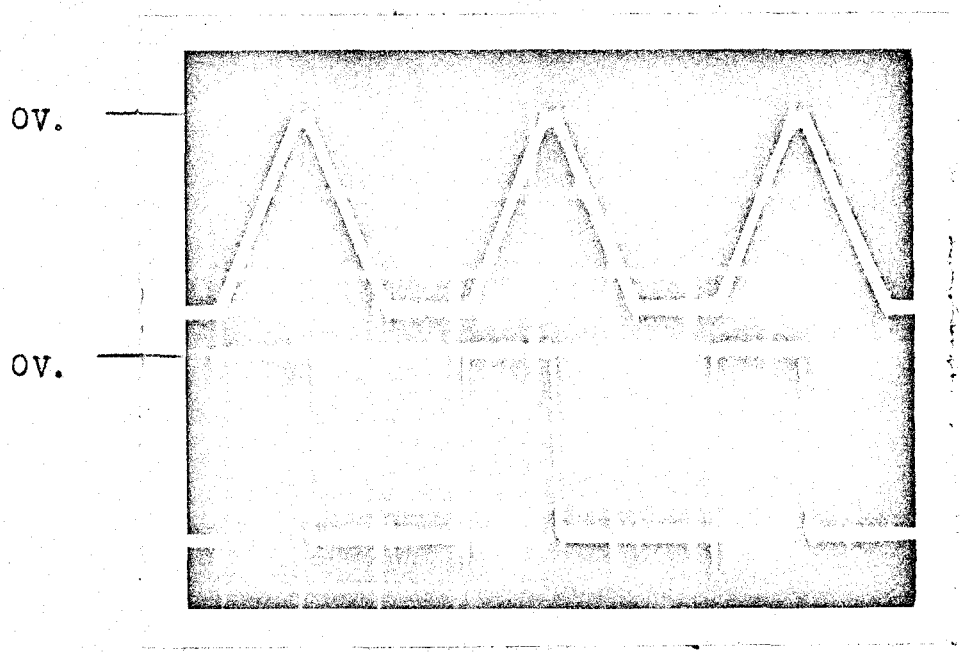


Figure 14
Vector Generator

be obtained by the correct setting of resistor R8 which controls the overall gain of the output sampling loop. The top half of Figure 15 shows the integrator output for a 0 to -5 volt input which is shown in the lower half of the same figure. However, when the input levels were changed to 0 and -0.8V it was found that the correct integrator output was obtained, except that there was a shift in d. c. level as shown in Figure 16A. By changing the value of resistor R3 the d. c. level could be corrected as shown in Figure 16B. This was also the case when the input was changed to -0.8 and -5V as shown in Figure 17A and 17B, after R3 was set for an input of 0 to -5V .

By examining the waveforms in the circuit it was noted that the change of output level was apparently due to an incorrect level at the output of the summing sample and hold element (SH2) which was clearly compensated for by altering the gain resistor R3. This led to an investigation as to the cause of the change of level, which implied incorrect sampling and/or holding of the sample and hold circuits. On observing the waveforms at the output of the sample and hold circuit #2 (SH2) shown in Figure 18, it is seen that after a change of output due to a new sampling, the waveform exhibits considerable changes before settling to a final value. A similar effect takes place at the output of SH1. From this it can be concluded that the effective input to the integrator apparently has the correct change of level but at the incorrect mean value.

The amplifiers were checked and found to be satisfactory, so that the only remaining possible of error was the operation of the electronic switches which had been assumed as satisfactory. As a first test, a d. c. input was applied and the output impedance was measured using a



Vert. Sens. : 2 Volts / cm.
Horz. Sens. : 100μ sec. / div.

Figure 15
Integrator Operation (0 to -5V)

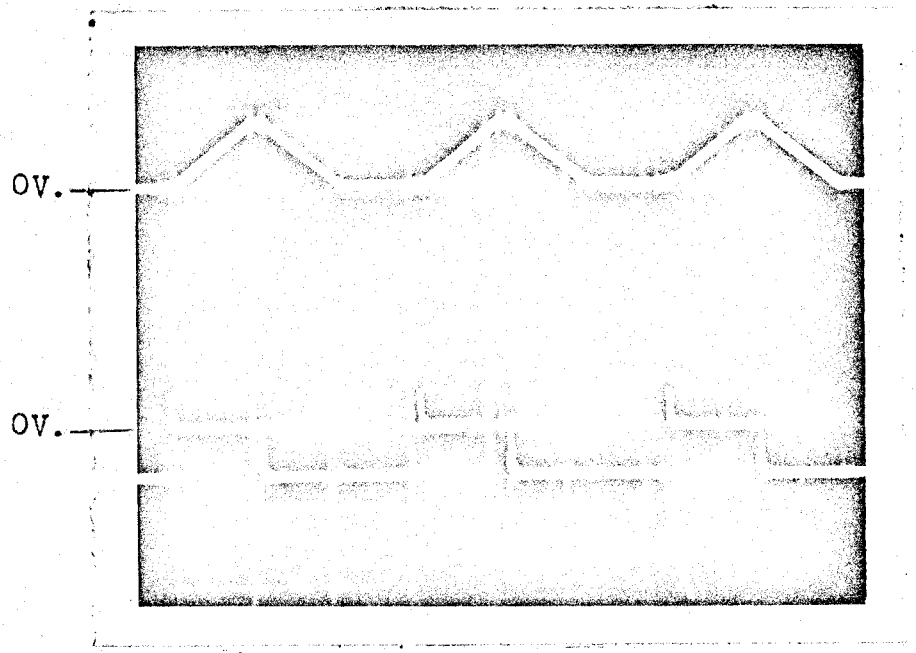


Fig. 16 A

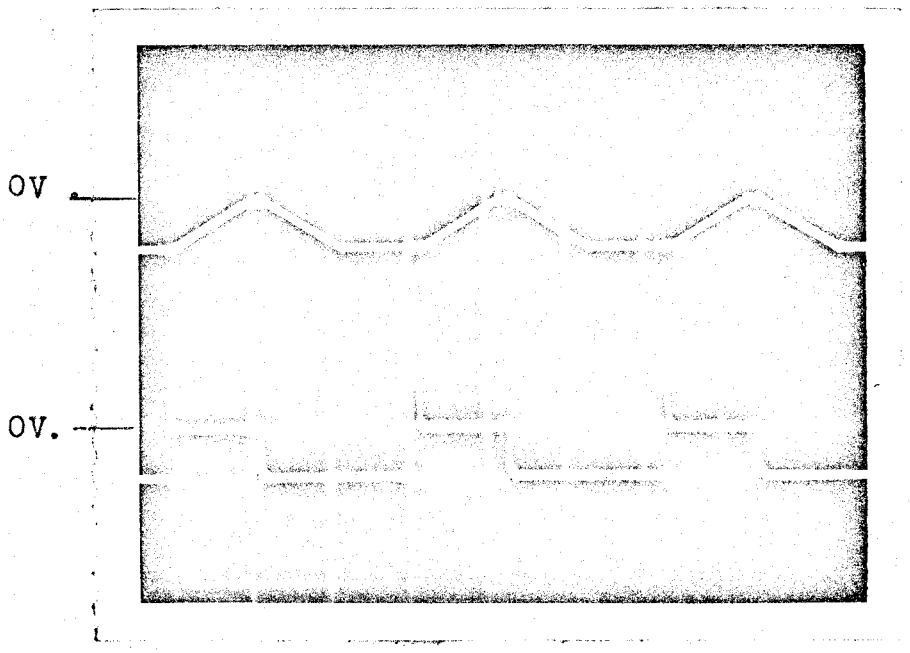


Fig. 16 B

Vert. Sens. : 1 Volt / cm.
Horz. Sens. : 100 μ sec. / div.

Figure 16
Integrator Operation (0 to -0.8 V)

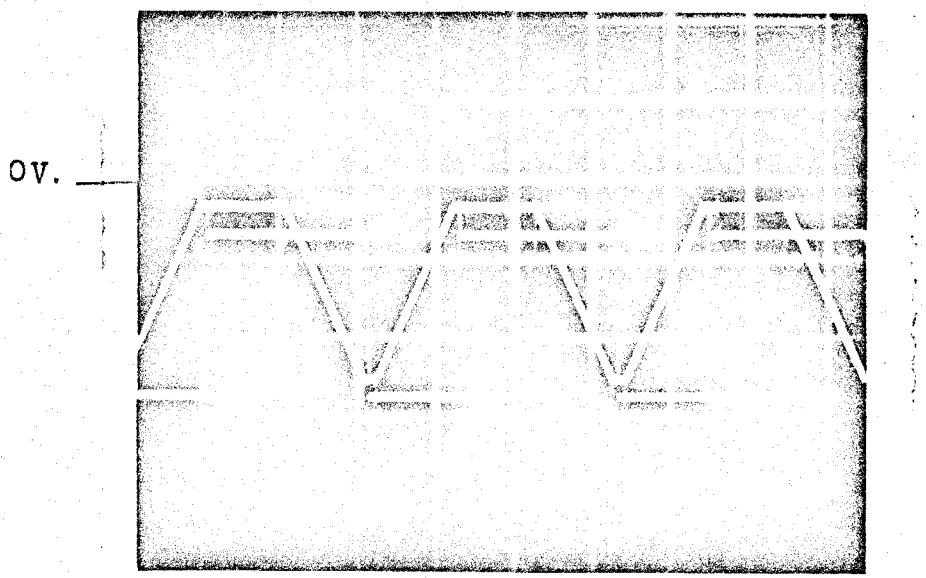


Fig. 17 A

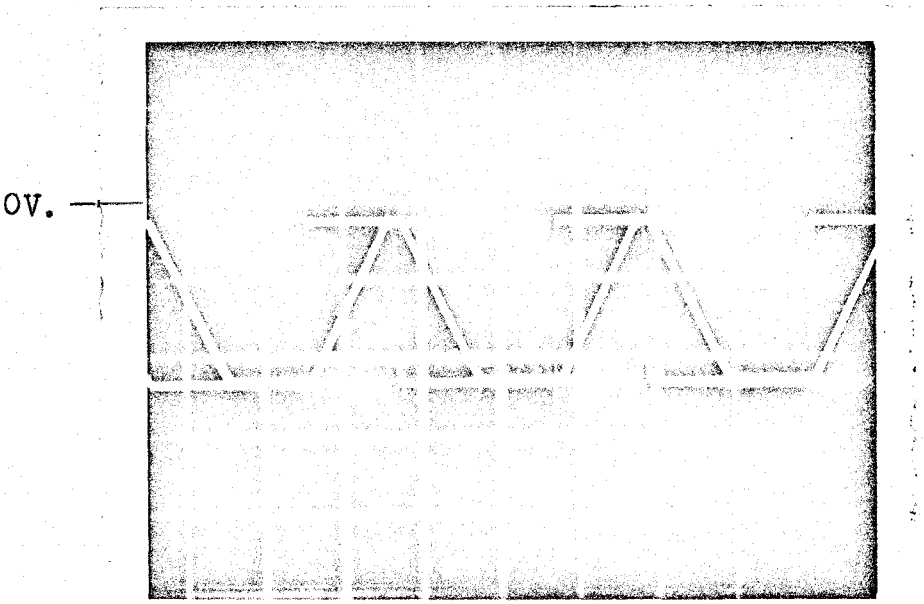
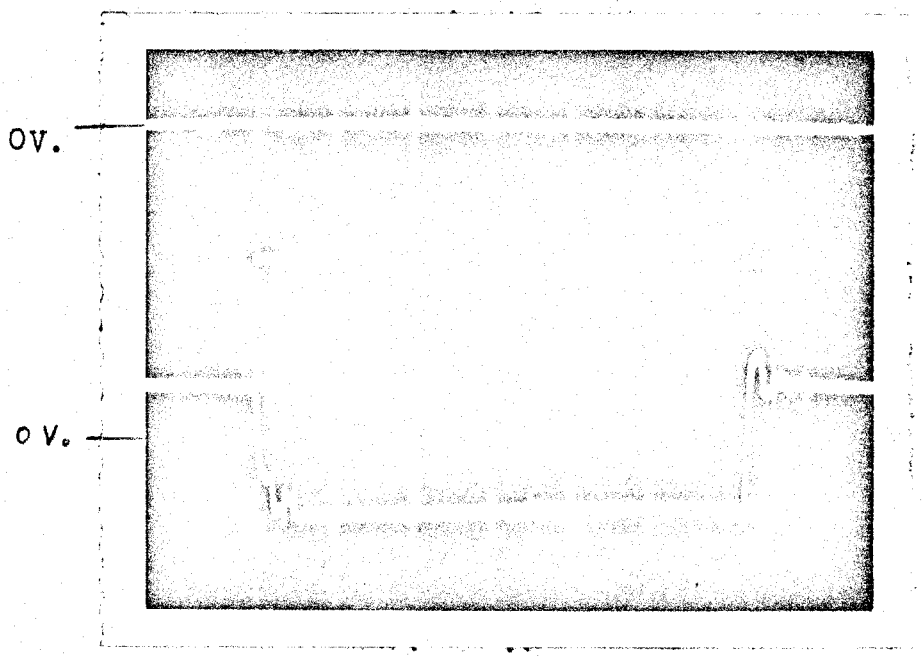


Fig. 17 B

Vert. Sens. : 2 Volts / cm.
Horz. Sens. : 100 μ sec. / div.

Figure 17
Integrator Operation (-0.8 V to -5 V)



Vert. Sens. : 2 Volts / cm.
Horz. Sens. : 20 μ sec. / div.

Figure 18
Output of S.H. #2 Circuit

digital voltmeter which indicated that the values of resistance were within the specifications; the closed resistance equalled 230 ohms and the open resistance was too high to be measured with the available equipment.

A second test was performed to measure the transient response using the circuit given in Figure 19 in which the resistor R was of the same order of magnitude to that used in the sample and hold circuits. The switch was operated by the same pulse source as used for SH#2. The output voltage obtained for different input voltages (V), which were both positive and negative, are shown in Figure 20. In all pictures the top trace is the trigger pulse which causes the switch to close when it goes negative (-3V). Figure 20A shows the output when the input voltage V was set to ground. The results obtained when the input voltage V was set to +1, -1, +2, -2, +5 and -5 volts is shown in Figure 20B to 20G respectively. At low level voltages (<3V) it will be observed that the output overshoots to a large extent and furthermore the switch has a "turn off" time of about 1 s. These two effects can understandably introduce errors in the sample and hold circuits as (i) the sample will tend to be high when there is an overshoot at the lower voltages, and (ii) the capacitor together with the imperfect switch resistance will tend to cause an integrator action as shown in Figure 21. The solution appears to be the use of improved switches which might have to be specially designed.

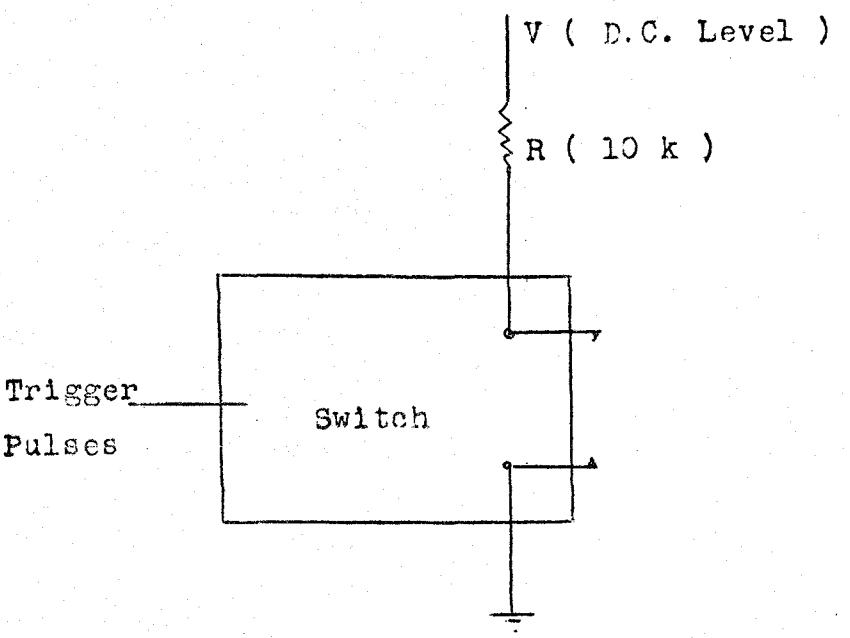
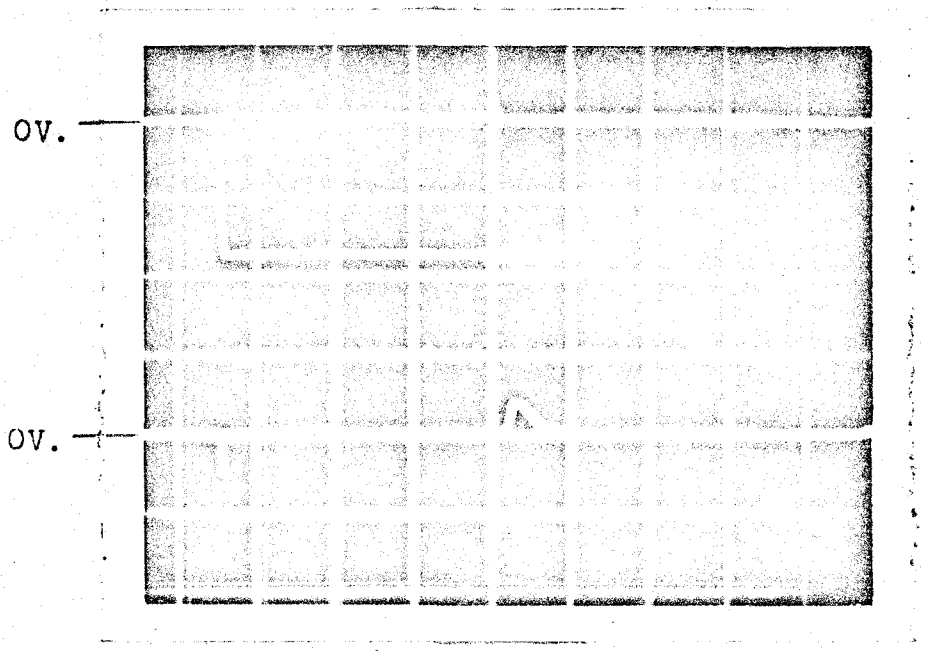


Figure 19
Switch Transient Response Test Circuit



Vert. Sens. : 2 Volts / cm.
Horz. Sens. : 2 μ sec. / div.

Figure 20 A

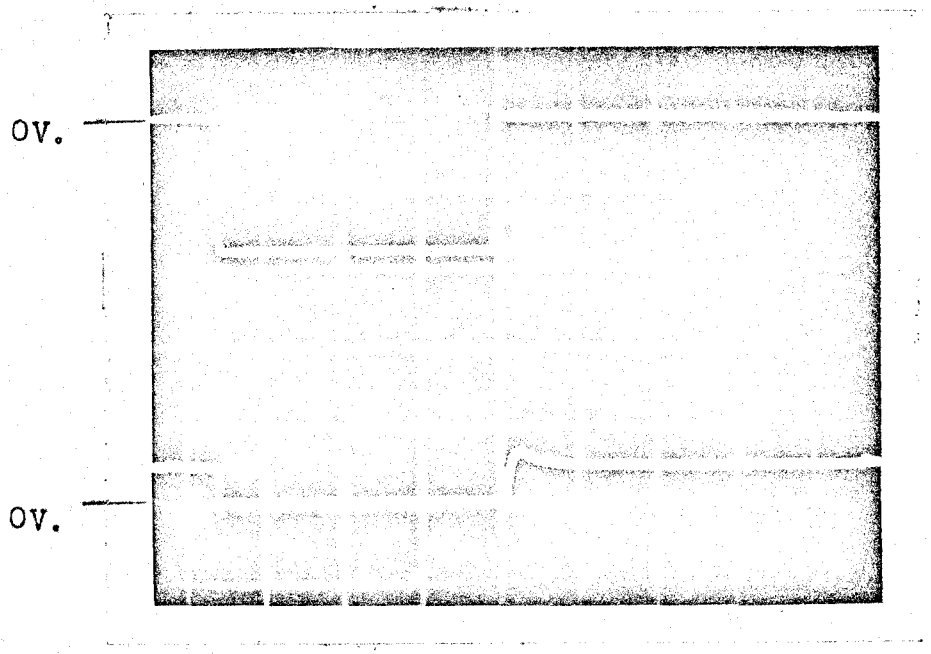


Fig. 20 B

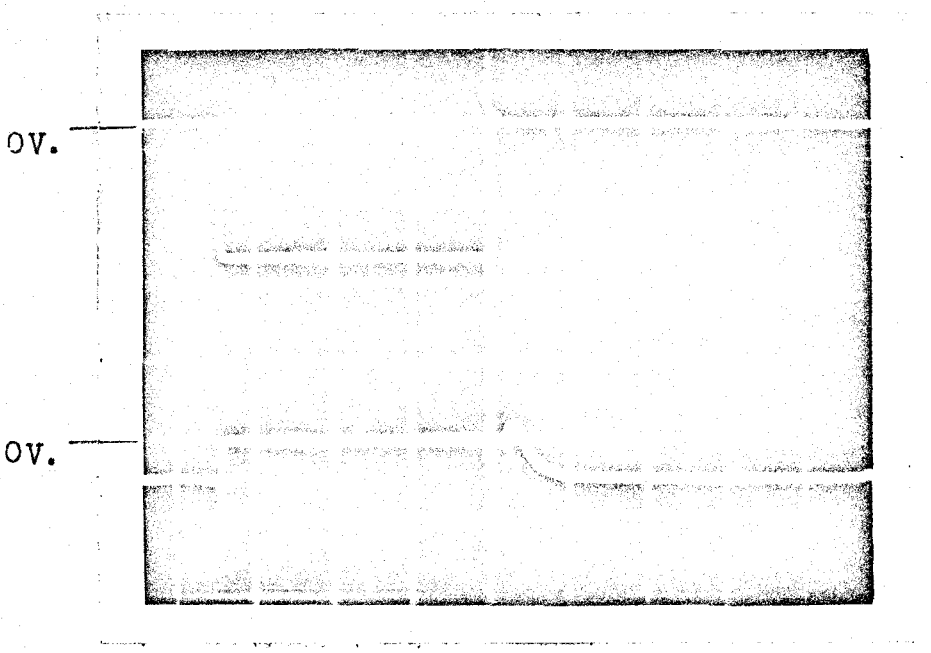


Fig 20 C

Vert. Sens. : 2 Volts / cm.
Horz. Sens. : 2 μsec. / div.

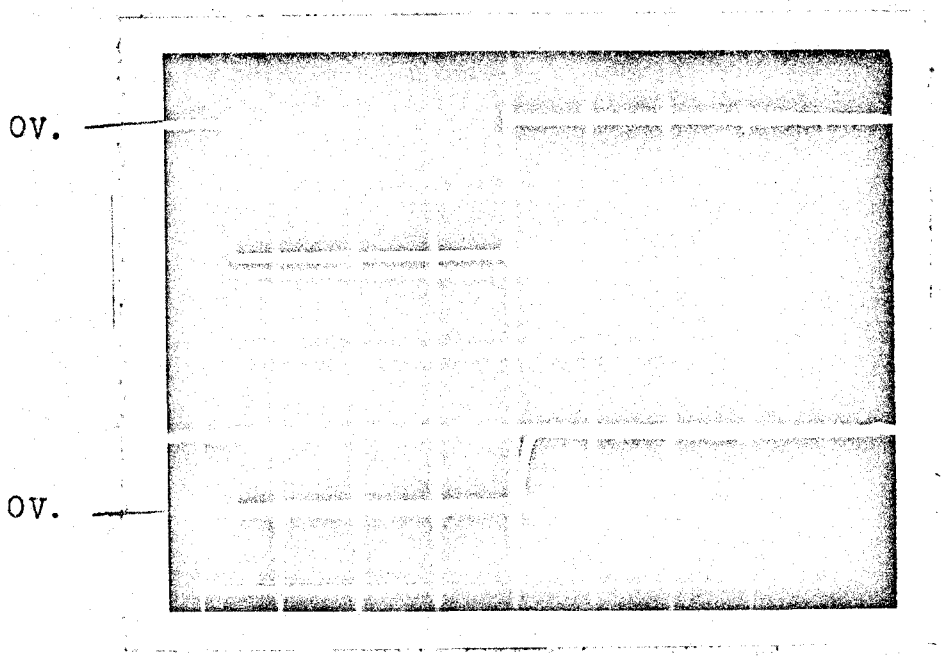


Fig. 20 D

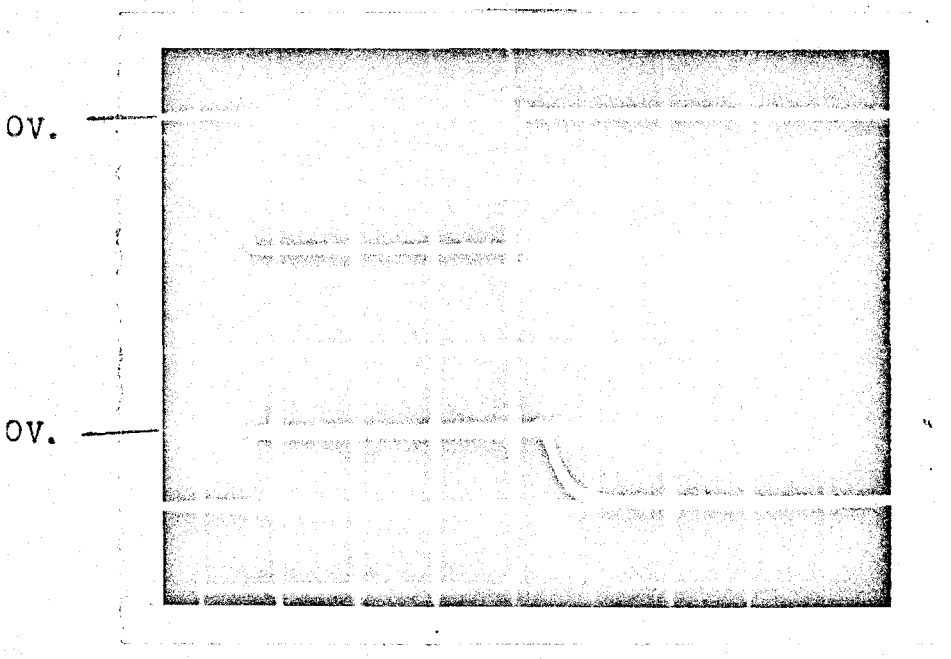


Fig. 20 E

Vert. Sens. : 2 Volts / cm.
Horz. Sens. : 2μsec. / div.

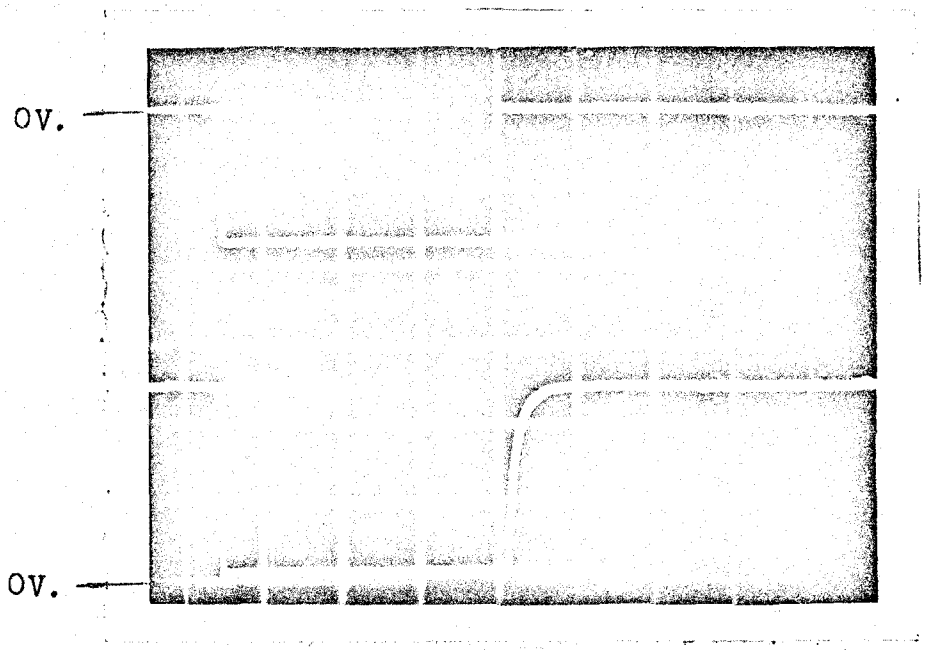


Fig. 20 F

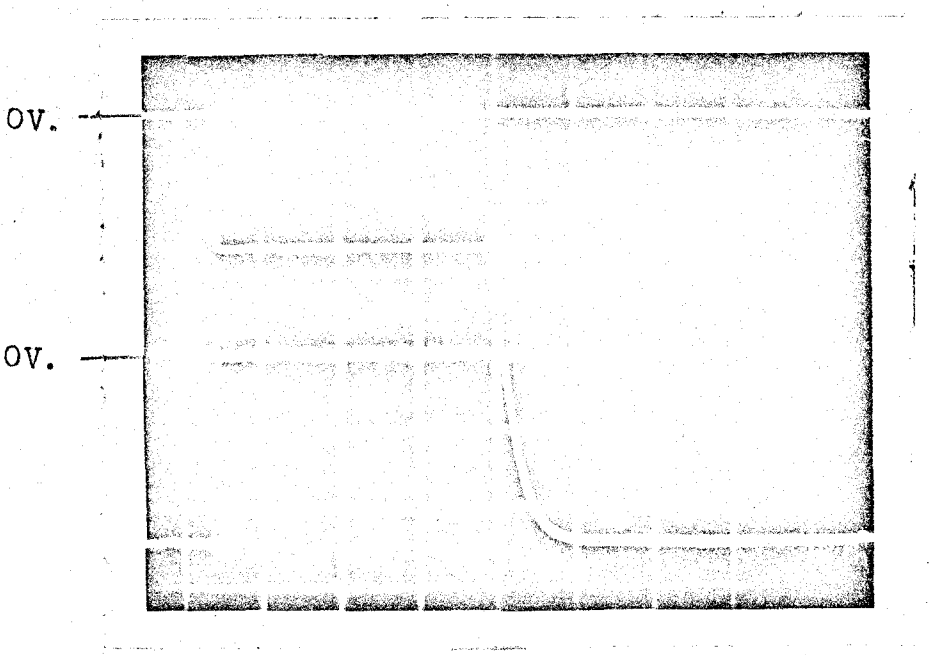


Fig. 20 G

Vert. Sens. : 2 Volts / cm.
Horz. Sens. : 2 μ sec. / div.

Figure 20
Transient Response Test Results

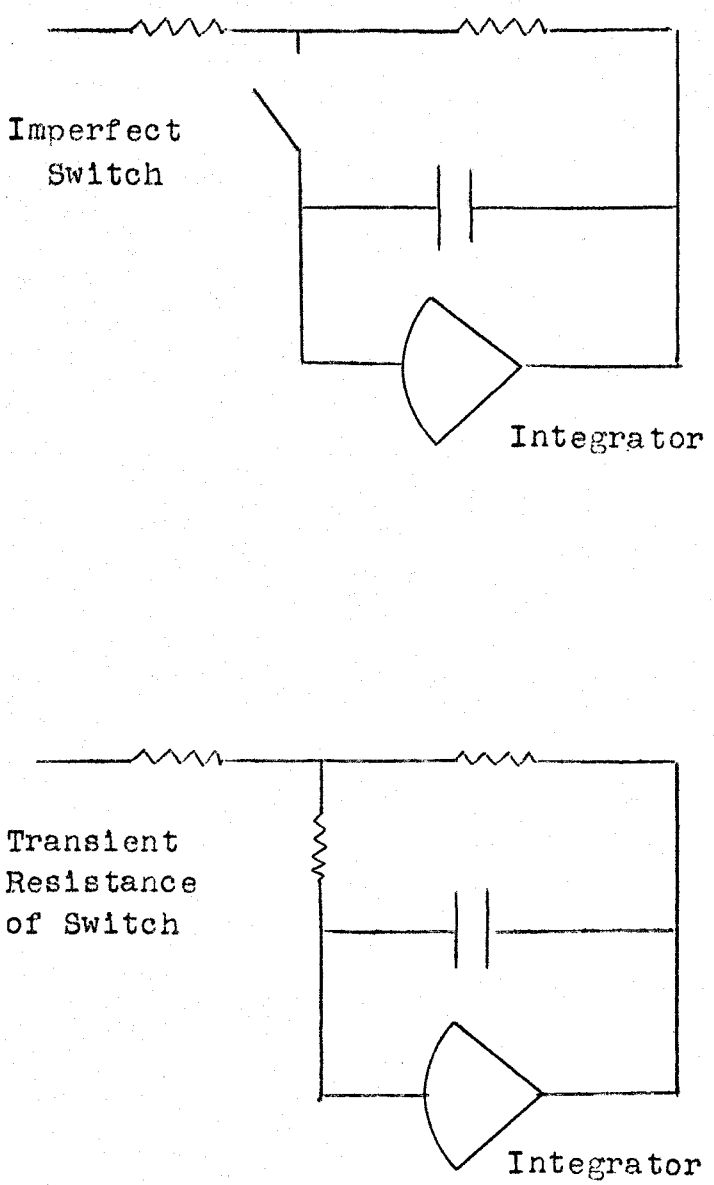


Figure 21
Integrator Action due to Imperfect Switch

CHAPTER V

General Conclusions

The dot generator was successfully designed and constructed as dotted line segments were displayed on the CRT according to the design specifications. The intensity selection circuits also operated as was intended. However, it was not possible to produce three distinct levels of brightness using the existing CRT Z - amplifier.

From the results of the tests performed on the vector generator it can be concluded that the design used is satisfactory, provided that improved switches are used in its construction.

APPENDIX I

LOGIC NOTATION

The following is a description of the various logic symbols used in this thesis.

(1) Logic Levels and Pulses

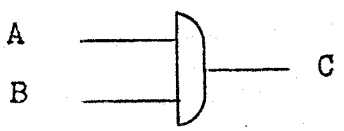
Ground potential is equivalent to the logic level "1"; therefor a ground connection represents a permanent "1" level. A straight line with no arrow head is the graphic symbol used to represent a level input or output.

LOGIC LEVEL ———————————

A pulse is defined as the leading edge of a level change from the "0" to "1" state where the "1" state is maintained for a minimum of 100 ns. The graphical representation of a pulse is a straight line with an arrow head.

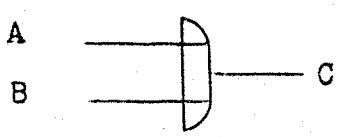
PULSE ——————————→

(2) AND GATE



$C = A \cdot B$

(3) OR GATE

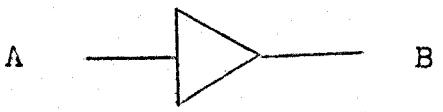


$C = A + B$

(4) DELAY

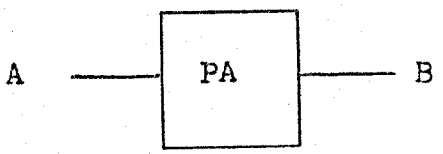
B = Delayed A

(5) INVERTER



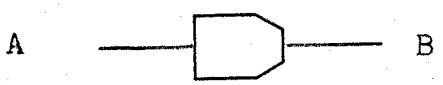
$B = \overline{A}$

(6) PULSE AMPLIFIER



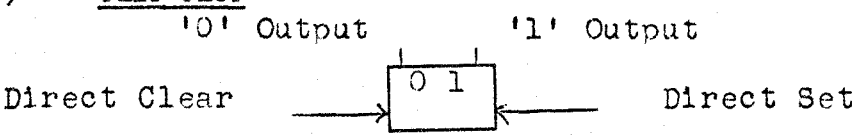
B = A B is merely A amplified.

(7) CLOCK

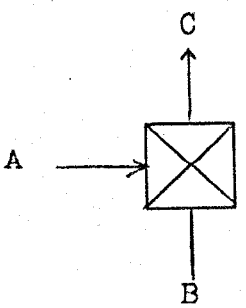


A is an enable level which allows the clock to operate. B is a series of 100 ns pulses, the frequency of which may be varied.

(8) FLIP FLOP



(9) DCD GATE

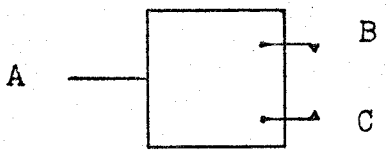


C = A . B

The DCD gate performs the "AND" operation between a level input and a pulse input and produces a pulse output. The level

input must be present for at least 400 ns before the input pulse is applied to the gate.

(10) ELECTRONIC SWITCH



When point A is held at ground potential points B and C form an open circuit. When A is held at -3 volts, points B and C form a short circuit.

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