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A Statistical Reliability Model for Single-Electron Threshold Logic

by

Yanjie Mao

A Thesis

Submitted to the Faculty of Graduate Studies and Research through
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in Partial Fulfillment of the Requirements for
the Degree of Master of Applied Science at the
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Abstract

As CMOS technology is predicted to reach its scaling limit in the next decade, various nanometer-scale devices have been investigated for future nano-electronics. One promising candidate is Single-Electron Tunneling (SET) technology which has benefits of its ultra-low power consumption and sub-nanometer feature size. However, shrinking device dimension has negative impact on reliability and results in increased device failure rates. In that case, reliability issue is becoming one of the biggest concerns in designing practical nanosystems.

In this thesis, we propose a statistical reliability model for individual SET logic gates with the consideration of manufacture faults and random background charges. Instead of assuming a constant failure rate for logic gates as in the previous work, we show how logic inputs affect the reliability of individual gates and the overall reliability of the whole system. In particular, we study two typical SET logic gates (2-input NOR gate and 2-input NAND gate) to quantitatively relate gate reliability to actual process variations as well as input patterns through MATLAB and SIMON. This model can be used in future CAD tools to estimate tunneling events, energy consumption, and reliability of SET-based digital logic circuits.

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Chapter 1

Introduction

1.1 Limits of CMOS Technology

Complementary metal-oxide-semiconductor (CMOS), is a major stream of integrated circuits in the recent years. During the past 25 years, Si-CMOS technology has been advancing along an exponential path of shrinking device dimensions and increasing packing density simultaneously. However, the original premise of the Moore's law reveals that integrated circuits will double in transistor counts every 18 to 24 months [1]. We take processor as an example, if it sustains the growth model in Table 1.1, the processor manufacturers would reach beyond a billion (10^9) transistors per processor core by 2007. The level of this development is not possible for today's CMOS manufacture techniques [2]. Even with the deployment of CMOS transistors

Table 1.1: Parameters of Process Adhered to Moore's Law

Process Name	P856	P858	Px60	P1262	P1264	P1266	P1268
1 st Production	1997	1999	2001	2003	2005	2007	2009
Lithography	0.25 μ m	0.18 μ m	13 μ m	90nm	65nm	45nm	32nm
Gate Length	0.20 μ m	0.13 μ m	<70nm	<50nm	<35nm	<25nm	<18nm
Wafer Size(nm)	200	200	200—300	300	300	300	300

in large numbers, the future development of traditional CMOS transistors is not possible to be carried out due to increasing power consumption concerns as well. As depicted in Figure 1.1, to maintain exponential growth in packing density, the next-generation Pentium would literally require as much power for operation as a nuclear reactor in size comparative analysis. In such a state of affairs, the continued success of the electronic industry will increasingly depend on emerging nanotechnologies which have advanced rapidly in the recent past and has shown potential for large scales of integration, specifically of an order of a trillion (10^{12}) devices in a square centimeter. Various nanometer-scale devices, such as single-electron tunneling transistors (SETs), resonant tunneling diodes (RTDs), and quantum dots and quantum cellular automata (QCA), have been investigated for future nanoelectronics epoch. In this thesis, we are focusing on Single-Electron Tunneling (SET) technology which has been extensively investigated for ultra-low power consumption and sub-nanometer feature size. So far, many SET-based circuits have been experimentally demonstrated.

1.2 Introduction to SET Technology

The principle of SET is to use the controllable transfer of single electrons for the functioning. Although, the first observation of single electron can be traced back to the early 1920s, when Robert Millikan manipulated single electrons onto oil drops,

Figure 1.1: Power Extrapolation of Processors Following Moore's Law

the replication of feat in the solid state took until the late 1980s. Early theoretical work was done by Ben-Jacob and Gefen (1985) [3], Likharev and Zorin (1985) [4], and Averin and Likharev (1986) [5]. In 1987, Fulton and Dolan of Bell laboratories first demonstrated the feasibility of SET device [6]. Today, there is a standard procedure to build a single-electron transistor with a double angle evaporation method in the Al/AlO_2 material system [7].

1.2.1 Theoretical Background

A fundamental understanding of single-electron devices can be achieved by electrostatic in the statics. Supposing an electron is positioned closely to an uncharged metal sphere (called an island), it would feel a repulse force from the sphere. Here, the net charge Q of the system consisted of island and the electron is $-e$. Although

the fundamental charge $e = 1.6 \times 10^{-19}$ is very small on the scale of human being, it is rather strong for nanoscale. Assuming the sphere is 1nm in radius and surrounded by vacuum, the surface electric field would be remarkably large as 14MV/cm. This electrostatic repulsion is called Coulomb Blockade.

The necessary condition to observe single-electron phenomena such as Coulomb blockade is

$$E_C = \frac{e^2}{2C} > k_B T \quad (1.1)$$

where k_B is Boltzmann's constant ($k_B = 1.38 \times 10^{-23} m^2 kgs^{-2} K^{-1}$), T is the absolute temperature, C is the total capacitance of the charged island, and e is the elementary charge ($e = 1.6 \times 10^{-19}$). E_C , here, is called *Coulomb energy*.

It is obvious that the characteristic capacitance of a single-electron system has to be quite small for operation at room temperature. Assuming $T = 300K$ (room temperature), according to Equation 1.1,

$$\begin{aligned} E_C = \frac{e^2}{2C} > k_B T &\implies C < \frac{e^2}{2k_B T} \\ &= \frac{(1.6 \times 10^{-19})^2}{2 \times 1.38 \times 10^{-23} \times 300} \\ &= 3 \times 10^{-18} \\ &= 3(aF) \end{aligned} \quad (1.2)$$

Equation 1.2 interprets that in order to observe the single-electron phenomena, the capacitance of the system should be on the order of 3aF, which means, the metal sphere has to be smaller than 5nm.

The structure of Single-electron tunnel circuits normally consists islands, tunnel junctions, capacitors and ideal driven voltages. Electrons tunnel independently from island to island through tunnel junctions. The tunnel resistances must be larger than the fundamental resistance in order to localize the electrons on islands.

$$R_T > R_q = \frac{h}{e^2} \approx 25813\Omega \quad (1.3)$$

where h is Planck's constant ($h = 6.626068 \times 10^{-34} m^2 kg/s$).

An electron tunneling through a junction in the quantum scale is a stochastic process. If we define P_{error} as the probability that the desired transport does not occur, the switching delay t_d can be expressed as:

$$t_d = \frac{-\ln(P_{error})q_e R_T}{|V_j| - V_c} \quad (1.4)$$

where R_T is the tunnel resistance.

1.2.2 Fabrication Limitation

Over the past few years, there has been rapid progress in the fabrication of the single-electron devices. Table 1.2 shows some single-electron transistors with different manufacture methods.

Nevertheless, the technology of fabrication of single-electron devices is still in its infancy. There is still a large gap between the laboratory and industry fabrication.

Implementation of SET devices requires a fabrication of very small conducting particles, and their accurate positioning with respect to electrons. However, the

Table 1.2: Some Single-Electron Transistors [8]

<i>Materials (Island, Barrier)</i>	<i>Fabrication Method</i>
Al, AlO_x	Evaporation through an e-beam-formed mask [9]
CdSe; organics	Nanocrystal binding to prepatterned Au electrodes [10]
Al, AlO_x	Evaporation on a Si_3N_4 membrane with a nm-scale orifice [11]
Ti; Si	Metal deposition on prepatterned silicon substrates [12]
Carboran molecule	E-beam patterned, thin-film gate; STM electrode [13]
Si, SiO_2	E-beam patterning + oxidation of a SIMOX layer [14]
Nb, NbO_x	Anodic oxidation using scanning probe [15]

technology for tight control of dimensions is not achievable at present. Although current nano-fabrication technologies have made possible small SET devices, the time for fabricating large SET circuits is still expected to be several decades away.

Further more, largely uncontrollable charge fluctuations, so-called random background charges, are a major obstacle for real world applications. Impurities and trapped electrons in the substrate induce charge on islands. Those unexpected charges usually destroy the correct function of the device. A single impurity electron located in an unanticipated position is possible to change the desired device behavior. As far as today's processing techniques, it is not able to control the purity of materials enough to meet conditions suitable for SET device production.

Under these circumstance, simulators are largely used for verification of proposed circuits instead of real fabrication. In this thesis, simulations were done with SIMON (SIMulation Of Nanostructures) [16].

1.3 Reliability Issue of SET Technology

Nano-scale devices are more sensitive to a variety of random noises including the SET devices. As mentioned above, it is imagined that certain amount of charges (random background charges) would appear on nodes of SET devices during the fabrication process. These charges generate a biased voltage contributing to the total voltage across the SET device. The logic behavior could fail in that event and the circuit becomes less reliable. For that reason, reliability turns to be one of the biggest concerns in designing practical nano-systems.

Progress in research work on reliability issues of nano-electronic circuits involves two aspects. One is reliability evaluation and analysis. The other one is reliability improvement.

Reliability analysis refers to techniques for estimating circuit reliability, or finding acceptable error bounds of individual devices for reliable operation of the overall circuit. Among these techniques are Markov model [17], Markov random fields (MRF) [18], Bayesian formalism [19], probabilistic transfer matrix (PTM) [20], probabilistic gate model (PGM) and bifurcation method [21].

Reliability improvement, on the other hand, is to use various architectures or new encoding techniques for increased reliability. Modular redundancy is such a typical example [22] [23].

1.4 A New Statistical Reliability Model of SET Technology

In most previous work, people analyze the reliability of SET circuit by assuming a constant value of failure rate which is not suitable in practise. The incorrect assumptions lead to an improper result, and then turn into an inaccuracy guidelines for circuit designers.

In this thesis, we evaluate the reliability of SET-based logic gates by presenting a statistical model which takes into account the process variations (especially random background charges) and input patterns. By indicating the reliability of a gate is not independent of other gates in the circuit but affected by all its fan-ins, we set up a relationship between process variations and the error bound for reliable operations. Those results serve as an important line for researchers and circuit designers. Moreover, the general method can be applied to other gates and other nano-scale technologies although only SET-based 2-input NOR and 2-input NAND logic gates are discussed in this thesis.

1.5 Organization of Thesis

The organization of this thesis is as follows.

Chapter 2 is focused on the design of threshold logic functions in SET logic gates with the tunnel junctions' specific behavior. The linear threshold logic gate's structure is introduced here. The experiment subjects 2-input NOR gate and 2-input NAND gate are dissected here.

Chapter 3 is devoted to the experiment of reliability of 2-input NOR gate and 2-input NAND gate. Given two assumptions of process variations and correlation of the two inputs, we conduct a particular experiment to see how the reliability of the 2-input NOR gate and 2-input NAND gate depend on random noises as well as input patterns. In the later part of the chapter, we propose our statistical model of 2-input NOR gate and 2-input NAND gate from the regression method, followed by the discussion on K -input gates.

In Chapter 4, bifurcation analysis is provided for finding out the error bound of 2-input NAND gate and 2-input NOR gate. K -input gates and time complexity of the experiment are discussed later.

Chapter 5 comments on the future work and applications.

Chapter 6 is the conclusion part.

Chapter 2

Threshold Logic Gate

Originally, Threshold Logic Unit is an idea from neuron network as the origin of artificial neuron. It is first proposed by Warren McCulloch and Walter Pitts [24] in 1943. It employs a threshold or step function taking on the values of 1 or 0 only.

By comparing the SET tunnel junction's specific behavior with the threshold logic unit, C. Lageweg applied it to the logic operations of SET [26]. The combination of these two opened up a new world in SET.

Figure 2.1: Single-Electron Box

2.1 Single-Electron Box

The so-called Single-Electron Box is an example of electrons tunneling. It consists of a tunnel junction in series with a true capacitor. The single-electron box has been the subject of numerous experimental and theoretical research, since it is a good circuit element to exhibit Coulomb blockade phenomena. The first experimental realization of a single-electron box was achieved by Lafarge et al [25].

2.1.1 Theoretical Background of Single-Electron Box

In Single-Electron Box, the tunnel junction is considered as a leaky capacitor. An electron needs an adequate energy or voltage threshold to tunnel from one plate of the capacitor to the other side. The critical voltage in Figure 2.1 is a judgement to decide whether the tunnel event is possible.

Suppose the tunnel junction with a capacitance of C_j and the remainder of the circuit has an equivalent capacitance of C_o in the C_j 's perspective. The critical voltage V_c for the junction is:

$$V_c = \frac{e}{2(C_j + C_e)} \quad (2.1)$$

In Equation 2.1, as well as in the remainder of this discussion, the charge of the electron is referred to as $e = 1.6 \times 10^{-19}$. Strictly speaking, it is not correct since the quantum of an electron is a negative value. However, it is much more convenient to consider it as positive. In this thesis, the true negative value is only taken into consideration when talking about the direction of the tunneling.

Generally speaking, if we define the voltage across a junction as V_j , a tunnel event will occur through this junction if and only if

$$|V_j| \geq V_C \quad (2.2)$$

If $|V_j| < V_C$ for all junctions, the tunnel event cannot occur. We call that the circuit is in a *stable state*. The voltage of each component is resulting from the dissipation of the input voltage source, so each stable state determines a new output value. We restrict the number of possible stable states to two (“1” and “0” or “ON” and “OFF”) based on the Boolean input and output logic we are using in our research.

2.1.2 Mathematics in Single-Electron Box

In Figure 2.1, the node (island) between the tunnel junction C_j and the true capacitor C_o is considered as a node containing j electrons.

When a tunnel event happens, electron can be added or removed from the island through tunnel junctions. When $j = 0$, the charge on the island is 0. In the microscopic view, the number of protons is the same as the electrons, which is so-called

electrical equilibrium. If j is smaller than 0, j electrons were removed from the island. Since the electron has a negative charge, $j < 0$ means that a positive charge is present on the island. Other if $j > 0$, j electrons were added to the island, and there is a negative charge present on the island.

The critical voltage V_c of the tunnel junction can be expressed as:

$$V_c = \frac{e}{2(C_j + C_o)} \quad (2.3)$$

The voltage V_j (Figure 2.1) across the tunnel junction is:

$$V_j = V_{in} \cdot \frac{\frac{1}{C_j}}{\frac{1}{C_j} + \frac{1}{C_o}} + \frac{je}{C_j + C_o} = \frac{V_{in}C_o}{C_j + C_o} + \frac{je}{C_j + C_o} \quad (2.4)$$

In Equation 2.4, the first item is due to capacitive division of the input voltage V_{in} over the capacitances C_j and C_o . The second item is the voltage resulting from the je charges on island divided by the total capacitance between the island and ground.

The output of the circuit is:

$$V_{out} = V_{in} - V_j = \frac{V_{in}C_j}{C_j + C_o} - \frac{je}{C_j + C_o} \quad (2.5)$$

The circuit is in a stable state when $|V_j| < V_c$. Combining Equation 2.3 and Equation 2.4 leads Equation 2.6.

$$\begin{aligned}
 |V_j| < V_c &\Rightarrow \left| \frac{V_{in}C_o}{C_j + C_o} + \frac{je}{C_j + C_o} \right| < \frac{e}{2(C_j + C_o)} \\
 &\Rightarrow -\frac{e}{2(C_j + C_o)} < \frac{V_{in}C_o}{C_j + C_o} + \frac{je}{C_j + C_o} < \frac{e}{2(C_j + C_o)} \\
 &\Rightarrow -\frac{e - 2je}{2C_o} < V_{in} < \frac{e - 2je}{2C_o}
 \end{aligned} \tag{2.6}$$

Therefore, for any value of V_{in} , the circuit could reach a stable state with specific j satisfying the above relation.

The gradual increase or decrease of the input voltage V_{in} from a stable state leads a similar increase or decrease of the output value in the circuit. Supposing the input voltage V_{in} increases from zero, the voltage across the junction V_j will eventually reach the tunnel event point when its absolute value is larger than V_c . In this case, an electron tunnels through the junction from one plate towards the other side. For a positive input voltage, the electron always tunnels away from island, resulting in a sudden increase of the island voltage (V_{out}). For a negative input voltage, the electron always tunnels towards island, resulting in a sudden decrease of the island voltage (V_{out}).

The $V_{out} \sim V_{in}$ transfer function is displayed in Figure 2.2. Here, the sudden change in output voltage is referred to as

$$V_{jump} = \frac{e}{C_j + C_o} \tag{2.7}$$

The increasing voltage range corresponding to a stable state is

$$V_{rise} = \frac{C_j e}{C_o(C_j + C_o)} \tag{2.8}$$

Figure 2.2: Transfer Function of Single-Electron Box

The detailed calculation is as follows:

According to Equation 2.6

$$\begin{aligned}
 j = 0 & \Rightarrow \frac{-e}{2C_o} < V_{in} < \frac{e}{2C_o} \\
 V_{out,j=0} &= \frac{C_j}{C_j + C_o} \cdot V_{in}
 \end{aligned} \tag{2.9}$$

$$\begin{aligned}
 j = -1 & \Rightarrow \frac{e}{2C_o} < V_{in} < \frac{3e}{2C_o} \\
 V_{out,j=-1} &= \frac{C_j}{C_j + C_o} \cdot V_{in} + \frac{e}{C_j + C_o}
 \end{aligned} \tag{2.10}$$

The V_{jump} and V_{rise} are calculated as follows:

$$\begin{aligned} V_{jump} &= V_{(out,j=-1,V_{in}=e/2C_o)} - V_{(out,j=0,V_{in}=e/2C_o)} \\ &= \frac{e}{C_j + C_o} \end{aligned} \quad (2.11)$$

$$\begin{aligned} V_{rise} &= V_{(out,j=-1,V_{in}=3e/2C_o)} - V_{(out,j=-1,V_{in}=e/2C_o)} \\ &= \frac{C_j}{C_j + C_o} \cdot \frac{3e}{2C_o} + \frac{e}{C_j + C_o} - \frac{C_j}{C_j + C_o} \cdot \frac{e}{2C_o} - \frac{e}{C_j + C_o} \\ &= \frac{C_j e}{C_o(C_j + C_o)} \end{aligned} \quad (2.12)$$

The ratio of V_{jump} and V_{rise} is

$$\frac{V_{jump}}{V_{rise}} = \frac{\frac{e}{C_j + C_o}}{\frac{C_j e}{C_o(C_j + C_o)}} = \frac{C_o}{C_j} \quad (2.13)$$

If $V_{jump} \gg V_{rise}$, the transfer junction curve regresses to a shape of a staircase. In that condition, $C_o \gg C_j$.

The sharp discontinuities of the staircase transfer function of Single-Electron Box indicate two facets. They are key points for creating a bridge between threshold logic theory and single-electron tunneling technology.

First, if the input voltage is limited to an small area around a discontinuity point, the point can be used as a threshold.

Second, if we apply an additional voltage to bias the circuit so that its state is close to a discontinuity point, only a small voltage can generate a large swing in the output voltage as an amplifier. The ratio over the output and the input is called amplification factor.

Figure 2.3: Transfer Function of Single-Electron Box when $V_{jump} \gg V_{rise}$

Given the characteristics of the Single-Electron Box, we can extend this circuit to perform linear threshold logic.

2.2 SET Linear Threshold Gate

2.2.1 Mathematics on SET Linear Threshold Gate

Threshold logic gates are devices which are able to compute any linear separable Boolean function relying on the following equations. These equations are derived from the step function in threshold logic unit in neuron network. The output $G(x)$ of this transfer function is binary of 1 and 0, depending on whether the input meets a specified threshold. If the operation meets the threshold, the output is set to be one. Otherwise, it is zero.

$$G(x) = \text{sgn}\{F(x)\} = \begin{cases} 0 & \text{if } F(x) < 0 \\ 1 & \text{if } F(x) \geq 0 \end{cases} \quad (2.14)$$

$$F(x) = \sum_{i=1}^n \omega_i x_i - \psi \quad (2.15)$$

where x_i is the Boolean inputs and ω_i is the corresponding integer weights.

The linear threshold gate performs a comparison between the weighted sum of the inputs $\sum_{i=1}^n \omega_i x_i$ and the threshold value ψ . If the weighted sum of inputs is greater or equal to the threshold, the gate produces a logic being 1. Otherwise, it is 0.

Single-Electron Box discussed in the previous section is following this threshold behavior. From the clues of the two indications mentioned above, the strong discontinuity point is referred to the gap between one stable state and its neighboring state. We choose two neighboring states and the discontinuity point between them. The circuit operation point is set to be in the area of the discontinuity point. The circuit can only produce two distinct values. By setting a threshold between these two values, we can make these two 1 and 0.

We choose $V_{in} = e/2C_o$ (Figure 2.3) as the discontinuity point and employ V^- and V^+ for the two desired values. The values of V^- and V^+ are $V^- = V_{rise} \approx 0$, and $V^+ = V_{jump}$.

Broadly speaking, the weights (ω_i) associated with the inputs of the linear threshold gate should be allowed both positive and negative values. However, most current implementations of the linear threshold gate only allow for positive weights [27] [28]. Anyhow, it is a limitation for the efficient implementation of the threshold gate algorithms [10]. To satisfy the wide application, the SET based implementation allows for positive and negative weights as well.

Figure 2.4: The N-Input Linear Threshold Gate

Figure 2.4 is the main structure of threshold linear logic which is implemented with Single-Electron Box as basis (Equation 2.14 and Equation 2.15). The basic two elements tunnel junction C_j and output capacitance C_o are adopted from Single-Electron Box. The input voltages $V^p = \{V_1^p, V_2^p, \dots, V_r^p\}$ are weighted by their corresponding capacitors $C^p = \{C_1^p, C_2^p, \dots, C_r^p\}$. The composite output is an added voltage across the tunnel junction. The input voltages $V^n = \{V_1^n, V_2^n, \dots, V_s^n\}$ are weighted by their corresponding capacitors $C^n = \{C_1^n, C_2^n, \dots, C_s^n\}$. The composite output is a subtract voltage across the tunnel junction. Since the tunnel junction voltage V_j should be larger than the critical voltage V_c , we set a biased voltage V_b with the corresponding weight C_b to adjust it in order to meet threshold value ψ .

For the purpose of making the following discussion clear and readability, we set the following notations from Lageweg's paper [26].

$$C_{\Sigma}^p = C_b + \sum_{k=1}^r C_k^p \quad (2.16)$$

$$C_{\Sigma}^n = C_o + \sum_{k=1}^s C_k^n \quad (2.17)$$

$$C_{\tau} = C_{\Sigma}^p C_j + C_{\Sigma}^p C_{\Sigma}^n + C_j C_{\Sigma}^n \quad (2.18)$$

Then Figure 2.4 regresses to Figure 2.5 which looks like Single-Electron Box. It is a circuit with a series of capacitors C_{Σ}^p , C_j and C_{Σ}^n . The C_{τ} is the sum of each two items' product.

To evaluate of this circuit, V_c is needed to be calculated first of all. According to Equation 2.3, we get V_c in this case. From C_j 's perspective, C_{Σ}^p and C_{Σ}^n are parallel and the equivalence of these two capacitors are

$$V_{eq(C_{\Sigma}^p, C_{\Sigma}^n)} = \frac{C_{\Sigma}^p C_{\Sigma}^n}{C_{\Sigma}^p + C_{\Sigma}^n} \quad (2.19)$$

$$V_c = \frac{e}{2(C_j + C_{eq})} = \frac{e}{2(C_j + \frac{C_{\Sigma}^p C_{\Sigma}^n}{C_{\Sigma}^p + C_{\Sigma}^n})} = \frac{(C_{\Sigma}^p + C_{\Sigma}^n)e}{2C_{\tau}} \quad (2.20)$$

We refer the voltage at node x as V_x . According to the Figure 2.6, the composite of the input voltage V^p and the biased voltage V_b on voltage V_x is

$$V_x(V_b, V^p) = \frac{(C_j + C_{\Sigma}^n)(C_b V_b + \sum_{k=1}^r C_k^p V_k^p)}{C_{\tau}} \quad (2.21)$$

The composite of the input voltage V^p and the biased voltage V_b on the V_j across tunnel junction is

Figure 2.5: The N-Input Linear Threshold Gate Regresses to Single-Electron Box

Figure 2.6: The Equivalent Capacitance in V_x 's View

$$V_j(V_b, V^p) = \frac{C_\Sigma^n (C_b V_b + \sum_{k=1}^r C_k^p V_k^p)}{C_\tau} \quad (2.22)$$

The composite of the input voltage V^n on the V_j across tunnel junction is

$$V_j(V^n) = \frac{-C_\Sigma^p \sum_{k=1}^s C_k^n V_k^n}{C_\tau} \quad (2.23)$$

Combing Equation 2.22 and Equation 2.23 leads to the composite of V_b , V^p and V^n on V_j across tunnel junction is as follows:

$$V_j = \frac{C_\Sigma^n \sum_{k=1}^r C_k^p V_k^p}{C_\tau} - \frac{C_\Sigma^p \sum_{k=1}^s C_k^n V_k^n}{C_\tau} + \frac{C_\Sigma^n C_b V_b}{C_\tau} \quad (2.24)$$

As we talked before, the activity about the electron is determined by the comparison of V_j and V_c . If $V_j > V_c$, the electron will tunnel in the arrow's direction in Figure 2.4.

Presently, we could formulate the function $F(x)$ in Equation 2.15 for the implementation of SET linear threshold logic.

$$F(x) = V_j(V_b, V^p, V^n) - V_c \quad (2.25)$$

Substituting Equation 2.3 and Equation 2.15, we conclude Equation 2.28

$$\begin{aligned} F(x) &= V_j(V_b, V^p, V^n) - V_c \\ &= \frac{C_\Sigma^n \sum_{k=1}^r C_k^p V_k^p}{C_\tau} - \frac{C_\Sigma^p \sum_{k=1}^s C_k^n V_k^n}{C_\tau} + \frac{C_\Sigma^n C_b V_b}{C_\tau} - \frac{(C_\Sigma^p + C_\Sigma^n)e}{2C_\tau} \end{aligned} \quad (2.26)$$

Since we only focus on the sign of $F(x)$, we simply ignore C_τ .

$$F(x) = C_\Sigma^n \sum_{k=1}^r C_k^p V_k^p - C_\Sigma^p \sum_{k=1}^s C_k^n V_k^n + C_\Sigma^n C_b V_b - \frac{1}{2}(C_\Sigma^p + C_\Sigma^n)e \quad (2.27)$$

We take part of $F(x)$ as ψ

$$F(x) = C_\Sigma^n \sum_{k=1}^r C_k^p V_k^p - C_\Sigma^p \sum_{k=1}^s C_k^n V_k^n - \psi \quad (2.28)$$

$$\psi = \frac{1}{2}(C_\Sigma^p + C_\Sigma^n)e - C_\Sigma^n C_b V_b \quad (2.29)$$

Comparing Equation 2.15 and Equation 2.28, we find that the corresponding weights ω_i are realized as C^n or C^p . To be more precise, the positive ω_i is realized as C^p (p means positive); the negative ω_i is realized as C^n (n means negative). What's more, $F(x)$ has nothing to do with the junction's capacitance.

In the same way, the inputs x_i are realized as V^n or V^p . To be more precise, the positive x_i is realized as V^p (p means positive); the negative x_i is realized as V^n (n means negative).

Equation 2.29, indicates that the threshold is affected by the biased voltage V_b (b means biased) and biased capacitance C_b .

To sum up, the presented circuit depicted in Figure 2.4 implements an n -input linear threshold gate. The circuit is consisted of one external voltage (V_b) and $n + 2$ true capacitors (n input capacitors, C_b and C_o) and the corresponding positive and negative input voltages.

After finishing talking about the structure of the threshold logic circuit, we change our views to the output value.

If one electron tunnels through the junction in the arrow's direction (Figure 2.4), it increases a $-e$ voltage on node x (V_x). The effect is

$$\delta V_x = \frac{-e(C_j + C_\Sigma^n)}{C_\tau} \quad (2.30)$$

$$\delta q_x = -e \quad (2.31)$$

Due to the voltage division, the changed voltage on V_o is

$$\delta V_o(x) = \frac{-eC_j}{C_\tau} \quad (2.32)$$

$$\delta q_x = -e \quad (2.33)$$

Likewise, when one electron tunnels through the junction in the arrow's direction (Figure 2.4), it increases a $+e$ voltage on node y (V_y). The effect is

$$\delta V_o(y) = \frac{e(C_j + C_\Sigma^p)}{C_\tau} \quad (2.34)$$

$$\delta q_y = e \quad (2.35)$$

To sum up, if one electron tunnels in the arrow's way, the composite effect on the output voltage V_o is

$$\delta V_o(1e) = \delta V_o(x) + \delta V_o(y) = \frac{-eC_j}{C_\tau} + \frac{e(C_j + C_\Sigma^p)}{C_\tau} = \frac{eC_\Sigma^p}{C_\tau} \quad (2.36)$$

Figure 2.7: Diagram of 2-input NOR Gate

Table 2.1: Truth Table for 2-input NOR Gate

A	B	Z
0	0	1
1	0	0
0	1	0
1	1	0

2.2.2 Circuit Examples for SET Threshold Logic

In this section, we first present a SET-based threshold logic implementation of 2-input NOR Gate (Figure 2.7). The 2-input NAND Gate and K-input gate will be discussed later. By using threshold logic, the 2-input NOR gate can be implemented with four capacitors (C_1, C_2, C_b, C_o) and one tunnel junction in two level logic (0 and 1).

The truth table for 2-input NOR gate is Table 2.1 by supposing the two inputs are A and B and the output is Z .

The corresponding equations are as follows:

$$z = \text{sgn}\{-a - b + 0.5\} \quad (2.37)$$

When assigning values to the components in the circuit, we assume the ratio of the capacitors could realize the input weights (ω_i). Comparing Equation 2.37 and Equation 2.28. We get the following relations for the weights ω_i :

$$C_k^p = 0 \quad (k = 1, 2, \dots) \quad (2.38)$$

$$C_\Sigma^p C_1^n = C_\Sigma^p C_2^n \quad (2.39)$$

$$C_\Sigma^p = C_b \quad (2.40)$$

$$C_\Sigma^n = C_1^n + C_2^n + C_o \quad (2.41)$$

Therefore, we get the relation with C_1^p and C_2^p

$$C_1^p = C_2^p \quad (2.42)$$

It is easy to understand, since the two inputs are equivalent in logic.

We follow Lageweg's unit capacitance [26], and set the capacitances C_1^p and C_2^p the same with his.

$$C_1^p = 0.5aF \quad (2.43)$$

$$C_2^p = 0.5aF \quad (2.44)$$

where $1aF = 1 \times 10^{-18}F$.

The output capacitance C_o is

$$C_o = 9aF \quad (2.45)$$

The biased voltage V_b is set as $16mV$ for the simplification and practice.

$$V_b = \frac{0.1e}{1aF} = 0.016V = 16mV \quad (2.46)$$

To correspond with V_b , the inputs A being 1 (V_1) and B being 1 (V_2) are also set as $16mV$.

$$V_1 = \frac{0.1e}{1aF} = 0.016V = 16mV \quad (2.47)$$

$$V_2 = \frac{0.1e}{1aF} = 0.016V = 16mV \quad (2.48)$$

By observing the truth table, we find that when $A = B = 0$, the output $Z = 1$. In other words, $F(x) > 0$.

We can calculate the $F(x)$ in that case, after substituting the capacitances and voltages we have set.

$$\begin{aligned}
& F(C_1^n = C_2^n = 0.5aF, C_o = 9aF, V_1^n = V_2^n = 0, V_b = 0.1e/1aF) \\
&= C_\Sigma^n \sum_{k=1}^r C_k^p V_k^p - C_\Sigma^p \sum_{k=1}^s C_k^n V_k^n - \frac{1}{2}(C_\Sigma^p + C_\Sigma^n)e + C_\Sigma^n \\
&= -C_b(C_1^n V_1^n + C_2^n V_2^n) - \frac{1}{2}(C_b + C_1^n + C_2^n + C_o)e + (C_1^n + C_2^n + C_o)C_b V_b \\
&= -C_b \times 0 - \frac{1}{2}(C_b + 0.5aF + 0.5aF + 9aF)e \\
&\quad + (0.5aF + 0.5aF + 9aF) \times C_b \times 0.1e/1aF > 0 \tag{2.49}
\end{aligned}$$

$$\Rightarrow C_b > 10aF \tag{2.50}$$

If there is one input being 1, for instance, $A = 1$, the output is going to be $Z = 0$.
So $F(x) < 0$

$$\begin{aligned}
& F(C_1^n = C_2^n = 0.5aF, C_o = 9aF, V_1^n = 0.1e/1aF, V_2^n = 0, V_b = 0.1e/1aF) \\
&= C_\Sigma^n \sum_{k=1}^r C_k^p V_k^p - C_\Sigma^p \sum_{k=1}^s C_k^n V_k^n - \frac{1}{2}(C_\Sigma^p + C_\Sigma^n)e + C_\Sigma^n \\
&= -C_b(C_1^n V_1^n + C_2^n V_2^n) - \frac{1}{2}(C_b + C_1^n + C_2^n + C_o)e + (C_1^n + C_2^n + C_o)C_b V_b \\
&= -C_b \times (0.5aF \times 1) - \frac{1}{2}(C_b + 0.5aF + 0.5aF + 9aF)e \\
&\quad + (0.5aF + 0.5aF + 9aF) \times C_b \times 0.1e/1aF < 0 \tag{2.51}
\end{aligned}$$

$$\Rightarrow C_b < 11.11aF \tag{2.52}$$

Thus, for the function 2-input NOR gate, C_b has to be picked up from

$$10aF < C_b < 11.11aF \tag{2.53}$$

Finally, we choose

$$C_b = \frac{1}{2}(10 + 11.11) \approx 10.6 \quad (2.54)$$

Only when the value of the C_b is in the above range, the circuit works as a 2-input NOR gate. Due to the manufacture problems, the C_b could not be accurate but has a deviation. Since the deviation is supposed to be equivalent for the positive and negative side, C_b is chosen as the middle value in the range, which makes it more tolerant. The following C_b for the other gates is chosen following this law as well.

To verify the parameters, we use SIMON as Figure 2.8. The two in the first line provide the two inputs A and B . And, the third one verifies the output Z .

The curves in Figure 2.8 correspond to the Table. 2.1 very well.

So far, we have had all the inputs and capacitance values for the 2-input NOR gate. The conclusion is as follows.

$$\begin{aligned} V_b &= 16mV \\ C_1 &= C_2 = 0.5aF, C_o = 9aF, C_b = 10.6aF \\ C_j &= 1.0aF, R_j = 100k\Omega \end{aligned} \quad (2.55)$$

where the value of C_j and R_j are adopted from SIMON. These parameters are called *standard values* for the following discussion.

We do the similar procedure and get the values for 2-input NAND gate. Different from the 2-input NOR gate, When $A = B = 1$, the output value is $Z = 0$, otherwise, it is $Z = 1$.

Figure 2.8: Simulation Result of 2-input NOR Gate by SIMON

Figure 2.9: Simulation Result of 2-input NAND Gate by SIMON

Table 2.2: Truth Table for 2-input NAND Gate

A	B	Z
0	0	1
1	0	1
0	1	1
1	1	0

The corresponding equation is

$$z = \text{sgn}\{-a - b + 1.5\} \quad (2.56)$$

For the 2-input NAND gate, we use SIMON as in Figure 2.9. Table 2.2) provides the truth table of 2-input NAND gate.

$$C_b = 11.8aF \quad (2.57)$$

Chapter 3

Reliability Issue on SET

A variety of nano-scale devices are currently being used to design digital logic. However, the random noises (such as process variations and random background charges) and physical failures with devices and interconnects may lead to faulty logic behaviors. When this happens with a wrong logic output, the logic gate is said to fail. If a logic gate has a failure probability ϵ , it is said to have a reliability r , where $r = 1 - \epsilon$. In this section, we look at the reliability model for SET-based logic gates by showing the process of experimentally obtaining their reliability. The proposed model turns out to be approximate with statistical nature.

Figure 3.1: Noise on Capacitances and Islands of 2-input NOR Gate

3.1 Experiment on Reliability of 2-input NOR Gate

3.1.1 Assumptions of the Experiment

As mentioned before, the reliability is not a constant value but varies with the environment. In order to see how the reliability of the 2-input NOR gate depends on random noises as well as input patterns, we conduct a particular experiment with the following two assumptions.

- (1) The noises from all capacitors and islands (Figure 3.1) are modeled as a *normal distribution* with mean μ and variance σ^2 .

The assumption is based on *the central limit theorem*, which is a set of weak-convergence results in probability theory. It states that if the sum of the variables has a finite variance, then it will be approximately normally distributed, following a normal distribution. Since many real processes generate distributions with finite variance, this reveals the universality of the normal probability distribution.

The probability density function of the normal distribution is

$$f(z; \mu, \sigma) = \frac{1}{\sigma\sqrt{2\pi}} \exp\left(-\frac{(z - \mu)^2}{2\sigma^2}\right) \quad (3.1)$$

where z is a random variable.

In case of capacitance, z is a random value of capacitance with mean μ being its standard value.

In case of islands, z represents the value of random background charge with mean $\mu = 0$. The value of σ can be selected based on the varying range of random variable.

The normal distribution function is effective from negative infinity to positive infinity. In industry, we choose part of this function instead of the whole one.

In Figure 3.2, about 68% of values drawn from a standard normal distribution are within 1 standard deviation (1σ) away from the mean; about 95% of the values are within two standard deviations (2σ) and about 99.7% lie within 3 standard deviations (3σ). That is so-called *3 σ control limit*, which is broadly used in industry.

Suppose the noise on the capacitance is within the range $\pm\eta \times 100\%$, which means the capacitance is picked up during the range $[C_{std} - \eta C_{std}, C_{std} + \eta C_{std}]$ following the normal distribution. According to the 3σ control limit,

Figure 3.2: 3σ control limit

$$\begin{aligned} \pm\eta \times 100\% \times C_{std} &= \pm 3 \times \sigma_c \\ \sigma_c &= \frac{\eta C_{std}}{3} \end{aligned} \quad (3.2)$$

where C_{std} is the standard value of capacitance.

In case of the islands, we set the noise is within the range $\pm\eta \times e$, and the random background charge on the island is within $[-\eta e, \eta e]$, so

$$\begin{aligned} \pm\eta \times e &= \pm 3 \times \sigma_e \\ \sigma_e &= \frac{\eta e}{3} \end{aligned} \quad (3.3)$$

Here, η is an important parameter representing the extent of process variations, and is hence called *variation factor* thereafter.

Table 3.1: Variables in Normal Distribution

	Capacitance	Island
z	Random value of capacitance	Value of random background charge
μ	Standard value $\mu = C_{std}$	$\mu = 0$
σ	$[C_{std} - \eta C_{std}, C_{std} + \eta C_{std}]$ $\sigma = \frac{1}{3}(\eta C_{std})$	$[-\eta e, \eta e]$ $\eta = \frac{1}{3}(\eta e)$

(2) The probabilities of input voltages V_1 and V_2 being logic 1 are P_1 and P_2 , respectively, and they are independent.

The assumption reveals that there is no correlation between the inputs. If there is, P_1 and P_2 cannot be set independently. The invisible relation between the inputs will affect the experiment results.

The variables in the *p.d.f* (*probability density function*) of normal distribution are concluded in the Table 3.1.

3.1.2 Procedure of the Experiment

The experiment is done with the statistical method. The procedure is as follows:

For each certain η , we try different pairs of (P_1, P_2) (P_1 is the probability that input V_1 being 1; P_2 is the probability that input V_2 being 1). P_1 is chosen from 0 to 1 with step 0.1; P_2 is chosen from 0 to 1 with step 0.1 as well.

The value of each component in the circuit is picked up according to the above assumptions. We generate the circuit with SIMON. The process of varying the values and conducting simulations is repeated for $T = 10,000$ times. The result data are collected. Comparing the result data with the inputs, we collect the number of correct

Table 3.2: Estimated reliability r for 2-input NOR gate with $\eta = 0.04$

$P_1 \backslash P_2$	0.0	0.1	0.2	0.3	0.4	0.5	0.6	0.7	0.8	0.9	1.0
0.0	0.8810	0.8663	0.8622	0.8603	0.8510	0.8501	0.8453	0.8363	0.8265	0.8230	0.8159
0.1	0.8709	0.8754	0.8609	0.8599	0.8571	0.8513	0.8505	0.8410	0.8390	0.8386	0.8325
0.2	0.8650	0.8626	0.8643	0.8710	0.8601	0.8625	0.8522	0.8581	0.8520	0.8523	0.8554
0.3	0.8573	0.8543	0.8550	0.8640	0.8605	0.8661	0.8618	0.8676	0.8653	0.8727	0.8652
0.4	0.8521	0.8536	0.8574	0.8657	0.8708	0.8705	0.8837	0.8766	0.8804	0.8870	0.8923
0.5	0.8418	0.8576	0.8577	0.8607	0.8700	0.8772	0.8828	0.8906	0.8890	0.9054	0.9033
0.6	0.8366	0.8470	0.8539	0.8616	0.8714	0.8813	0.8913	0.8976	0.9036	0.9206	0.9251
0.7	0.8360	0.8463	0.8600	0.8649	0.8728	0.8907	0.9047	0.9080	0.9251	0.9314	0.9442
0.8	0.8238	0.8413	0.8597	0.8610	0.8812	0.8911	0.9025	0.9246	0.9333	0.9481	0.9596
0.9	0.8299	0.8365	0.8500	0.8661	0.8862	0.9009	0.9212	0.9296	0.9505	0.9661	0.9814
1.0	0.8163	0.8264	0.8476	0.8627	0.8866	0.9061	0.9238	0.9422	0.9607	0.9808	0.9981

outputs as M , then the ratio M/T is the estimate of the gate reliability r .

The above evaluation process is repeated for different values of η from 0 to 0.50 with step 0.01 as well as different pairs of (P_1, P_2) . The gate reliability is generally expressed in terms of η , P_1 and P_2 . Table 3.2 shows one group of the estimated reliabilities with a specific value of $\eta = 0.04$. Figure 3.3 plots the values.

3.2 Statistical Model for Gate Reliability

Observation from the Table 3.2 or Figure 3.3, it is difficult to find out an explicit expression $r = r(\eta, P_1, P_2)$. Therefore, we resort to the regression method as follows. For a given value of η , the two models are used for the 2-input NOR gate.

$$r = \alpha_0 + \alpha_1(P_1 + P_2) + \alpha_2 P_1 P_2 \quad (3.4)$$

$$r = \alpha'_0 + \alpha'_1(P_1 + P_2) + \alpha'_2 P_1 P_2 + \alpha'_3(P_1^2 + P_2^2) \quad (3.5)$$

where the coefficients α_i ($i=0, 1$ and 2) and α_j ($j=0, 1, 2$ and 3) are constants. These values are obtained with the *least square method* from Table 3.2.

Figure 3.3: Reliability vs. Input Probabilities for 2-input NOR gate with $\eta = 0.04$

For the α_i ($i=0, 1$ and 2) in Equation 3.4.

$$\begin{aligned}\alpha_0 &= 0.8788 \\ \alpha_1 &= -0.0645 \\ \alpha_2 &= 0.2486\end{aligned}\tag{3.6}$$

The maximum error for this model is 0.8%.

For the α_j ($j=0, 1, 2$ and 3) in Equation 3.5.

$$\begin{aligned}
 \alpha'_0 &= 0.8790 \\
 \alpha'_1 &= -0.0652 \\
 \alpha'_2 &= 0.2485 \\
 \alpha'_3 &= 0.0007
 \end{aligned} \tag{3.7}$$

The maximum error for this model is 0.79%.

Compared with these two models, the first one is simpler and in good agreement with the experimental data. Therefore, the first model is chosen for the following discussion.

When taking into account the role of η , the first model can be generally rewritten as

$$r = r(\eta, P_1, P_2) = \alpha_0(\eta) + \alpha_1(\eta)(P_1 + P_2) + \alpha_2(\eta)P_1P_2 \tag{3.8}$$

where $\alpha_0(\eta)$, $\alpha_1(\eta)$, $\alpha_2(\eta)$ are plotted in Figure 3.4, Figure 3.5 and Figure 3.6 based on our experimental results.

3.3 Reliability Model for Other Gates

The similar experiment can be conducted for any type of gates with multiple inputs.

Figure 3.4: Reliability model coefficient $\alpha_0(\eta)$ for 2-input NOR gate

Figure 3.5: Reliability model coefficient $\alpha_1(\eta)$ for 2-input NOR gate

Figure 3.6: Reliability model coefficient $\alpha_2(\eta)$ for 2-input NOR gate

Figure 3.7: Diagram of 2-input NAND Gate

3.3.1 2-input NAND Gate

The parameters of 2-input NAND gate can be implemented using Figure 2.4 with different parameters.

$$\begin{aligned}V_b &= 16mV \\C_1 &= C_2 = 0.5aF \\C_o &= 9aF \\C_b &= 11.8aF \\C_j &= 1.0aF, R_j = 100k\Omega\end{aligned}\tag{3.9}$$

By performing the reliability experiment, we observe similar properties of the reliability r with NAND gate. The reliability model is

$$r = r(\eta, P_1, P_2) = \beta_0(\eta) + \beta_1(\eta)(P_1 + P_2) + \beta_2(\eta)P_1P_2\tag{3.10}$$

where the coefficients $\beta_0(\eta)$, $\beta_1(\eta)$ and $\beta_2(\eta)$ are obtained again through the experiments, as shown in Figure 3.9, Figure 3.10 and Figure 3.11

3.3.2 K-input Gates

Besides 2-input gates, we apply the statistical method to multiple input gates.

In general, for K-input gates, the statistical reliability model can be approximately expressed as

Figure 3.8: Circuit of 2-Input NAND Gate in SIMON

Figure 3.9: Reliability model coefficient $\beta_0(\eta)$ for 2-input NAND gate

Figure 3.10: Reliability model coefficient $\beta_1(\eta)$ for 2-input NAND gate

Figure 3.11: Reliability model coefficient $\beta_2(\eta)$ for 2-input NAND gate

$$r = r(\eta, P_1, P_2, \dots, P_k) = \gamma_0(\eta) + \gamma_1(\eta) \sum_{i=1}^K P_i + \gamma_2(\eta) \sum_{i,j,j>i}^K P_i P_j \quad (3.11)$$

where the coefficients $\gamma_0(\eta)$, $\gamma_1(\eta)$ and $\gamma_2(\eta)$ can be determined by the experiments. The maximum order of the equation is restricted to *the second order*.

For the overall discussion, we provide the 3-input NOR gate and 4-input NOR gate in the following.

For the 3-input NOR gate (Figure 3.12 and Figure 3.13), the parameters are

Figure 3.12: 3-Input NOR Gate

$$\begin{aligned}V_b &= 16mV \\C_1 &= C_2 = C_3 = 0.5aF \\C_o &= 9aF \\C_b &= 10aF \\C_j &= 1.0aF, R_j = 100k\Omega\end{aligned}\tag{3.12}$$

The simulation result from SIMON is shown in Figure 3.14. The first three are the inputs while the fourth shows the outputs.

For the 4-input NOR gate (Figure 3.15 and Figure 3.16), the parameters are

$$\begin{aligned}V_b &= 16mV \\C_1 &= C_2 = C_3 = 0.5aF \\C_o &= 9.58aF \\C_b &= 10aF \\C_j &= 1.0aF, R_j = 100k\Omega\end{aligned}\tag{3.13}$$

Figure 3.13: 3-Input NOR Gate Based on SET Threshold Logic

The simulation results from SIMON are shown in Figure 3.17. The first four are the inputs while the fifth shows the outputs.

Figure 3.14: Simulation Result of 3-Input NOR Gate by SIMON

Figure 3.15: 4-Input NOR Gate

Figure 3.16: 4-Input NOR Gate Based on SET Threshold Logic

Figure 3.17: Simulation Result of 4-Input NOR Gate by SIMON

Chapter 4

Bifurcation Analysis for SET Logic Circuits

It is obvious that if the variation factor η of an individual gate increases, the reliability would be reduced. As the η goes up, the circuit eventually becomes unreliable. Based on the above reliability models, a question raised: for what value of variation factor η , can the circuit consisting of individual gates operate reliably in a probabilistic sense? The researchers in the bifurcation analysis paper [21] answered it by assuming the failure rate of individual gate is a constant ϵ . There, the error bound for NAND gate is technically calculated as $\epsilon^* = 0.08856$. In other words, the individual NAND gate has the reliability of more than $r^* = 1 - \epsilon^* = 0.91144$ for the circuit built out of NAND gates to compute reliably with probability greater than 0.5.

However, the assumption of a constant reliability in the circuit is unrealistic. The reliability of a specific logic gate in the circuit, along with its input probabilities, determines its output probability which, as indicated in our statistical model, will change the reliability of its fan-out gates. More specifically, the same NAND gates in the circuit may have different reliabilities due to the varying probabilities at their inputs, and all these probabilities and reliabilities can also propagate throughout the circuit from its inputs to outputs. In this section, we will apply the bifurcation technique to this complex situation where r is not a constant.

Here, we use bifurcation analysis for circuit built out of the logic gates.

In mathematics, specifically in the study of dynamical systems, a bifurcation occurs when a small smooth change made to the parameter values (the bifurcation parameters) of a system causes a sudden ‘qualitative’ or topological change in the system’s long-term dynamical behavior [30]. In other words, bifurcation is the act of splitting into two branches. The bifurcation point (in this case, it is so-called error bound) is the place where something divides into two branches. In the SET logic gates, bifurcation point (error bound) is the threshold that the logic fails.

4.1 Bifurcation Analysis for Circuit Built out of NAND Gates

Assuming the two inputs of NAND gate are independent with probabilities P_1 and P_2 of their logic values being a 1, the reliability is r ($r > 0.5$) and the probability of P_o of the output V_o being a 1 is

$$P_o = r(1 - P_1 P_2) + (1 - r)P_1 P_2 = r - (2r - 1)P_1 P_2 \quad (4.1)$$

There are a few properties of P_o .

(1) When $r = 1$ and P_1, P_2 take the values either 1 or 0, Equation 4.1 regresses to the standard definition of an error-free NAND gate.

$$P_o = 1 - P_1 P_2 \quad (4.2)$$

(2) When P_1 (or P_2) is fixed, P_o linearly decreases with P_2 (or P_1).

(3)

$$\begin{aligned} \max(P_o) &= r & \text{when } P_1 = P_2 = 0 \\ \min(P_o) &= 1 - r & \text{when } P_1 = P_2 = 1 \end{aligned} \quad (4.3)$$

(4) P_o decreases fastest along $P_1 = P_2$, and hence $P_1 = P_2$ constitutes the worst case scenario.

It is because that $P_1 = P_2 = 0$ brings the maximum value of P_o . While, $P_1 = P_2 = 1$ comes out the minimum value.

In our experiment, we connect the NAND gates in series. Each output of NAND gates becomes the input to the next stage NAND gate which fits the case $P_1 = P_2 = X$. Clearly, we label a sequence of NAND gates by index $i, i = 1, 2, \dots, n, \dots$, where the output of gate i becomes the input to gate $i + 1$. Equation 4.1 regresses to a nonlinear map

$$X_{n+1} = r - (2r - 1)X_n^2 \quad (4.4)$$

The dynamic behavior of the map can be resolved by the bifurcation analysis. Mathematically, it involves the following procedure.

Given any initial value for X_0 and then iterates Equation 4.4. After a sufficient amount of iterates, the solution of the map converges to some attractor. If the map has a globally attracting fixed point solution, the recorded value of X_n all becomes the same eventually. If not, the branches of X_n declare bifurcation scenario.

Substituting the model we choose in Chapter 3 (Equation 3.8), Equation 4.4 goes to

$$X_{n+1} = f(X_n) = (\alpha_0(\eta) + 2\alpha_1(\eta)X_n + \alpha_2(\eta)X_n^2) - (2(\alpha_0(\eta) + 2\alpha_1(\eta)X_n + \alpha_2(\eta)X_n^2) - 1)X_n^2 \quad (4.5)$$

For each fixed value of η , the coefficients of X_n are constant. Equation 4.5 comes out as a fourth order one. By computing the value of X_n with $X_{n+1} = X_n$, we figure out the solution of $X_n = x_0$, to which value X_n converges.

Mathematically, this is ensured by the condition

$$|f'(x_0)| < 1 \quad (4.6)$$

When $|f'(x_0)| > 1$, x_0 loses stability with some oscillational values, which means, the system computes reliably in a probabilistic sense. This is because of the fact that for a 2-input NAND gates to function reliably, two identical inputs of 1 or 0 should output a 0 or 1, respectively. In other words, if the system remains reliable, the output should oscillate between 1 and 0, leading to the oscillation of P_o . Otherwise, if the system flows to unreliable, the output will converge to some attractor eventually, leading to a fixed value of P_o finally.

Indeed, when η is very small, the gate has high reliability and it is found that $|f'(x_0)| > 1$, indicating that the system is reliable. As η increases gradually, one can keep checking the relationship between $|f'(x)|$ and 1. Eventually, at $\eta = \eta^*$, $|f'(x)| = 1$. That is when the system fails to compute reliably.

This behavior can be interpreted as follows: any circuit built out of 2-input NAND gates with $\eta < \eta^*$ can operate reliably in a probabilistic sense. Here, η represents the range of process variations, as discussed before.

In other words, the reliability of the whole circuit has been associated with the noise parameter. This is impossible with previous work which assumes a constant failure rate for all gates in the circuit.

By using the above bifurcation on Equation 4.5 with an initial value of $\eta = 0$, we find that

$$\begin{aligned}
 \eta^* &= 0.0358 \\
 x_o &= 0.6062 \quad (|f'(x)| = 1) \\
 \alpha_0 &= 1.0000 \\
 \alpha_1 &= -0.1093 \\
 \alpha_2 &= 0.0893
 \end{aligned} \tag{4.7}$$

When $\eta = \eta^* = 0.0358$, we do the statistical experiment on this η , and collect the reliabilities for different pairs of (P_1, P_2) . The average of the reliabilities over all possible input probabilities of the NAND gate is calculated as

$$r_{avg} = r^* = 0.8960 \tag{4.8}$$

Figure 4.1: The Gate Reliability at Different Stages of NAND Gates

Compared to the traditional reliability bound of

$$1 - \epsilon^* = 1 - 0.088536 = 0.9144 \quad (4.9)$$

where ϵ^* is the error threshold given by [21] with the assumption of a constant failure rate ϵ for 2-input NAND gate.

The error bound in the traditional method is smaller than the one in our method. Based on their rules, the manufacture technology needs more restrictions than ours, which is not so necessary.

From the above bifurcation analysis, the reliabilities of different gates in the circuit keep changing from one gate to the next, and therefore X_n propagates in a different way from the traditional approach.

Figure 4.1 shows the values of reliability r_n of the i^{th} stage in the network assuming the initial input probabilities are 0.5. For instance, at $\eta = 0.03 < \eta^*$, the individual gate reliability varies from 0.9229 to 0.9820. Overall, the gate reliability increases with reduced value of η , as expected. Also, it can be clearly seen from the figure that when $\eta = 0.03 < \eta^*$, the motion of gate reliability (and hence X_n) is periodic, indicating the system can compute reliably in a probabilistic sense. When $\eta = 0.04 > \eta^*$, the gate reliability (and hence X_n) converges to a stable fixed point after the 80th stage, meaning that the value of η is too large for the system to function reliably in general from a probabilistic point of view.

4.2 Bifurcation Analysis for Circuits Built out of 2-input NOR Gates

Assuming the two inputs of NOR gate are independent with probabilities P_1 and P_2 of their logic values being a 1, the reliability is r ($r > 0.5$) and the probability of P_o of the output V_o being a 1 is

$$P_o = r(1 - P_1)(1 - P_2) + (1 - r)\{1 - (1 - P_1)(1 - P_2)\} \quad (4.10)$$

Using similar bifurcation analysis, one can have the following nonlinear mapping function:

$$\begin{aligned} X_{n+1} &= g(X_n) \\ &= (\alpha_0(\eta) + 2\alpha_1(\eta)X_n + \alpha_2(\eta)X_n^2)(1 - X_n)^2 \\ &\quad + \{1 - (\alpha_0(\eta) + 2\alpha_1(\eta)X_n + \alpha_2(\eta)X_n^2)\}\{1 - (1 - X_n)^2\} \end{aligned} \quad (4.11)$$

Our computation reveals that for a system built out of 2-input NOR gate

$$\begin{aligned}
 \eta^* &= 0.0324 \\
 x_o &= 0.3928 \quad (|g'(x)| = 1) \\
 \alpha_0 &= 0.9247 \\
 \alpha_1 &= -0.5918 \\
 \alpha_2 &= 0.1935
 \end{aligned} \tag{4.12}$$

4.3 Bifurcation Analysis for Circuits Built Out of K-input NOR Gate

4.3.1 Bifurcation Analysis for Circuits Built Out of 3-input NOR Gate

We do the similar bifurcation analysis for circuits built out of 3-input NOR gates.

Assuming the three inputs of NOR gate are independent with probabilities P_1 , P_2 and P_3 of their logic values being a 1, the reliability is r ($r > 0.5$) and the probability of P_o of the output V_o being a 1 is

$$P_o = r(1 - P_1)(1 - P_2)(1 - P_3) + (1 - r)\{1 - (1 - P_1)(1 - P_2)(1 - P_3)\} \tag{4.13}$$

Using similar bifurcation analysis, we can have the following nonlinear mapping function:

$$\begin{aligned}
 X_{n+1} &= h(X_n) \\
 &= (\alpha_0(\eta) + 3\alpha_1(\eta)X_n + 3\alpha_2(\eta)X_n^2)(1 - X_n)^3 \\
 &\quad + \{1 - (\alpha_0(\eta) + 3\alpha_1(\eta)X_n + 3\alpha_2(\eta)X_n^2)\}\{1 - (1 - X_n)^3\} \quad (4.14)
 \end{aligned}$$

Our computation reveals that for a system built out of 3-input NOR gate

$$\begin{aligned}
 \eta^* &= 0.084 \\
 x_o &= 0.3600 \quad (|g'(x)| = 1) \\
 \alpha_0 &= 0.5104 \\
 \alpha_1 &= 0.3218 \\
 \alpha_2 &= -0.1633 \quad (4.15)
 \end{aligned}$$

4.3.2 Bifurcation Analysis for Circuits Built Out of 4-input NOR Gate

We do the similar bifurcation analysis for circuits built out of 4-input NOR gates.

Assuming the four inputs of NOR gate are independent with probabilities P_1, P_2, P_3 and P_4 of their logic values being a 1, the reliability is r ($r > 0.5$) and the probability of P_o of the output V_o being a 1 is

$$P_o = r(1 - P_1)(1 - P_2)(1 - P_3)(1 - P_4) + (1 - r)\{1 - (1 - P_1)(1 - P_2)(1 - P_3)(1 - P_4)\} \quad (4.16)$$

Using similar bifurcation analysis, we can have the following nonlinear mapping function:

$$\begin{aligned}
X_{n+1} &= h(X_n) \\
&= (\alpha_0(\eta) + 4\alpha_1(\eta)X_n + 6\alpha_2(\eta)X_n^2)(1 - X_n)^4 \\
&\quad + \{1 - (\alpha_0(\eta) + 4\alpha_1(\eta)X_n + 6\alpha_2(\eta)X_n^2)\}\{1 - (1 - X_n)^4\} \quad (4.17)
\end{aligned}$$

Our computation reveals that for a system built out of 4-input NOR gate

$$\begin{aligned}
\eta^* &= 0.078 \\
x_o &= 0.3318 \quad (|g'(x)| = 1) \\
\alpha_0 &= 0.5724 \\
\alpha_1 &= 0.1752 \\
\alpha_2 &= -0.0382 \quad (4.18)
\end{aligned}$$

4.3.3 Discussions on the K-input Gate

For the 3-input NOR gates, the running time is 3114.5s with one certain η , while for the 4-input NOR gate, the running time is 47418s with one certain η . Hence, due to the calculation complexity, it is unrealistic to go on calculating the more K-input gate.

Table 4.1 provides the hardware and software environment for the experiment.

What's more, even only taking the 3-input NOR Gate into attention, before we find η^* , we keep doing calculations for the comparisons of $|f'(x)|$ and 1 which is a

Table 4.1: Hardware and Software Environment of the Experiment

Hardware Info	Intel(R), Pentium(R) 4 CPU 2.80GHz, 2.79GHz 512M of RAM
System Info	Microsoft Windows XP Professional Version 2002 Service Pack 2
MATLAB Info	Version 7.0.4.365 (R14) Service Pack 2

Figure 4.2: Tendency of $|g'(x)|$ in 2-input NOR Gate

long-time test. For this reason, we study the tendency of $|g'(x)|$ to wish for a quick way.

From Figure 4.2, $|g'(x)|$ seems like a monotone decreasing function. However, we haven't found a way to prove it right now. But if it is true, the complexity of the process of finding η^* could be reduced by increasing the step of $\Delta\eta$.

We collect the η we calculate for 3-input NOR gate (Figure 4.3), and observe the same discipline as that in 2-input NOR gate.

Figure 4.3: Tendency of $|h'(x)|$ in 3-input NOR Gate

Chapter 5

Future Work and Application

5.1 Energy Estimation

The proposed model characterizes a SET-based logic gate in terms of reliability, and can be used not only for the whole circuit reliability analysis, but also for tunneling event analysis and energy estimation. From Equation 4.10 and Equation 4.1, the probability for the tunneling event inside a gate j to occur, $P_{t,j}$, depends on its input probability as well as reliability, both of which are closely interwoven with other gates and may propagate throughout a circuit from its inputs to outputs. The energy consumed by a single tunneling event can be calculated as

$$\Delta E_j = e(|V_j| - V_c) \tag{5.1}$$

where V_j is the voltage across the junction and V_c the critical voltage of the junction. Thus, the sum of products of $P_{t,j}$ and ΔE_j (i.e., $\sum P_{t,j} \Delta E_j$) over all tunnels gives an estimated energy consumption of the SET-based logic circuit. The detailed implementation of this idea will be investigated in our future research work.

5.2 Fast Algorithm

The number of inputs can bring positive or negative impact on the reliability of the gate. By comparing different η^* of different number of inputs, we can find the maximum threshold value which implies the optimal number of inputs.

From Chapter 4, we can list the η^* we calculate for 2-input NOR gate, 3-input NOR gate and 4 input NOR gate in Table 5.1.

Comparing these three values, the 3-input NOR gate has the maximum value of η^* , which implies it is the optimal number of inputs during these three. By calculating more K-input NOR gate, we can find the optimal number of inputs regarding the high reliabilities.

However, as we discussed in Chapter 4.3.3, the time complexity of calculating η^* rises exponentially. It is not sensible to calculate the η^* for K-input ($K > 4$) gate by increasing η gradually. If the $|f'(x)|$ appears monotonously decreased in a certain area, we can develop some arithmetic for speeding up. By giving a large step length for η , we can find the x_1 fixed for $|f'(x)| > 1$ and x_2 fixed for $|f'(x)| < 1$ with a

Table 5.1: η^* for Different Number Inputs of NOR Gate

Number of Inputs	2	3	4
η^*	0.0324	0.084	0.078

rough glance. Then, the step could be changed to small to look for the η^* which fits for $|f'(x)| = 1$. Theoretical and practical demonstration would be focused on in the future work.

What' more, since most time of the calculation is spent on finding out α_i and β_j , another way to speed up is to find a function (sometimes sectioned) applying for α_i or β_j . Thus, the α_i or β_j could be looked for in the function curve figure without doing complex calculation.

5.3 Inputs Correlations

The above bifurcation analysis assumes that the inputs of a gate are statistically independent. However, this assumption is generally invalid for the circuit built with both NOR and NAND gates, where the input signals of a gate may be correlated. In this case, calculation of their joint and conditional probabilities among the inputs is generally required before the output probability can be evaluated [31]. The probabilistic transfer matrices (PTMs) proposed in [20] can be used to address this issue. The only difference is that in our situations, the reliability is not a constant, but a function of input probabilities in Equation 3.8 and Equation 3.10. Since the PTM approach is based on a exhaustive listing of input and output probabilities, the computational cost could be very expensive for large circuits. A more efficient mechanism based on Bayesian networks has been reported [19] to deal with this situation.

Chapter 6

Conclusion

In this thesis, we have proposed a statistical reliability model for individual SET logic gates. Different from the experiment in previous work where the failure factor assumed to be a constant value, it has been shown that the reliabilities of logic gates in a circuit are dependent on each other, even if they are physically identical. The scenarios of 2-input NOR gate, 2-input NAND gate and K-input NOR gate are discussed in this work.

With the bifurcation analysis, it has been demonstrated that there exists an upper bound of process variations for individual gates, which allows the circuit to operate reliably in a probabilistic sense. In this thesis, 2-input NAND gate is discussed and compared with the traditional method [21]. The smaller η^* in our work reduces the restriction in circuit designs.

Discussions on time complexity of K-input NOR gates are also provided here, followed by potential extensions and applications of this model.

Appendix A

MATLAB Programs for SET Experiment

A.1 Reliability Calculation for 2-input NAND Gate

This program is dedicated to calculate the reliabilities of different pairs of (P_1, P_2) with a certain η for 2-input NAND Gate.

Input: η 's value. Output: Reliabilities

```
function [ratio]=sigma_var_nand2(sigma)
```

```
cycle=10000; % the number of loops
```

```
ratio=zeros(11,11);
% the table for reliability p1 is from 0 to 1 by 0.1,
P2 is from 0 to 1 by 0.1.

for m=0:0.1:1 %P1
    for n=0:0.1:1 %P2
        count=0;

        for i=1:cycle
            c1=0.5;
            c2=0.5;
            co=9;
            cb=11.8;

            v1=binornd(1,m,[1,1]); %V1=e or 0
            v2=binornd(1,n,[1,1]); %V2=e or 0
            vb=1;

            v11=v1+randn(1)*v1*sigma/3;
            v22=v2+randn(1)*v2*sigma/3;
            c11=c1+randn(1)*c1*sigma/3;
            c22=c2+randn(1)*c2*sigma/3;
            cbb=cb+randn(1)*cb*sigma/3;

            vbb=vb+randn(1)*vb*sigma/3;
```

```
coo=co+randn(1)*co*sigma/3;

qx=randn(1)*sigma/3;
qy=randn(1)*sigma/3;
cnn=c11+c22+coo;

if v11>=0.5
    v11=1;
else
    v11=0;
end

if v22>=0.5
    v22=1;
else
    v22=0;
end

F=10*cnn*qx-cbb*(c11*v11+c22*v22+10*qy)-5*(cbb+cnn)+cnn*cbb*vbb;

result_true=sign(-v1-v2+1.5);

result=sign(F);

if result_true==result
    count=count+1;
end
```

```

end

a=round(m*10+1);
b=round(n*10+1);

ratio(a,b)=count/cycle;
end
end ratio

```

A.2 Calculation of α_i of 2-input NOR Gate

This program is dedicated to calculate α_0 , α_1 and α_2 for 2-input NOR gate.

```

A =[
    0.6130    0.6015    0.6059    0.6069    0.6156
    0.6055    0.6048    0.6068    0.6078    0.6012    0.6112;
    0.6058    0.6123    0.6119    0.6098    0.6163
    0.6106    0.6219    0.6097    0.6183    0.6418    0.6226;
    0.6023    0.6127    0.6129    0.6228    0.6208
    0.6263    0.6256    0.6262    0.6313    0.6476    0.6548;
    0.6060    0.6014    0.6196    0.6123    0.6273
    0.6304    0.6507    0.6438    0.6483    0.6625    0.6595;
    0.6134    0.6090    0.6204    0.6282    0.6267
    0.6338    0.6462    0.6538    0.6679    0.6773    0.6802;
    0.5990    0.6168    0.6233    0.6327    0.6422
    0.6540    0.6617    0.6635    0.6766    0.6890    0.7011;
    0.5986    0.6104    0.6345    0.6332    0.6507

```

A. MATLAB PROGRAMS FOR SET EXPERIMENT

0.6652	0.6801	0.6776	0.6877	0.7092	0.7183;
0.6098	0.6281	0.6272	0.6469	0.6561	
0.6695	0.6822	0.7004	0.7066	0.7204	0.7292;
0.6099	0.6083	0.6421	0.6533	0.6789	
0.6805	0.6974	0.7110	0.7144	0.7403	0.7488;
0.5988	0.6243	0.6399	0.6563	0.6735	
0.6874	0.7087	0.7257	0.7445	0.7571	0.7715;
0.6067	0.6261	0.6429	0.6660	0.6764	
0.6939	0.7164	0.7327	0.7585	0.7675	0.7890];

```
B=zeros(11,11);
```

```
for i=1:11
    for j=1:i
        B(i,j)=0.5*(A(i,j)+A(j,i));
    end
end
```

```
K=zeros(66,1);
```

```
for i=1:66
    P(i,1)=1;
end
```

```
for i=1:11
    for j=1:i
```

```

        K((i-1)*i/2+j)=B(i,j);
        P((i-1)*i/2+j,2)=(i+j-2)*0.1;
        P((i-1)*i/2+j,3)=(i-1)*0.1*(j-1)*0.1;
    end
end

s=P\K

error=P*s-K;

errorratio=error./K;

max(errorratio)

```

A.3 Calculation for η^* of 2-input NOR Gate

The program is dedicated to calculate the η^* for 2-input NOR gate with the reliabilities collected from A.1. By comparing $|f'(x)|$ with 1, η^* is obtained.

```

clear clc
ss1 =[
    1.0000    1.0000    0.9897    0.9393    0.8788
    0.8218    0.7786    0.7441    0.7178    0.6925
    0.6751    0.6568    0.6441    0.6335    0.6233;
    0    -0.0002   -0.0271   -0.0575   -0.0645
    -0.0582  -0.0532  -0.0480  -0.0438  -0.0343

```

A. MATLAB PROGRAMS FOR SET EXPERIMENT

```

-0.0316  -0.0237  -0.0236  -0.0211  -0.0154;
         0   0.0003   0.0647   0.1760   0.2486
    0.2858  0.3030   0.3064   0.2981   0.2795
    0.2685  0.2506   0.2446   0.2284   0.2111];

```

```

ss2=[
    0.6190  0.6088  0.5996  0.5950  0.5872
    0.5813  0.5801  0.5753  0.5715  0.5664
    0.5634  0.5609  0.5565  0.5487  0.5512;
   -0.0207  -0.0137  -0.0088  -0.0084  -0.0048
   -0.0004  -0.0040  -0.0027  -0.0024  0.0038
    0.0054  0.0040  0.0069  0.0136  0.0089;
    0.2100  0.1912  0.1753  0.1669  0.1614
    0.1478  0.1480  0.1428  0.1392  0.1224
    0.1135  0.1171  0.1042  0.0973  0.0984];

```

```

ss3=[
    0.5499  0.5470  0.5442  0.5412  0.5404
    0.5395  0.5374  0.5354  0.5331  0.5331
    0.5304  0.5269  0.5267  0.5235  0.5221;
    0.0110  0.0103  0.0142  0.0136  0.0148
    0.0157  0.0167  0.0169  0.0200  0.0192
    0.0191  0.0254  0.0248  0.0272  0.0295;
    0.0897  0.0921  0.0815  0.0840  0.0780
    0.0733  0.0677  0.0721  0.0653  0.0617
    0.0650  0.0502  0.0504  0.0460  0.0407];

```

```

ss4=[
    0.5219    0.5226    0.5192    0.5172    0.5173    0.5184;
    0.0276    0.0263    0.0306    0.0325    0.0323    0.0283;
    0.0443    0.0442    0.0364    0.0307    0.0315    0.0369];

ss=[ss1,ss2,ss3,ss4];

S2=solve('a0=0.9897','a1=-0.0271','a2=0.0647','eta=0.02',
'a0+x*(2-4*a0+2*a1)+x*x*(-1+2*a0-8*a1+a2)
+x*x*x*(4*a1-4*a2)+x*x*x*x*2*a2=x')
x=.38430165546097061335289602172135; a0=0.9897;a1=-0.0271;a2=0.0647;
daoshu2=
abs((2-4*a0+2*a1)+x*2*(-1+2*a0-8*a1+a2)+x*x*3*(4*a1-4*a2)+x*x*x*4*2*a2)
daoshu2=1.1772;

S3=solve('a0=0.9393','a1=-0.0575','a2=0.1760','eta=0.03',
'a0+x*(2-4*a0+2*a1)+x*x*(-1+2*a0-8*a1+a2)
+x*x*x*(4*a1-4*a2)+x*x*x*x*2*a2=x')
x=.39110792502617101953124427236501; a0=0.9393;a1=-0.0575;a2=0.1760;
daoshu3=
abs((2-4*a0+2*a1)+x*2*(-1+2*a0-8*a1+a2)+x*x*3*(4*a1-4*a2)+x*x*x*4*2*a2)
daoshu3=1.0318;

S4=solve('a0=0.8788','a1=-0.0645','a2=0.2486','eta=0.04',
'a0+x*(2-4*a0+2*a1)+x*x*(-1+2*a0-8*a1+a2)
+x*x*x*(4*a1-4*a2)+x*x*x*x*2*a2=x')
x=.39855168966584040807999964690406; a0=0.8788;a1=-0.0645;a2=0.2486;

```

```

daoshu4=
abs((2-4*a0+2*a1)+x*2*(-1+2*a0-8*a1+a2)+x*x*3*(4*a1-4*a2)+x*x*x*4*2*a2)
% daoshu4=0.9018;

S5=solve('a0=0.8218','a1=-0.0582','a2=0.2858','eta=0.05',
'a0+x*(2-4*a0+2*a1)+x*x*(-1+2*a0-8*a1+a2)
+x*x*x*(4*a1-4*a2)+x*x*x*x*2*a2=x')
x=.40562682844793606412379201618205; a0=0.8218;a1=-0.0582;a2=0.2858;
daoshu5=
abs((2-4*a0+2*a1)+x*2*(-1+2*a0-8*a1+a2)+x*x*3*(4*a1-4*a2)+x*x*x*4*2*a2)
daoshu5=0.7985;

S6=solve('a0=0.7786','a1=-0.0532','a2=0.3030','eta=0.06',
'a0+x*(2-4*a0+2*a1)+x*x*(-1+2*a0-8*a1+a2)
+x*x*x*(4*a1-4*a2)+x*x*x*x*2*a2=x')
x=.41182834861314188595580724704232; a0=0.7785;a1=-0.0532;a2=0.3030;
daoshu6=
abs((2-4*a0+2*a1)+x*2*(-1+2*a0-8*a1+a2)+x*x*3*(4*a1-4*a2)+x*x*x*4*2*a2)
daoshu6=0.7171;

% S25=solve('a0=0.5634','a1=0.0054','a2=0.1135','eta=0.25',
'a0+x*(2-4*a0+2*a1)+x*x*(-1+2*a0-8*a1+a2)
+x*x*x*(4*a1-4*a2)+x*x*x*x*2*a2=x')
x=.46119747479344398387555401845264; a0=0.5634;a1=0.054;a2=0.1135;
daoshu25=
abs((2-4*a0+2*a1)+x*2*(-1+2*a0-8*a1+a2)+x*x*3*(4*a1-4*a2)+x*x*x*4*2*a2)
daoshu6=0.3852;

```

```
% S=solve('a0=1.1208-6.05*eta','a1=-0.0365-0.7*eta','a2=-0.0418+7.26*eta',
'eta=0.035',
'a0+x*(2-4*a0+2*a1)+x*x*(-1+2*a0-8*a1+a2)
+x*x*x*(4*a1-4*a2)+x*x*x*x*2*a2=x')
x=.39471104834237266454313863420964; a0=0.90905;a1=-0.061;a2=0.2123;
daoshu=
abs((2-4*a0+2*a1)+x*2*(-1+2*a0-8*a1+a2)+x*x*3*(4*a1-4*a2)+x*x*x*4*2*a2)
daoshu6=0.9661;

S=solve('a0=1.1208-6.05*eta','a1=-0.0365-0.7*eta','a2=-0.0418+7.26*eta',
'eta=0.0325',
'a0+x*(2-4*a0+2*a1)+x*x*(-1+2*a0-8*a1+a2)
+x*x*x*(4*a1-4*a2)+x*x*x*x*2*a2=x')
x=.39288094782631372330944845154668;
a0=0.924175;a1=-0.592500000000000000000000000000e-1;a2=0.19415;
daoshu=
abs((2-4*a0+2*a1)+x*2*(-1+2*a0-8*a1+a2)+x*x*3*(4*a1-4*a2)+x*x*x*4*2*a2)
daoshu6=0.9988;

S=solve('a0=1.1208-6.05*eta','a1=-0.0365-0.7*eta','a2=-0.0418+7.26*eta',
'eta=0.032',
'a0+x*(2-4*a0+2*a1)+x*x*(-1+2*a0-8*a1+a2)+x*x*x*(4*a1-4*a2)+x*x*x*x*2*a2=x')
x=.39252184868858686565445126061987;
a0=0.9272000;a1=-0.589000000000000000000000000000e-1;a2=0.19052;
daoshu=
abs((2-4*a0+2*a1)+x*2*(-1+2*a0-8*a1+a2)+x*x*3*(4*a1-4*a2)+x*x*x*4*2*a2)
```

```
daoshu6=1.0054;
```

```
S=solve('a0=1.1208-6.05*eta','a1=-0.0365-0.7*eta','a2=-0.0418+7.26*eta',
'eta=0.0324',
'a0+x*(2-4*a0+2*a1)+x*x*(-1+2*a0-8*a1+a2)+x*x*x*(4*a1-4*a2)+x*x*x*x*2*a2=x')
x=.39280894594434976144240266055196;
a0=0.92478;a1=-0.591800000000000000000000000000e-1;a2=0.193424;
daoshu=
abs((2-4*a0+2*a1)+x*2*(-1+2*a0-8*a1+a2)+x*x*3*(4*a1-4*a2)+x*x*x*4*2*a2)
daoshu6=1.0001;
```

```
S=solve('a0=1.1208-6.05*eta','a1=-0.0365-0.7*eta','a2=-0.0418+7.26*eta',
'eta=0.03242',
'a0+x*(2-4*a0+2*a1)+x*x*(-1+2*a0-8*a1+a2)+x*x*x*(4*a1-4*a2)+x*x*x*x*2*a2=x')
x=.39282333902252856368667680843748;
a0=0.924659;a1=-0.591940000000000000000000000000e-1;a2=0.193569200;
daoshu=
abs((2-4*a0+2*a1)+x*2*(-1+2*a0-8*a1+a2)+x*x*3*(4*a1-4*a2)+x*x*x*4*2*a2)
daoshu6=0.9998;
```

```
S=solve('a0=1.1208-6.05*eta','a1=-0.0365-0.7*eta','a2=-0.0418+7.26*eta',
'eta=0.03241',
'a0+x*(2-4*a0+2*a1)+x*x*(-1+2*a0-8*a1+a2)+x*x*x*(4*a1-4*a2)+x*x*x*x*2*a2=x')
x=.39281614202751588562645501680364;
a0=0.9247195;a1=-0.59187e-1;a2=0.1934966;
daoshu=
abs((2-4*a0+2*a1)+x*2*(-1+2*a0-8*a1+a2)+x*x*3*(4*a1-4*a2)+x*x*x*4*2*a2)
```

```
daoshu6=0.9999;

S=solve('a0=1.1208-6.05*eta','a1=-0.0365-0.7*eta','a2=-0.0418+7.26*eta',
'eta=0.032405',
'a0+x*(2-4*a0+2*a1)+x*x*(-1+2*a0-8*a1+a2)+x*x*x*(4*a1-4*a2)+x*x*x*x*2*a2=x')
x= .39281254387196096367341749927720;
a0=0.92474975;a1=-0.5918350e-1;a2=0.1934603;
daoshu=
abs((2-4*a0+2*a1)+x*2*(-1+2*a0-8*a1+a2)+x*x*3*(4*a1-4*a2)+x*x*x*4*2*a2)
daoshu6=1.0000;

xx=0.03:0.01:0.04; y1=ss(1,4:5); P1=ones(2,2); P1(:,2)=xx; K1=y1';
s1=P1\K1; s1=[1.1208,-6.05] figure;plot(xx,y1,'r+') hold on
plot(xx,s1(1)+s1(2)*xx,'b')

y2=ss(2,4:5); P2=ones(2,2); P2(:,2)=xx; K2=y2'; s2=P2\K2;
s2=[-0.0365,-0.7] figure;plot(xx,y2,'r+') hold on
plot(xx,s2(1)+s2(2)*xx,'b')

y3=ss(3,4:5); P3=ones(2,2); P3(:,2)=xx; K3=y3'; s3=P3\K3;
s1=[-0.0418,7.26] figure;plot(xx,y3,'r+') hold on
plot(xx,s3(1)+s3(2)*xx,'b')
```

A.4 Stages of 2-input NAND Gate

The program is dedicated to compare the reliabilities with $\eta > \eta^*$ and $\eta < \eta^*$ for 2-input NAND Gate

```
clear
clc

k=120;

eta=0.03;
a0=1.000;
a1=-0.0709;
a2=0.051;

x=zeros(1,k);

z=zeros(1,k);

r=zeros(1,k);

x(1)=0.7;

for i=1:k
    r(i)=a0+a1*2*x(i)+a2*x(i)*x(i);
    z(i)=r(i)+(2*r(i)-1)*(x(i)*x(i)-2*x(i));
    x(i+1)=z(i);
end

i=1:k;

plot(i,r(i),'o')
```

```
hold on

etaa=0.04;
aa0=1.0002;
aa1=-0.1366;
aa2=0.1164

xx=zeros(1,k);
zz=zeros(1,k);

xx(1)=0.7;

rr=zeros(1,k);

for i=1:k
    rr(i)=aa0+aa1*2*xx(i)+aa2*xx(i)*xx(i);

    zz(i)=rr(i)+(2*rr(i)-1)*(xx(i)*xx(i)-2*xx(i));

    xx(i+1)=zz(i);
end

i=1:k;
plot(i,rr(i),'r')
plot(i,r(i))
plot(i,rr(i),'r')
```

```
xlabel('stage')
ylabel('reliability')

legend('\eta=0.03', '\eta=0.04')
title('NAND 2input gate')
```


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