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An On-chip PVT Resilient Short Time Measurement Technique

Esrafil Jedari Sefidgari  
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An On-chip PVT Resilient Short Time Measurement Technique

By

Esrafil Jedari

A Dissertation
Submitted to the Faculty of Graduate Studies
through the Department of Electrical and Computer Engineering
in Partial Fulfillment of the Requirements for
the Degree of Doctor of Philosophy
at the University of Windsor

Windsor, Ontario, Canada

2018

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An On-chip PVT Resilient Short Time Measurement Technique

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Declaration of Co-Authorship
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I. CO-AUTHORSHIP DECLARATION

I hereby declare that this dissertation incorporates material that is the result of research conducted under the supervision of my supervisors, Dr. R. Rashidzadeh and Dr. M. Saif. An industry application of this work has been published with two co-inverters from industry, Mr. K. Bishop and Mr. A. Shanawaz as well. Results related to this research are reported in Chapters 2 through 4.

I am aware of the University of Windsor's Senate Policy on Authorship and I certify that I have properly acknowledged the contributions of the other researchers to my dissertation, and I have obtained written permission from my co-authors to include the aforementioned materials in my dissertation.

I certify that this dissertation, and the research results to which it refers, is the product of my own work.
II. DECLARATION OF PREVIOUS PUBLICATION

This thesis includes three original papers/patent that have been previously submitted for publication in peer reviewed journals and conferences, as follows:

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Abstract

As the CMOS technology nodes continue to shrink, the challenges of developing manufacturing tests for integrated circuits become more difficult to address. To detect parametric faults of new generation of integrated circuits such as 3D ICs, on-chip short-time intervals have to be accurately measured. The accuracy of an on-chip time measurement module is heavily affected by Process, supply Voltage, and Temperature (PVT) variations. This work presents a new on-chip time measurement scheme where the undesired effects of PVT variations are attenuated significantly. To overcome the effects of PVT variations on short-time measurement, phase locking methodology is utilized to implement a robust Vernier delay line. A prototype Time-to-Digital Converter (TDC) has been fabricated using TSMC 0.180 µm CMOS technology and experimental measurements have been carried out to verify the performance parameters of the TDC. The measurement results indicate that the proposed solution reduces the effects of PVT variations by more than tenfold compared to a conventional on-chip TDC.

A coarse-fine time interval measurement scheme which is resilient to the PVT variations is also proposed. In this approach, two Delay Locked Loops (DLLs) are utilized to minimize the effects of PVT on the measured time intervals. The proposed scheme has
been implemented using CMOS 65nm technology. Simulation results using Advanced Design System (ADS) indicate that the measurement resolution varies by less than 0.1ps with ±15% variations of the supply voltage. The proposed method also presents a robust performance against process and temperature variations. The measurement accuracy changes by a maximum of 0.05ps from slow to fast corners. The implemented TDC presents a robust performance against temperature variations too and its measurement accuracy varies a few femto-seconds from -40 ºC to +100 ºC.

The principle of robust short-time measurement was used in practice to design and implement a state-of-the-art Coordinate Measuring Machine (CMM) for an industry partner to measure geometrical features of transmission parts with micrometer resolution. The solution developed for the industry partner has resulted in a patent and a product in the market. The on-chip short-time measurement technology has also been utilized to develop a solution to detect Hardware Trojans.
Dedication

To my parents, my wife and my lovely daughters and son.
I would like to extend my acknowledgement to the people without whom this dissertation would never have been accomplished. First and foremost, my wonderful loving family, especially my spouse Dr. Mina Maleki. Their continuous support have provided me with the inspiration, power, and dedication I needed to complete this work.

I cannot thank enough my honorable supervisors, Dr. Rashid Rashidzadeh and Dr. Mehrdad Saif who were my guidance throughout my Ph.D. studies. Especially Dr. Rashidzadeh was monumental in helping me always. The amount of time he spent with me correcting and suggesting my research plan, and effort he put behind me was outstanding.

I appreciate my wonderful committee members, Dr. Alioune Ngom from Computer Science, Dr. Huapeng Wu, and Dr. Roberto Muscedere from Electrical Engineering for their constructive feedback and valuable comments.

Next, I would like to thank my colleagues and friends in the Research Centre for Integrated Microsystems (RCIM), particularly Tareq Muhammad Supon for his support and technical assistance.

Lastly, I would like to thank everyone that I have ever talked to or met during my study at the University of Windsor.
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Chapter 1

Introduction

1.1. MOTIVATION OF THIS WORK

The CMOS technology has followed the path to shrink the transistor sizes for decades with a relatively constant rate [1]. Fig. 1.1 shows the development of CMOS technology since 1970. While the reduction of transistor sizes contributes significantly to the technology development, it also presents challenges to IC designers. Developing manufacturing test for new generation of integrated circuits is proven to be quite challenging. Parametric faults and delay faults in such devices are becoming the dominant sources of defects which are difficult to detect using a conventional Automatic Test Equipment (ATE). To cover these faults in the test phase, an on-chip short-time measurement module can be utilized [8]. However, the resolution and accuracy of on-chip time measurement solutions vary considerably with PVT variations. An overview of timing-related problems in circuits, time measurement techniques, and a brief description of the proposed solutions are presented in the following subsections.
1.2. **TIMING PROBLEMS**

**Jitter**

One of the main sources of timing problems in circuits is jitter which is defined as a difference between the phase of an ideal and actual clock [10]. Fig. 1.2, shows an ideal clock with a solid line and the actual clock with a dashed-line. The deviation from the ideal edges determines the jitter. Cycle to cycle jitter, and period jitter are taken into consideration in jitter characterization and measurements [11], [12]. Jitter performance of a circuit limits the time-measurement system’s resolution. Variations of Process, Voltage,
and Temperature (PVT) affect the switching time of digital cells which results in poor jitter performance [13].

Clock Skew

Clock skew occurs when a clock experiences different path delays and therefore the clock is applied at different times to the circuits connected to the clock tree. Fig. 1.3 shows two registers driven by the same clock. However due to the routing delay, the clock arrives at different times of $t_{CLK1}$ and $t_{CLK2}$ causing wrong data to be captured by the flip flops.

### 1.3. Time Interval Measurement Techniques

A. Counter-based time measurement technique

There are different time-measurement methods, an easy solution to measure time intervals is to use a high frequency clock and a counter [15]. The counter starts counting at the rising edge of the input signal and stops counting at its falling edge as shown in Fig. 1.4. The number at the output of the counter multiply by the period of the clock represents
the time interval of $\Delta T$. This method is easy to implement but the measurement resolution is limited.

**B. Signal condition technique**

Signal conditioning technique can also be used for time measurement [16]. In this method, the input pulse is used to turn on a switch to charge a capacitor with a known current source,
I1, and then the switch is turned off discharging the capacitor with another current source, 
I2, where $I_2 << I_1$. In this method a high resolution counter is used to determine the time 
interval of $T$. The dual slop measurement in this method eliminates the first degree non-
linearity errors.
C. Delay line methods

A delay line with a series of flip-flops, as shown in Fig. 1.6a, can also be used for time measurement [17-21]. A digital code at the flip-flops outputs represents the time difference between the Start and the Stop signals. As shown in Fig. 1.6a Start and Stop signals are applied to the inputs. The Start signal experiences a delay after each delay cell in its path and therefore the flip flops receive the data at different times. The output of each flip-flop stays the same (i.e. 1) until the Start signal leads the Stop signal. The number of ones at the output of the flip-flops multiply by the propagation delay of delay cells represents the time interval between the Start and the Stop signals. The minimum propagation delay of a delay cell, \( t_d \), represents the measurement resolution of the tapped-delay line. To overcome this limitation, a Vernier Delay Line (VDL) as shown in Fig. 1.6b can be utilized. The principle
of operation for this new configuration is the same as explained for the previous configuration. However, the TDC utilizing Vernier delay line support a much higher measurement resolution of $t_{d1} - t_{d2}$.

**D. TDC performance with PVT variations and proposed method**

A Vernier based TDCs is sensitive to the delay performance of the delay cells. Different parameters in the fabrication process can cause device performance variations [22]. For instance, the exposure time results in different lengths and widths of transistors, which affect their parasitic capacitances and their propagation delay performance. Temperature variations also affect the threshold voltage of transistors [23]. The Threshold voltage decreases as the temperature increases which leads to a lower gate propagation delay. Power supply variations can also impact the threshold voltage of transistors.

In this work a technique is presented to control the propagation delay through two DLLs to minimize the effect of PVT variations on time interval measurement.
A DLL uses a feedback structure to compare the delay (phase) of two signals at the input of phase frequency detector (PFD) as shown in Fig. 1.7. [24]. When a DLL locks, it reduces the phase difference between the two inputs to zero in an ideal case. The PFD produces pulses based on the phase difference between the inputs, $\phi_{in}$ and $\phi_{out}$ where $\phi_{in}$ represents the phase of the input signal and $\phi_{out}$ is the phase of the output of the Voltage Controlled Delay Line (VCDL). These pulses are applied to a charge pump (CP). The CP increases or decreases the propagation delay of the delay cells in the VCDL. The VCDL delay variation changes the phase difference between the output and the input signals until the lock is captured where the phase difference between them ideally becomes zero. In the locked state, the delay of the VCDL represents the total delay between the two signals. We
have used two VCDLs controlled by two DLLs in a Vernier based TDC as shown in Fig. 1.8. The DLLs guarantee that the propagation delay of delay cells remain constant regardless of PVT variations.

1.4. RESEARCH CONTRIBUTIONS

The following paragraphs outline the main research contributions described in this dissertation:

A. Designed and fabricated an accurate and high-resolution time measurement scheme which is resilient to the Process, supply Voltage, and Temperature (PVT) variations:

A DLL enabled Vernier-based TDC has been designed and fabricated using 0.180μm CMOS technology. Measurement results using a prototype show that the proposed measurement scheme reduces the effects of PVT variations by more than tenfold compared to the conventional Vernier-based TDC technique. The results of this work have been published in the Elsevier Journal of Microelectronics and presented in Chapter [25].

B. Controllable fine-coarse time measurement circuit:

A programmable coarse-fine time measurement circuit with adjustable resolution is presented in Chapter 3. In the proposed measurement solution, two DLLs have been utilized to minimize the effects of PVT variations on the measurement results. A two-step time-to-digital converter is designed to ensure a high-resolution measurement over a wide dynamic range. The proposed scheme has been implemented using CMOS 65nm technology. Simulation results indicate that the
measurement resolution varies by less than 0.1ps with ±15% of supply voltage fluctuation. The proposed method also presents a robust performance against process and temperature variations and its accuracy changes by a maximum of 0.05ps from slow to fast corners for process variations and it varies a few femto-seconds with changes from -40 ºC to +100 ºC in temperature [26].

C. Hardware Trojan detection using a magnifying method

To reduce the fabrication costs of microchips many companies have started to outsource their manufacturing to offshore foundries. Outsourcing semiconductor manufacturing creates opportunities for adversaries to add malicious circuits and Trojans to microchips. A new technique based on a high-resolution TDC is developed to magnify Trojan switching activities without increasing the background noise. A passive component is used to increase a Trojan visibility and detect its switching activities using an on-chip TDC. Chapter 4 represents the details of proposed scheme for hardware Trojan detection [27].

D. Time measurement for an industry application:

Time measurement systems are used for different applications including 3D imaging cameras [28], [29]. Accurate and high-resolution time measurement systems can be utilized for geometrical measurement of auto-industry parts. The Coordinate Measuring Machine (CMM) in Fig. 1.9 was designed, implemented and tested for an industry partner to accurately measure the geometrical features of transmission parts. The designed system outperforms the available CMM
machines by a wide margin. It is currently in the market and actively used by auto-part manufacturers. In this project, the principle of accurate time measurement was utilized to improve the measurement accuracy and extract the geometrical features of transmission parts with a resolution of less than 10μm. This project has been recognized among the top 8 projects funded by Ontario Centres of Excellence (OCE) projects in the OCE 2017 annual report. It is also reported as a success story by Canadian Microelectronics Corporation (CMC) in 2017. The proposed measurement solution has been patented in both US and Canada. The details of published patent are represented in appendix A [30].

Fig. 1.9. Implemented Coordinate Measurement Machine for the industry partner in which the principle of short-time measurement is utilized to support less than 10μm measurement resolution for auto-industry parts.
1.5. DISSERTATION STRUCTURE

The rest of this dissertation is organized as follows:

- Chapter 2 presents a paper on A PVT Resilient Short-Time Measurement Solution for On-Chip Testing. This work has been published in the Microelectronics Journal from Elsevier, Feb. 2018.

- Chapter 3 is another paper on A PVT Resistant Coarse-fine Time-to-Digital Converter which has been published in the 2017 IEEE International Symposium on Circuits & Systems (ISCAS 2017) held in Baltimore, MD, USA.

- Chapter 4 covers a new technique to magnify Trojan switching activities without increasing the background noise. A paper titled “A Hardware Trojan Activity Magnifier” has been submitted to the IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems in Sept. 2018.

- Chapter 5 outlines the summary of this work, conclusions and the future work.

- Appendix A includes the published US patent as a results of application of time measurement in a real product at auto-industry, published on Oct. 24, 2017.

- Appendix B contains the list of published journal and conference papers during my PhD studies, but not related to the dissertation topic.

BIBLIOGRAPHY


Chapter 2

*A PVT Resilient Short-Time Measurement Solution for On-Chip Testing*

2.1. Introduction

Accurate short time measurement is essential for many applications [1] including fault detection in Through Silicon Vias (TSV) based 3D ICs [2] and hardware Trojan detection. Test solutions for TSV parametric faults [3-4] require an accurate high-resolution time measurement module. A delay measurement method is proposed in [5] to determine the delay variations caused by TSV open resistive defects. In this method, a reference voltage is applied to the TSV under test and the output is compared with a reference to determine pass/fail results. The difference between frequencies of two ring oscillators has also been proposed to detect TSV defects [6-7]. Most of the available on-chip time-measurement solutions in the literature do not address the effect of Process, supply Voltage, and Temperature (PVT) variations on the measurement accuracy. A Vernier delay line is commonly used to measure on-chip short-time intervals [8]. The measurement resolution of a Vernier based Time-to-Digital converter (TDC) is determined by the propagation delay difference between the delay-cells used to
implement the TDC. However, the PVT effects can undermine the measurement results in this method leading to faulty devices passing manufacturing tests or good parts failing the tests. To ensure the accuracy of on-chip measurement results in the presence of PVT variations, Delay Locked Loops (DLLs) are utilized in the current study. Fine-coarse DLL based TDC has been presented in [9]. The current study presents characterization and measurement results of a Vernier based TDC controlled by two DLLs implemented using Cadence tools and fabricated using 180nm CMOS technology. The rest of this chapter is organized as follows: Section II introduces background of short time measurement methods, detailed discussion and the architecture of the proposed scheme; Section III introduces details of the measurement circuit and its limitations; simulation and measurement results are discussed in Section IV; and conclusions are presented in Section V.

### 2.2. ARCHITECTURE OF PROPOSED TIME INTERVAL MEASUREMENT SCHEME

**Background of Short Time Measurement Methods**

The conventional approach to measure short-time intervals in the integrated circuits is to utilize a series of delay cells and flip-flops to convert a time-interval to a digital code. Such a scheme is commonly called a tapped-delay line Time-to-Digital Converter (TDC). A tapped-delay line TDC, as shown in Fig. 2.1a, consists of flip-flops employed as arbiters. The start signal is applied to the data inputs of flip-flops through a delay line and the stops signal is fed to the clock inputs. The time difference between the rising edges of the start and stop signals decreases after each step until the start signal leads the stop signal. The
outputs of the flip-flops indicate the time difference between the start and stop signals. The resolution of the time measurement in this method is limited by the propagation delay of a single delay cell \( t_d \) in the delay lines. Such a measurement resolution is not appropriate for many applications. To increase the resolution of a tapped delay line TDC, a Vernier delay line (VDL) based TDC is proposed. The schematic diagram of a VDL based TDC is shown in Fig. 1b. The measurement resolution of the Vernier based TDC in Fig. 2.1b is determined by the time difference between the propagation delays of the delay cells in the upper and lower delay chains in the structure.
which is $t_{d1} - t_{d2}$, where $t_{d1}$ and $t_{d2}$ are the propagation delays of each delay cell at the top and bottom delay lines, respectively. The resolution of a VDL based TDC is much smaller than the propagation delay of one delay cell.

The measurement accuracy of a Vernier based TDC is heavily affected by PVT variations. The propagation delay of the cells in the delay lines changes with process, supply voltage and temperature variations considerably affecting the measurement accuracy and resolution. To overcome the undesired effects of PVT on the measurement results, in this work Delay Locked Loop (DLLs) are used to control the propagation delay of the delay cells through a reference signal.

2.3. Delay Locked Loop Structure to Control Voltage of VCDL

A DLL is a feedback system that compares the phase between its input and output signals [2]. In an ideal locked condition, the phase difference between the input and output signals is reduced to zero. Fig. 2.2 shows the block diagram of a conventional DLL. The
Phase Frequency Detector (PFD) is driven by the input clock and the output signal of the Voltage Controlled Delay Line (VCDL). The PFD generates error pulses based on the phase difference between the clock and the output signals. These pulses are applied to the charge pump (CP) to increase or decrease the control voltage, Vctrl, to control the delay values in the VCDL. The variations of the control voltage changes the phase of the VCDL output signal until it becomes in-phase with the input clock. When the DLL settles, the phase difference between the input and output signals is minimized and the lock is acquired. In a locked DLL, the delay of each delay cell has to be a fraction of the period of applied clock at the input, $T$. Therefore, by using DLL, practically one can control the propagation delay of delay cells in the VCDL, precisely. The propagation delay of each delay-cell can be calculated from $t_d = T/N$ in the structure shown in Fig. 2.2, where $N$ is number of delay cells in the VCDL.

2.4. Proposed scheme

The block diagram of the proposed scheme is shown in Fig. 2.3. The circuit is composed of a Vernier based TDC and two DLLs where a reference clock is applied to the DLLs. As shown in Fig. 2.4, when the “Start” and “Stop” signals with delay difference of $\Delta T$ are applied to the circuit, the delay difference between them reduces by $t_{d1} - t_{d2}$ after each stage. where $t_{d1}$ and $t_{d2}$ are the propagation delays of delay cells in DLL1 and DLL2 respectively. When the rising edge of the Start signal passes the Stop signal, the transition is captured by a flip-flop in the TDC. The number of zeros at the output of flip-flops in the TDC multiply by the measurement resolution of the circuit ($t_r$) represents the time interval between rising edges of the Start and the Stop signals. In the proposed
solution, instead of free running delay cells of conventional Vernier based TDCs, voltage controlled delay cells are used. When the DLLs lock on the reference clock, the propagation delay of the delay lines in the DLLs is adjusted to maintain the lock regardless of the PVT variations. The measurement resolution can be controlled by varying the reference clock frequency. The number of delay cells in the DLLs can also affect the measurement resolution. In Fig. 2.3, DLL1 consists of N1 delay cells and DLL2 includes N2 delay cells. It is shown by equations in the following subsection that the use of different number of delay-cells allows the proposed solution to support a high measurement accuracy and resolution.

Fig. 2.3. Proposed Vernier delay line TDC utilizing two DLLs and using their delay lines to control delay chains.
A. Resolution and limitations of the proposed scheme

When the DLLs in Fig. 2.3 are locked, the propagation delay of each delay-cell becomes a function of the reference clock period, $T_{\text{ref}}$, and the number of delay cells in the delay lines, $N_1, N_2$. The propagation delay of each delay-cell can be calculated from $t_{d1} = T_{\text{ref}} / N_1$, $t_{d2} = T_{\text{ref}} / N_2$, where $T_{\text{ref}}$ is the period of the reference clock, $N_1$ and $N_2$ are the number of delay cells in the delay chains of DLL1 and DLL2, respectively.

As the number of delay cells in the delay lines are not equal, we can write $N_2 = N_1 + M$, where $M$ is the additional delay cells implemented in the DLL2. Thus, the resolution of the TDC can be calculated from

$$t_R = \frac{T_{\text{ref}}}{N_1} - \frac{T_{\text{ref}}}{N_1+M} = \frac{MT_{\text{ref}}}{N_1(N_1+M)}. \hspace{1cm} (1)$$

It can be seen from (1) that the number of delay cells in the delay lines and the frequency/period of the reference clock are the main parameters to control the measurement resolution in the proposed circuit. The number of delay cells cannot be altered after fabrication and should be chosen based on the dynamic range of measurement and the desired measurement resolution. However, $T_{\text{ref}}$ can be tuned during the measurement phase to meet the required measurement resolution.

In practice, the resolution of the proposed circuit is limited by jitter performance of the circuit. The rms jitter of the proposed circuit in Fig. 2.3 can be expressed as follow [10]:

$$\sigma_{\text{rms}} = \sqrt{\sigma_{\text{DLL1}}^2 + \sigma_{\text{DLL2}}^2 + \sigma_{\text{DL1}}^2 + \sigma_{\text{DL2}}^2}. \hspace{1cm} (2)$$

where, $\sigma_{\text{DLL1}}, \sigma_{\text{DLL2}}, \sigma_{\text{DL1}}, \sigma_{\text{DL2}}$ are the rms jitter of the DLLs and the delay lines in the TDC. It should be noted that two external sources of jitter affect the precision of the measurement. These sources are the rms jitter of the reference clock, $\sigma_{\text{ref}}$ and the jitter.
of Start and Stop signals, \( \sigma_{\text{Start}}, \sigma_{\text{Stop}} \). Since, the Stop signal is a delayed version of the Start signal, we can consider \( \sigma_{\text{Start}} = \sigma_{\text{Stop}} \). The rms jitter of a DLL can be determined from the jitter of a single delay cell, \( \sigma_{\text{cell}} \) as

\[
\sigma_{\text{DLL}_{1,2}} = \sqrt{N_{1,2}} \sigma_{\text{cell}} \cdot \sigma_{\text{DLL}_{1,2}} = \sqrt{N} \sigma_{\text{cell}}. \tag{3}
\]

Therefore, the total rms jitter of the proposed measurement solution in Fig. 2.3 can be written as:

\[
\sigma_{\text{rms, total}} = \sqrt{(N_1 + N_2)\sigma_{\text{cell}}^2 + \sigma_{\text{ref}}^2 + 2\sigma_{\text{Start}}^2} \tag{4}
\]
It can be seen from (4) that the rms jitter increases with the number of delay cells. Meanwhile, increasing the number of delay cells as predicted by (1), results in a higher measurement resolution.
B. Prototype circuit fabrication

The proposed time measurement solution was implemented using TSMC 0.18um CMOS process as a proof of concept. The Cadence simulation environment was used to design and simulate the circuit. Fig. 2.5 shows the chip layout and a microphotograph of the fabricated prototype. The layout of the designed TDC has a compacted size of $65\mu m \times 425\mu m$.

The building blocks of the circuit which consists of Voltage Controlled Delay Lines (VCDLs), phase detectors, and charge pumps and a 20-bit TDC are highlighted in Fig. 2.5a. Two key points were considered in the delay chains’ fabrication. First, the delay lines were fabricated as close as possible to each other and necessary measures were taken to ensure symmetrical layout in order to minimize the delay mismatch between the TDC delay-lines. Second, the delay cell routing and placements were performed to ensure identical path lengths for both DLLs and delay lines in the TDC.

A reference clock of 100 MHz clock (10ns) was used to test the circuit. Extra delay cells were added to the delay-lines to ensure that the DLLs can capture the lock. The total number of $N_2=70$, and $N_1=65$ delay cells were implemented in the delay lines.

2.5. PVT VARIATION ANALYSIS

In order to investigate the effect of process variations on the performance of the proposed TDC versus a conventional TDC, corner analysis for fast-fast (ff), slow-slow (ss) and typical-typical (tt) transistors were performed. To evaluate the effect of power supply variation, the supply voltage varied by $\pm 15\%$ from its nominal value of 1.8V. The implemented time measurement circuit is designed to operate from -50ºC to +75ºC.
Simulations were performed in the desired range of temperature variation to evaluate the TDC performance. The effect of temperature variations was also verified through measurements using the fabricated prototypes.

Table 2.1 shows the range of PVT variations used to conduct simulations and measurements to verify the performance of the proposed TDC for short-time measurements which is 126 simulation points in total. The details of the results are discussed in the following section.

![Graph showing variation of transfer propagation delay for a single delay cell with ±15% variation of power supply voltage from 1.8, at 27°C temperature.]

**Fig. 2.6.** Variation of transfer propagation delay for a single delay cell with ±15% variation of power supply voltage from 1.8, at 27°C temperature.
2.6. SIMULATION AND MEASUREMENT RESULTS

The propagation delay variation at the room temperature for a single delay cell with control voltage is presented in Fig. 2.6, when the supply voltage varies from 1.53V to 2.07V. The deviation of ±15% from the nominal supply voltage of 1.8V is considered to perform the simulation. Fig. 2.6 shows that the delay fluctuations become significant when the control voltage falls below 1V. It also can be seen that as the control voltage exceeds 1.4V, the variations of the propagation delay drop considerably. As a result, it can be concluded that the control voltage has to be close to the operating voltage of the TDC in order to support a higher resolution on delay changes.

The propagation delay variation of a single delay cell for three process corners (ff, tt, ss) is shown in Fig. 2.7 where the temperature varies from -50ºC to 75ºC. The delay variations
are also shown in Fig. 2.7 when the DLLs are locked. It can be seen that the delay of single
delay cell deviates by ~11ps if a conventional TDC is used, ~4ps comes from the process
variations and ~7ps is due to temperature changes. However, in the proposed TDC the
delay variations fall below 0.1 pico-second due to the DLL’s feedback loop.

Fig. 2.8 shows the delay variation versus supply voltage changes over the desired
temperature range. The propagation delay varies up to 7ps as indicated in Fig. 2.8 for a
conventional TDC. The delay fluctuation stays under 1ps for both supply voltage and
temperature variations in the proposed TDC.

To illustrate the effects of PVT deviations on the propagation delay, a 3D graph is plotted
in Fig. 2.9. The propagation delay varies from minimum of 21ps to maximum of 41ps. The
minimum propagation delay (i.e. 21ps) occurs for the fast-fast corner when the power
supply voltage takes the maximum value (2.07V) and the temperature falls to the minimum value (-50 °C). The maximum propagation delay happens for the slow-slow corner when \( V_{DD} = 1.53V \), \( \text{Temperature} = 75^\circ\text{C} \) shown on the top left corner in Fig. 2.9. Experimental measurements were performed to confirm the simulation results. The test setup is shown in Fig. 2.10a. The measurement setup includes an HP 81130A as a precise pulse generator and an MDO 4104 oscilloscope from Tektronix. HP81130A can provide two precise clocks up to 400MHz. A reference clock of 100MHz was used to perform measurements. For simplicity Start signal was connected to the reference clock during the measurements. Fig. 2.11 shows the measurement and simulation results of delay changes versus supply voltage variations. It can be seen that the measurement results follow the simulation results with a slight variation. Two reference clocks with time intervals from zero to 300ps are applied to measure the transfer function, the differential non-linearity (DNL) and the integral non-linearity (INL) of the TDC. The DNL and INL are both measured 0.5
and 4 LSB, respectively. The output codes of the TDC are shown in Fig. 2.10a. It can be seen that the digital outputs, Q12 to Q20, of the TDC are logic “0” for a time interval of ~150ps. The TDC presents a 15ps time measurement resolution. Table 2.2 compares the performance of the proposed circuit with the reported designs in the literature. The results indicate that the proposed circuit achieves comparable performances in LSB, dynamic
range and power consumption parameters while presenting a robust performance against PVT variations.

Table 2.2. Comparison table of proposed scheme with recent published delay line based TDCs.

<table>
<thead>
<tr>
<th>Ref.-Year</th>
<th>Technology</th>
<th>LSB</th>
<th>Speed</th>
<th>DR</th>
<th>DNL</th>
<th>INL</th>
<th>Power</th>
<th>Area</th>
<th>Application</th>
</tr>
</thead>
<tbody>
<tr>
<td>Unit</td>
<td>nm</td>
<td>ps</td>
<td>Hz</td>
<td>ns</td>
<td>LSB</td>
<td>LSB</td>
<td>mW</td>
<td>mm²</td>
<td></td>
</tr>
<tr>
<td>[11], 2013</td>
<td>CMOS-65</td>
<td>3.75</td>
<td>200M</td>
<td>0.45</td>
<td>0.9</td>
<td>2.3</td>
<td>3.6</td>
<td>0.02</td>
<td>ADPLL</td>
</tr>
<tr>
<td>[12], 2013</td>
<td>CMOS-350</td>
<td>1.76</td>
<td>300M</td>
<td>1.8</td>
<td>0.6</td>
<td>1.9</td>
<td>115</td>
<td>2.83</td>
<td>PET</td>
</tr>
<tr>
<td>[13], 2012</td>
<td>CMOS-350</td>
<td>8.88</td>
<td>-</td>
<td>-</td>
<td>74000</td>
<td>1</td>
<td>20.8</td>
<td>85</td>
<td>8.88 ToF Ranging</td>
</tr>
<tr>
<td>[14], 2014</td>
<td>CMOS-65</td>
<td>1.12</td>
<td>250M</td>
<td>0.56</td>
<td>0.6</td>
<td>1.8</td>
<td>15.4</td>
<td>0.14</td>
<td>ADPLL</td>
</tr>
<tr>
<td>[15], 2017</td>
<td>CMOS-130</td>
<td>1.74</td>
<td>10M</td>
<td>-</td>
<td>0.41</td>
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<td>2.4</td>
<td>0.06</td>
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<tr>
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<td>50M</td>
<td>-</td>
<td>1.7</td>
<td>4</td>
<td>0.3</td>
<td>0.01</td>
<td>ADPLL</td>
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<tr>
<td>Proposed scheme</td>
<td>CMOS-180</td>
<td>15</td>
<td>100M</td>
<td>500</td>
<td>0.7</td>
<td>4</td>
<td>75</td>
<td>0.028</td>
<td>Fault Detection</td>
</tr>
</tbody>
</table>

Fig. 2.11. Measured delay changes vs. simulation results with power supply voltage variation from -15% to 15%.
2.7. CONCLUSIONS

A high resolution and accurate on-chip measurement circuit is needed to test new generation of integrated circuits in order to detect possible parametric faults and hardware Trojans. PVT variations limit the resolution of on-chip measurement methods considerably. In the proposed measurement solution two delay locked loops are utilized to implement a Vernier delay line based TDC. The proposed solution presents a robust performance against PVT variations due to the internal feedback of the DLLs. Measurement results on a fabricated prototype indicate that the delay associated with each delay cell in a conventional Vernier delay line changes by more than 3ps when the power supply voltage varies by ±15%. In the proposed scheme, the deviations of a cell delay due to the process and temperature variations are reduced to less than 0.3ps, more than tenfold attenuation. Experimental measurements using a fabricated prototype on CMOS 0.18µm process are in good agreement with the simulation results and present improved performance against PVT variations.

REFERENCES


Chapter 3

A PVT Resistant Coarse-Fine Time-To-Digital Converter

3.1. INTRODUCTION

Precise time interval measurement is essential for many applications such as biomedical imaging, range estimations using Time-of-Flight [1], and parametric fault detections in integrated circuits. New generations of integrated circuits such as Through Silicon Vias (TSV) based 3D ICs present new testing and manufacturing challenges. To detect TSV manufacturing defects affecting propagation delay, on-chip time-intervals have to be accurately measured by a high-resolution measurement module [2].

The main solutions for on-chip time measurement include delay-lines, pulse shrinking circuits, Vernier delay lines, time stretching modules, and DLLs. Generally, increasing measurement resolutions reduces the dynamic range of measurement. For certain applications such as fluorescence lifetime imaging microscopy, a high-resolution measurement over a wide dynamic range is required [3]. While meeting the design requirements for sub-picosecond resolutions by itself is a challenging task, supporting a
high-resolution measurement over a wide dynamic range presents a more difficult problem to solve.

A single stage TDC has a limited dynamic range, while a TDC utilizing a differential Vernier delay line (VDL) [1] supports a high-resolution time measurement. Various coarse-fine time interval measurements have recently been proposed to support a high-resolution measurement over a wide dynamic range. In [4], a time amplifier is used to support a 1.25ps measurement resolution. A coarse-fine TDC implementation in 0.18 μm CMOS process is presented in [5], which can measure, up to 225ps with a 1.05ps resolution.

Theoretically a Vernier delay line can support sub-picosecond resolution however in practice, the resolution is limited by noise and variations of Process, supply Voltage, and Temperature (PVT). Fluctuations in fabrication parameters and changes in temperature and supply voltage affect the operating point of transistors and the accuracy of TDC circuits. Process variations change the threshold voltage of transistors and consequently the switching behavior of delay-cells in delay lines. Variations of power supply change the voltage level for switching in delay cells and affects their propagation delay. Temperature variation also affects the speed of delay cells and consequently the measurement resolution. A sub-picosecond on-chip time measurement requires a TDC with a robust performance against PVT variations.

In this paper, a new coarse-fine two-stage TDC controlled by two DLLs is proposed. The first stage utilizes a delay line based TDC to coarsely quantize the input time-interval. The output of the first stage is used to feed a Vernier delay line with a high measurement
The delay cells in both coarse and fine stages of measurement are controlled by delay-locked-loops to minimize the effects of PVT.

The rest of the paper is organized as follows. The operation principle of the proposed scheme is presented in section II. The calibration process to compensate nonlinearities is covered in section III. Simulation results and PVT effects on the measurement resolution are discussed in section IV. Finally, section V concludes the results.

### 3.2. Proposed DLL Based Coarse-Fine Time to Digital Converter

#### A. Concept description

Fig. 3.1 shows the conceptual block diagram of the proposed scheme. It includes two TDCs; the first one measures the input interval with a coarse resolution of $\tau_1$. The output of TDC$_1$ in Fig. 3.1 is applied to TDC$_2$ which has high resolution time interval.
measurement by $\tau_1 - \tau_2$. The schematic diagram of the employed VDL based TDC is shown in Fig. 3.2. The “Start” signal is applied to a voltage controlled delay line (VCDL) with a propagation delay of $\tau_1$ and the “Stop” signal is applied to another delay line with $\tau_2$. The difference between the rising edges of the “Stop” and “Start” signals reduces by $\tau_1 - \tau_2$ after each stage. The output of flip-flops connected to the delay lines remain logic
low as long as the Start signal is behind the Stop signal. When the Start signal passes the
Stop signal, the output of the flip-flop \(Q_n\) becomes the logic high. The timing diagram of
TDC2 is shown in Fig. 3.2.

The resolution and the accuracy of the TDC in Fig. 3.2 varies considerably with PVT
variations. To minimize the effect of PVT, a DLL can be used to ensure that the propagation
delay remains constant in the delay-cells regardless of PVT variations. The TDC in Fig.
3.2 is used as a sub-block, marked as TDC2, in the proposed solution as shown in Fig. 3.3.
TDC2 is used to support high-resolution measurement. Another TDC, TDC1 in Fig. 3.3, is
utilized for coarse measurement. Both TDCs are connected to DLLs to ensure the
robustness against PVT variations.

The number of flip-flops with logic low in TDC1 represents the coarse delay difference
between the Start and the Stop signals. The output of TDC1 is connected to TDC2 for fine
measurement resolutions. To feed a delayed version of “Start”, “Start\(_{dn}\)” signals in Fig 3.3,
a multiplexer (MUX1) is used. The inputs of the multiplexer are connected to the delayed versions of the “Start” signal, which are “Start_{d1}” to “Start_{dN}”. The multiplexer output is selected based on the output of the coarse TDC. To compensate the delay added by the multiplexer to the path of the Start signal, another multiplexer (MUX2) with the same propagation delay has been added to the path of the Stop signal as indicated in Fig. 3.3.

**B. Resolution**

The DLLs in Fig. 3.3 are fed with reference external clocks. Due to the inherent feedback of DLL systems, the propagation delay of each cell at the locked state remains constant regardless of PVT variations. The control voltage of the delay cells in the DLLs are connected to the control voltage of the delay cells in the TDCs. As a result, the propagation delay of the delay cells in the TDCs will also remain independent of PVT variations. The propagation delay of cells in a free running delay line is affected considerably by PVT variations while the propagation delay of the cells in a DLL remains constant in the locked state.

When the DLLs in Fig. 3.3 are locked, the resolution of the coarse ($t_{RC}$) and fine ($t_{RF}$) blocks can be determined from:

\[
t_{RC} = \tau_1 \tag{1}
\]

\[
t_{RF} = \tau_1 - \tau_2 \tag{2}
\]
where $\tau_1 = T_{ref1}/N_1$, $\tau_2 = T_{ref2}/N_2$, $N_1$, and $N_2$ are the number of gates of the delay lines in DLL1 and DLL2, and $T_{ref1}$ and $T_{ref2}$ are the period of $Ref_1$ and $Ref_2$ clocks, respectively. Therefore, the highest resolution that can be achieved is given by:

$$t_{RF} = \frac{T_{ref1}}{N_1} - \frac{T_{ref2}}{N_2} = \frac{(N_1+K)T_{ref1}-N_1T_{ref2}}{N_1(N_1+K)} \quad (3)$$

where $K$ is the number of delay cells in the second delay line, DL2. The measurement resolution of TDC2 can be controlled by selecting two main parameters. First, by choosing two different reference frequencies with a slight difference, one can control $T_{ref}$ on both DLLs. Second, the resolution can also be controlled by using a different number of delay cells in the delay line of DLL2. This will lead to a faster path for “Stop” signal than “Start” signal. Also, by selecting a different number of TDC elements including DFFs and their associated delay cells, the number of bits on coarse and fine blocks can be determined. This configuration supports a programmable measurement range.

The dynamic range of the circuit is determined by the coarse block TDC1 which can be extended by adding more delay cells to TDC1. It is possible to apply the same clock to both DLLs if a different number of delay cells are selected in each DLL.

**C. Dynamic Range**

The dynamic range of the proposed fine Vernier based TDC with M delay cells in the delay line is defined by

$$t_{DR,Fine} = M \times (\tau_1 - \tau_2) = M \times \left(\frac{T_{ref1}}{N_1} - \frac{T_{ref2}}{N_2}\right) \quad (4)$$

The overall dynamic range can be determined from the dynamic range of the coarse TDC which is given by:
\[ t_{DR, coarse} = N \times \tau_1 \]  

(5)

From (5) the dynamic range can be controlled by changing \( N \) or the number of delay cells in the coarse block, TDC1.

**D. Jitter Performance**

In practice, the resolution of the proposed circuit is limited by jitter performance of the DLLs. The RMS jitter of a DLL can be determined from the jitter of a single delay cell, \( \sigma_{jitter} \) as described in [6]:

\[ \sigma_{DLL} = \sqrt{N} \sigma_{jitter} \]  

(6)

The measurement error in the \( n \)th stage of a Vernier delay line is calculated from:

\[ \sigma_n = \sqrt{n \left( \frac{\sigma^2_{DLL1}}{N_1} + \frac{\sigma^2_{DLL2}}{N_2} \right)} \]  

(7)

where, \( \sigma^2_{DLL1} \) and \( \sigma^2_{DLL2} \) are the jitter of DLL1 and DLL2, respectively. For \( K = 1, N = N + 1 \), and assuming \( \sigma^2_{DLL1} = \sigma^2_{DLL2} \) for \( N \gg 1 \), the Vernier delay line error can be calculated from:

\[ \sigma_n = \sqrt{n \left( \frac{\sigma^2_{DLL}}{N} \right)} \sigma_{DLL} \]  

(8)

The resolution margin is limited by the number of delay cells and jitter performance of the total delay line. It can be seen from (8) that the resolution can be increased using a high frequency clock or choose a large number of delay cells in the DLL.

**E. PVT Performance**

Different parameters in the fabrication process can cause device performance variations. For instance, the exposure time results in different lengths and widths for transistors, which affect their parasitic capacitances. To study the effects of process variations on the
conventional and the proposed time-to-digital converter, the performance of both circuits have been investigated by using transistors’ parameters on slow-slow, fast-fast and nominal corners. The delay sensitivity with the supply voltage variations is given by [7]:

\[ S_{\Delta V_{DD}} = \lim_{\Delta V_{DD} \to 0} \frac{\Delta \tau_D / \Delta V_{DD}}{V_{DD}} = \frac{V_{DD}}{\tau_D} \cdot \frac{\Delta \tau_D}{\Delta V_{DD}} \]

Temperature variations affect the switching threshold voltage of transistors. The threshold voltage variations can be determined from

\[ V_{TH}(T) = V_{TH}(T_r) - k_{vt}(T - T_r) \]

where \( T_r \) is room temperature and \( k_{vt} \) is a constant value between 1-2 mV/K. The threshold voltage decreases as temperature increases which leads to a lower gate propagation delay.

### 3.3. Calibration Process

One of the main issues of delay-line based TDCs is the different delay values for each delay-cell which causes different quantization levels. The Integral Nonlinearity (INL) and the Differential Nonlinearity (DNL) are used to characterize the linearity performance of a TDC. This nonlinearity causes TDC quantization error.

Different calibration methods can be used to minimize the nonlinearity effects. To fine tune, a direct calibration method can be used for the proposed TDC in this work. In direct calibration methods, two external signals with a precise delay difference between them (Tin) are applied to each TDC [9]. The applied time-interval is increased by a small value of \( \varepsilon \) at each step and the output of the TDC is recorded. The result of such a measurement is used to minimize the nonlinearity effect.
3.4. SIMULATION RESULTS

To verify the proposed time interval measurement, the circuit in Fig. 3.3 was implemented in Advanced Design System (ADS) environment using TSMC 65nm CMOS technology. The parameters of \( N = 15 \) and \( f_p = 10\text{MHz} \) were selected to perform simulations. Fig. 3.4 shows the performance of the proposed TDC compared to the conventional VDL based TDC when the supply voltage changes by ±15%. Delay values have been measured in the circuit by applying power supply voltages from 0.85V (-15%) to 1.15 (+15%). It can be seen that the delay varies by ±3ps in the conventional VDL based TDC while in the proposed circuit, the variations are in the range of 0.1ps. Fig. 3.5 shows the performance of the proposed method with the process and temperature variations using slow-slow (ss),

![Delay Changes vs Power Supply Variation](image-url)

Fig. 3.4. Propagation delay variation of a delay cell with variation of power supply voltage for circuits operating at \( V_{dd}=1\text{V} \), the proposed circuit less than 0.1% for supply voltage variations of ±15%. 

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typical-typical (tt) and fast-fast (ff) transistors for corner analysis. It can be seen that the propagation delay of the delay cells for each corner changes by more than 5ps in the conventional TDC. In the proposed method for all three corners of ss, tt and ff, the propagation delay becomes almost equal and variations with temperature from -40º to 100º falls to less than a 0.1ps. This is due to the internal feedback of the employed delay-locked loops where the delay of each delay cell is adjusted to a certain value through the feedback in the DLL systems.

3.5. CONCLUSION

An accurate short time measurement circuit is needed for a wide range of applications including parametric fault detection on the new generation of integrated circuits such as
3D ICs. The accuracy and resolution of on-chip time measurement is heavily affected by process, supply voltage and temperature variations. In this work, a new on-chip time-to-digital converter is presented to support a high measurement resolution. In the proposed circuit, two delay-locked-loops are utilized to minimize the effects of PVT variations on the measurement results. Simulation results using TSMC 65nm CMOS technology indicate that the delay of each delay cell in a conventional Vernier delay line changes by more than four picoseconds when the power varies by ±15%, while in the proposed circuit under the same simulation conditions the delay variation of each cell remains less than a few femtoseconds. Likewise, in the proposed measurement scheme the deviations of a cell delay due to process and temperature variations are attenuated significantly due to the DLLs’ internal feedback.

REFERENCES


Chapter 4

A Hardware Trojan Activity Magnifier

4.1. INTRODUCTION

The fabrication process of Integrated Circuits (ICs) are outsourced to external manufacturers across the globe to reduce the costs of fabrication. Untrusted third-party firms can insert malicious circuits, called Hardware Trojans (HTs) into the fabricated chips. Hardware Trojans can leak critical information or cause catastrophic damages to electronic devices. Hardware Trojans are difficult to detect using manufacturing tests as they may not get activated in the test phase.

Different methods, such as circuit delay analysis, Trojans full activation, probabilistic analysis, design characteristics extraction, thermal profile tracking, and power mapping methods have been proposed for hardware Trojan detection [1]-[5]. Power fingerprints have been used to detect a Trojan in presence of various noise sources [6]. In this method, a series of random patterns are applied to the Circuit Under Test (CUT) to identify Trojan. In [7] a method using power supply transient responses is presented to detect Trojans. The authors have investigated the detection sensitivity in the presence of measurement noise.
and background switching activities. A calibration technique is developed to accurately compare the CUT responses with a golden reference circuit. In [8], a partitioning method is proposed to enhance the chance of Trojan detection in which the CUT is divided into sub-circuits to limit the search area for Trojans. Power analysis which is commonly used for side-channel attacks can be utilized to detect Trojans. In most of the available methods, it is assumed that a Trojan footprint exceeds the background noise. However, this assumption is not fulfilled if the Trojan is designed to have a minor signature. This is true particularly for new technologies such as 3D ICs where the background noise on the supply is relatively high due to multi die bonding.

Side channel attacks using power analysis are widely used by attackers to identify crypto-cores and extract their critical on-chip information [9]-[11]. The footprint of switching activities on the power supply rail is used by attackers to identify crypto-cores and extract on-chip information [12]. While power analysis is commonly used to perform side-channel attacks [13], it can also be used to detect Trojan activities. To avoid easy Trojan detection, an adversary may design a Trojan with a negligible impact on the power lines. A Trojan footprint on the power lines can be masked by various sources, including circuit noise, cross talk, ambient noise, and other random variations that manifest themselves on the supply line during the circuit operation. A Trojan footprint on the supply rails has to be greater than the noise level on the supply path, otherwise it becomes impossible to detect it through power analysis. To overcome this problem, circuit partitioning methods are proposed to improve Trojan detection rate by splitting the CUT into multiple regions. Partially activating a circuit can increase Trojan-to-circuit switching activity and raises the Trojan-to-circuit power consumption [14]. There are various partitioning techniques
among them clock gating is a popular technique which is commonly used to limit the
dynamic power consumption in synchronous circuits [15],[16]. The main drawback for the
partitioning method is the fact that increasing the number of partitions may result in a
Trojan split between different partitions where the Trojan is partially activated.
In this paper, a new method is presented to ensure that Trojan activities are not masked by
the background noise. In the proposed solution, a Trojan imprint on the supply path is first
amplified and then the Trojan is identified through detection techniques. If the Trojan
imprint on the supply rail is considered as the desired signal, the proposed method improves
the signal-to-noise ratio and increases the probability of Trojan detection. To detect a
Trojan in this work, the phase and the power of the spikes created by a Trojan on the power
lines are measured. The ISCAS’85 benchmark circuit [17] is used to verify the performance
of the proposed solution. The rest of the paper is organized as follows. Section II explains
why switching activities of digital circuit leave a footprint on the power supply lines. The
proposed Trojan detection solution is presented in section III. Section IV and V presents
the simulation and measurement results, respectively. Finally, the conclusions are
summarized in section VI.

4.2. BACKGROUND

There are many sources of noise in circuits that corrupt the supply voltage including cross
talk, leakage current, charge sharing and mismatch, however the main contributor to the
supply voltage fluctuation in digital circuits is the switching activates.
A. Switching profile on the power supply lines

To understand the nature of switching footprint on the supply path and explain the proposed solution, the operation of an inverter at the transistor level is analyzed. For the inverter shown in Fig. 4.1a, the path that connects the inverter to the supply voltage can be modeled by an inductor, $L$ and a resistor, $R$ as shown in Fig 1b. Initially we assume that the circuit is in the steady state with logic high at the input where M2 is ON and M1 is OFF. If the input state changes to logic low, M2 turns off and M1 turns on and the output experiences a transition. The transition from logic-low to logic-high at the output happens typically in a few picoseconds. During the output transition for a short period of time both M1 and M2 turn on and a direct path from VDD to ground opens. As a result, the current drawn from

![Fig. 4.1. (a) a CMOS inverter. (b) Simplified equivalent circuit.](image)
the power supply path suddenly rises. Assuming that the current variation during the transition is represented by \( \Delta I \) and the time it takes is represented by \( \Delta t \), the voltage across the inductor, \( V_L \) can be calculated from \( V_L = L(\Delta I/\Delta t) \). \( L \) and \( \Delta I \) depend on many factors and their range of variations can be considerably different from one circuit to another. For a typical CMOS integrated circuit, \( L \) can be a few nano-henry and \( \Delta I \) can be a few milliamps. Assuming \( \Delta t \) is a few picoseconds, the voltage drop across the inductor can vary from a few millivolts to tens of millivolts. The voltage across the inductor creates spikes on the supply line whenever signal transitions happen at the inverter output. From this observation, two important points can be concluded which are (a) switching activities at the output of logic gates fluctuate the supply voltage and (b) the fluctuation level increases as the supply path inductance rises. Many design techniques have been developed to reduce or eliminate the effects of switching activities on the supply lines to protect circuits against side channel attacks. If the effect of switching activities on the power supply path can be used by adversaries to extract critical on-chip information, it can also be used against them by circuit designers to identify malicious activities of Trojans.

### 4.3. Proposed Trojan Detection Solution

In this work contrary to the common approach against power–based side-channel attacks, the footprint of switching activities is intentionally amplified in the test phase to have a better Trojan visibility and detect possible malicious circuits. From \( V_L = L\Delta I/\Delta t \) it can be seen that there is a linear relationship between the voltage of switching spikes on the power
supply lines and the inductance. An external inductor can be added to the power supply path in the test phase to amplify the switching footprint. The inductor has to be chosen properly to ensure that the supply voltage fluctuations remain in the boundary defined by $V_{DD} \pm 10\%$ to ensure circuit functionality.

A. **Transfer function of switching activities**

The basic analysis in the previous section reveals that the power supply lines are affected by switching activities, however it does not reveal the transient response of the supply path to the switching activities. In this part, a transfer function to specify the effects of logic gate activities on the supply lines is developed. Fig. 4.2a indicates a digital gate or a CUT which is connected to the supply voltage. The $L$ and $R$ in the circuit represent the inductance and resistance of the supply path respectively. $C_s$ and $C_L$ are the parasitic

---

Fig. 4.2. (a) Circuit model for a device-under-test connected to the power supply. (b) Equivalent circuit model.
capacitances of the power supply and the CUT. During the transition from high-to-low or from low-to-high, \( \Delta I \) current passes from the supply to the ground. To determine the variation of the supply voltage across the load after a switching, the response of the equivalent circuit in Fig. 4.2b to \( \Delta I \) is calculated. The load voltage variation, \( \Delta V \), is given by \( \Delta V = \Delta I \cdot Z_{in} \) where \( Z_{in} \) is the impedance seen by the load and determined from:

\[
Z_{in} = (Ls + R)\frac{1}{Cs}
\]  

(1)

Substituting (3) in (2), the transfer function of \( \Delta V_{DUT}/\Delta I \) can be calculated from:

\[
\frac{\Delta V_{DUT}}{\Delta I}(s) = \frac{LS+R}{LCS^2+RCS+1}
\]  

(2)

Eq. (2) represents a second order system with a zero at \(-L/R\) and two poles at \( p_{1,2} = \omega_n[-\xi \pm \sqrt{\xi^2 - 1}] \).

where \( \xi = \frac{R}{2} \sqrt{\frac{C}{L}} \) and \( \omega_n = \frac{1}{\sqrt{LC}} \). For typical values of \( L \) and \( R \), the zero is excited at lower frequencies and as the frequency increases and becomes closer to the natural frequency, \( \omega_n \), the poles are excited. For \( L = 10\text{nH}, R = 1\Omega, \text{ and } C = 0.2\text{pF} \) the poles are located at \( p_{1,2} = 10^{-10}(-0.005 \pm j3.16) \) while the zero is located at \( z = -10^6 \). The magnitude and the phase responses of such a system is shown in Fig. 4.3. It can be seen that the system behaviour is initially dominated by the zero and the system presents a high pass filter response. At high frequencies where the poles are excited the high pass effect of the zero is cancelled out and the system becomes a low pass filter. It can be seen that the gain has a sharp peak as the frequency approaches \( \omega_n \). Inserting a Trojan to a circuit not only can affect the switching footprint on the supply paths but also can reduce the load resistance. The leakage current consumed by the Trojan changes the load current and varies the total resistance, \( R \), in the equivalent circuit accordingly. Thus, a Trojan can be detected by
monitoring the amplitude of the spikes on the supply voltage lines as well as the delay variations of the spikes. To evaluate the performance of the proposed solution and examine the time domain responses, an inverter from CMOS 0.18μm technology is used to conduct transient simulations in Cadence environment. Fig. 4.4 shows the switching footprint of
the inverter when different inductors are inserted in the power supply path. It can be seen that the amplitude of the spikes rises as the inductance increases. These results are in good agreement with the results predicted by the transfer function in Eq. (2).

**B. Proposed technique in the presence of noise**

Detecting a Trojan from its switching effects on the supply lines is challenging particularly in the presence of circuit noise. If a Trojan footprint on the supply rail falls below the noise
on the supply rail, it becomes impossible to detect the Trojan. To overcome this limitation, the Trojan switching footprint has to be amplified without increasing the noise on the supply rail. It is shown in this section that this objective can be achieved by adding an inductor to the supply rail. This minor circuit modification, increases the signal-to-noise ratio (SNR) by a factor of \((Q)^2\) at frequencies lower than the natural frequency, \(\omega_n\). \(Q\) is the quality factor of the added inductor. Such a significant SNR improvement allows the detection of malicious switching activities by Trojans. In the following analysis, the switching footprint of a Trojan on the supply rail is considered to be the desired signal and the noise in the circuit is assumed to be dominated by the thermal noise.

Fig. 4.5(a) shows a simplified circuit model for a digital gate connected to a supply voltage. It is initially assumed that the supply path presents just ohmic resistance, \(R\), and no inductance. The capacitor, \(C\) in the model represents the gate’s parasitic capacitance. The supply voltage variation, \(\Delta V_{out}\), due to the switching activities can readily be calculated from

\[
\Delta V_{out}(s) = R\Delta I /(RCs + 1)
\]

(3)

The equivalent circuit for noise power calculation is shown in Fig. 4.5(b) in which \(R_n\) is the equivalent noise resistance of the device-under-test. For the equivalent circuit in Fig 5(b) which includes a capacitor and a resistor the power of the noise [18] at the output is given by \(kT/C\), where \(k\) is the Boltzmann factor and \(T\) is the temperature. The maximum SNR in this case is given by

\[
SNR_1 = (R\Delta I)^2 / (kT/c)
\]

(4)
If an inductor is added to the circuit as shown in Fig. 4.4c, the output voltage variations, $\Delta V_{out}$, at frequencies lower than $\omega_n$ can be calculated from Eq.(2). For a frequency range of $f_z < f < \omega_n/2\pi$, the system represented by the transfer function
in Eq. (2) behaves like a high pass filter due to the zero in the system and the response can be estimated by

$$\Delta V_{DUT}(s) \approx \Delta I (Ls + R)$$  \hspace{1cm} (5)$$

where $f_z$ is the frequency of the zero in the transfer function. Thus $\Delta V_{out}(s)$ can be determined from

$$\Delta V_{out}(s) = \Delta I |Ls + R| \rightarrow \Delta V_{out} = \Delta IR \sqrt{1 + (L\omega / R)^2}$$  \hspace{1cm} (6)$$

For $Q = L\omega / R > 4$, we have $\Delta V_{out} \sim Q \Delta I R$. The total power of the noise in this case does not change considerably and still can be estimated by $kT/C$. This is due to the fact that the area under the transfer function which defines the noise bandwidth does not change considerably. Thus, the signal to noise ratio can be estimated by

$$SNR_2 \sim (QR\Delta I)^2 / (kT/C) = Q^2 SNR_1$$  \hspace{1cm} (7)$$

It can be seen that the added inductor has increased the signal-to-noise ratio by a factor of $Q^2$. As the frequency approaches $\omega_n$, the SNR improvement becomes even more significant. The magnitude of the transfer function in Eq. (2) becomes maximum at the natural frequency, $\omega_n$. At this frequency, the magnitude of the denominator takes its minimum value of $2\xi$. Thus the transfer function in Eq. (2) is simplified to

$$\frac{\Delta V_{DUT} (s)}{\Delta I} = \frac{|Lj\omega_n + R|}{(2\xi)^2} = \frac{R\sqrt{1 + (L\omega_n / R)^2}}{(2\xi)^2}$$  \hspace{1cm} (8)$$

Representing $Q = L\omega_n / R$ and considering the fact that for real circuits $L\omega_n / R \gg 1$ we can estimate the magnitude of $\sqrt{1 + (L\omega_n / R)^2}$ with $Q$ and we have

$$\Delta V_{out} \approx \Delta IRQ / 4\xi^2$$  \hspace{1cm} (9)$$
Thus, the signal to noise ratio at the natural frequency, \( \omega_n \), can be estimated by

\[
SNR_2 \sim \left( \frac{\Delta IRQ}{4\xi^2} \right)^2 / \left( \frac{kT}{C} \right) = \frac{(\Delta IR)^2}{(kT/C)(Q/4\xi^2)^2}
\]  

(10)

and thus we have

\[
SNR_2 \sim SNR_1 \left( \frac{Q}{4\xi^2} \right)^2
\]

(11)

It can be seen that the added inductor has increased the signal-to-noise ratio by a factor of \( (Q/4\xi^2)^2 \). Since \( \xi \) in a real circuit is much smaller than one, the SNR improvement in this case becomes significantly higher than the case where there is no inductor in the circuit.

C. Trojan detection procedure

In general, as the ratio of a Trojan size with respect to the main circuit decreases the Trojan detection success rate falls. This problem becomes more difficult to overcome as the technology evolves. For instance, Trojan detection in 3D ICs is more challenging as the background noise in such circuit can mask the Trojan activities. One can partition the chip to sub-regions and use separate power grid in each region to detect suspicious Trojan in the desired region [19]-[20]. The combinational or sequential Trojans can be detected by this method. The proposed solution reduces the need for the circuit partitioning. A combination of the circuit partitioning techniques and the Trojan magnification method can be employed in practice to detect Trojans. The flowchart of the Trojan detection is shown in Fig. 4.6. In this procedure, the power is applied to the selected segment through an
inductor, then the power of switching spikes is measured and compared with the measured power form the reference/golden circuit. If the power difference exceeds an acceptable level in any segment, Trojan is reported. Otherwise, the CUT is considered Trojan-free.

4.4. Simulation Results

The proposed scheme is evaluated with different Trojan sizes to see how the profile of the spikes on the supply path of the main circuit is affected. The ISCAS’85 benchmark circuits were used to conduct the experiments and verify the results. The C432 circuit from
ISCAS’85 benchmark which is a 27-channel interrupt controller is used as the main circuit. The simulations were performed in the Cadence Virtuoso design environment.

A. **Switching imprint on the power supply path vs. inductance**

In the first experiment, the effect of adding an inductor to the supply voltage path is investigated without the noise. Fig. 4.7 shows the variation of the voltage on the power supply versus different inductor values in the time domain. It can be seen that the peak of the overshoots increases as the inductance value rises. Moreover, it can be seen that the delay between the peak of the signal with respect to the rising edge of the clock increases with the inductor value. These results are in agreement with the circuit response predicted by the transfer function in Eq. (2).
B. Effect of circuit noise on the switching imprint

To study the noise effect on the proposed solution, a noise source is added to the supply path of the circuit. Fig. 4.8a, shows the results when there is no external inductor between the power supply and the circuit. The simulation results for the same circuit with 5nH, 10nH, and 15nH inductors are also shown in Fig. 4.8. It can be seen that the amplitude of the spikes increases with the inductor values. To evaluate the effect of inductance on the
power of switching imprint, the supply path inductor was varied from 0 to 15nH and the power gain for the spikes on the supply path were determined through simulation.

Fig. 4.9. (a) The ISCAS'85 C432 interrupt controller circuit used to perform simulation. (b) N-bit sequential counter inserted to the device-under-test as a Trojan.
C. Effect of Trojan on the switching imprint

Fig. 4.9(a) shows the C432 circuit from ISCAS 85 benchmark and a sequential Trojan used to perform the experiments. The C432 circuit from the ISCAS’85 is a 27-channel interrupt controller. The input channels are grouped into three 9-bit buses (we call them A, B and C), wherever the bit position within each bus determines the interrupt request priority. A forth 9-bit input (called E) enables and disables interrupt requests inside the respective bit positions. The added Trojan is an N bit counter [21] which upon trigger affects the value of its internal states or the output data as shown in Fig. 4.9(b).

To determine the power gain, the power of the spikes on the supply path with and without an inductor are determined and then the ratio of the powers are calculated. Fig. 4.10 shows the power gain of Trojan switching imprint versus the supply path inductance for different Trojan sizes. It can be seen that the power gain rises as the supply path inductance increases. In addition, it can also be seen that the power of the switching imprint rises as the ratio of the Trojan to circuit size increases. These results are in close agreement with the results of theoretical analysis. It has to be noted that a limited power gain can be achieved in this method. There is an upper limit for the inductor value since the level of the spikes on the supply line has to be limited to ensure the functionality of the circuit-under-test.

The difference between the supply voltage of the circuit-under-test and the supply voltage of the reference Trojan free circuit is used for power analysis and Trojan detection. Simulation results in Fig. 4.11 indicate the supply path voltage variation before and after the Trojan insertion and before and after adding a 10nH inductor to the supply path. It can be seen in Fig. 4.11(a) that there is a small spike at the rising edge of the clock on the
supply line when there is no inductor added to the supply line. If a Trojan is added to the same circuit as shown in Fig. 4.11(b) the switching imprint will not vary considerably. When a 10nH inductor is added to the supply path of the circuit as indicated in Fig. 4.11(c), the switching imprint becomes more prominent compared to the case where there is no inductor. In this case, if a Trojan is added to the circuit the switching imprint variation becomes significantly higher than the case without the inductor. The difference between the supply voltage variation

![Graph](image)

Fig. 4.10. The power gain of Trojan switching imprint versus supply path inductance. The gain increases as the inductance rises. A higher power gain is also achieved as the ratio of Trojan area to circuit size increases.
for both cases of with and without the inductor are determined using Cadence calculator. The results in Fig. 4.12 indicates the difference between the supply voltages of the Trojan infected circuit and the Trojan free circuit. It can be seen that the supply voltage variation when a 10nH inductor is added to the supply path becomes significantly higher. To get a performance parameter for comparison, the power of the voltage spikes for both cases of with and without the inductor are determined. The power of the signal in Fig. 4.12(a),
where the inductor is added, is about 200 times higher than the power of the signal in Fig. 4.12(b), where there is no inductor in the supply path. Such a significant improvement on the Trojan imprint can increase the visibility and the Trojan detection rate.

**D. Effect of Trojan size on the switching delay imprint**

In addition to the power of the switching activities on the supply path, the effect of Trojan on the delay can also be observed to detect a Trojan. Adding a Trojan to the circuit-under-test affects the delay difference between the rising edge of the clock and the switching imprint on the supply path as shown in Fig. 4.13. To evaluate the effect of Trojan size on the delay difference, counters with 1 to 8 cells are added to the C432 circuit as Trojans. Simulations were performed with L=10nH added to the supply path and the delay difference between the infected circuit and the reference Trojan infected circuit were
measured. The results in Fig. 4.13 shows that as the Trojan size increases, the delay difference between the responses of the Trojan free circuit and the Trojan infected circuit rises.

4.5. Measurement Results and Discussion

An experiment was conducted to verify the effect of supply path inductance on the switching imprint. The measurement setup which is shown in Fig. 4.14 includes a precise pulse generator (HP 81130A), a mixed signal oscilloscope (MDO 4104), a 30nH inductor and the circuit under test. A separate calibration was performed to cancel out the inductance of the wires connecting the circuit. In this experiment, the switching imprint on the supply was first recorded without the inductor. Then the inductor was added to the supply path.
and the experiment was repeated. A 10MHz square wave with a rising time of 1ns was applied to the input of the CUT during the measurements.

Fig. 4.15 shows the measurement results at the rising edge of the clock. It can be seen that the imprint of the switching activity without an inductor has a much lower profile compared to the case where a 30nH inductor is added to the supply path. The peak values of the signals are 872mV with the inductor and 85mV without the inductor. The second experiment is conducted to show how the supply path inductance can be utilized to have a better visibility for Trojan activates. Fig. 4.16 indicates the measurement results for the Trojan free and the Trojan infected circuit with a 30nH inductor added to the supply path. It can be seen that the phase and the amplitude of the switching imprint are both affected by the Trojan. The difference between the peak of the spikes on the supply path as shown in Fig. 4.16 is 116mV. If the inductor

Fig. 4.14. Experimental measurements setup which includes a precise pulse generator and an oscilloscope.
is removed from the supply path the difference between the amplitude of the spikes falls from 116mV to less than 10mV.

4.6. CONCLUSIONS

Side channel attack using power analysis is a known technique which relies on the switching imprint of crypto-cores on the supply path. In principle, the same technique can
be utilized to detect Trojans. However, Trojan detection is more challenging as the
signature of a Trojan can be masked by the circuit noise partially when the Trojan size
becomes much lower than the circuit size. In this work, a new method to overcome this
problem is presented. It is shown how to magnify the switching imprint without increasing
the noise. The proposed method is capable of detecting a hardware Trojan as small as 2%
of the size of the circuit under test. The magnification scale can be controlled by the
inductance value. Simulation results using the ISCAS’85 benchmark circuit indicates that
the phase and the amplitude of the switching imprint are both affected by a Trojan added
to the circuit. This is in a good agreement with the simulation and analytical results. The
effect of Trojan on the switching imprint has also been verified through experiment
measurement result. Experimental measurements indicate that the use of a 30nH inductor
on the supply path increase the amplitude of the switching imprint by more than ten folds
from 85 mV to 872 mV. Experimental measurements also indicate that a Trojan activity
affects both the phase and the amplitude of the switching imprint.

ACKNOWLEDGMENT
The authors would like to thank the research and financial support received from Natural
Sciences and Engineering Research Council (NSERC) of Canada, CMC Microsystems..

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Chapter 5

Conclusions and Future work

CONCLUSIONS

In this work, two new on-chip short-time measurement techniques have been proposed which are resilient to variations of fabrication Process, supply Voltage and the Temperature (PVT). The principle of phase locking is utilized to minimize the fluctuations of propagation delay in a Vernier-Delay Line (VDL) based Time-to-Digital Converter (TDC). The first circuit has been fabricated using 0.180 μm CMOS technology. The experimental measurement results on the prototype show that the proposed scheme can reduce the effects of PVT variations on the time measurement by more than tenfold compared to commonly used VDL based TDCs.

A fine-coarse time measurement circuit has also been proposed to cover a large dynamic range without compromising the measurement accuracy and resolution. The proposed scheme has been implemented using CMOS 65nm technology. Simulations were
conducted to evaluate the TDC performance parameters. The results indicate that the measurement accuracy varies less than 0.1ps when the supply voltage varies by 15%.

The knowledge of short-time measurement techniques was used to successfully complete an industry project and measure geometrical features of transmission parts with a high accuracy. This work resulted in a US patent in 2017 and a product in the market. The project was recognized by Ontario Centres of Excellence (OCE) and listed among the top 8 OCE funded projects in the OCE 2017 annual report. It is also reported as a success story by Canadian Microelectronics Corporation.

The proposed on-chip time measurement solution has also been used for hardware Trojan detection. A new method is presented to magnify the switching imprint of hardware Trojans on the supply path. The proposed method relaxes the requirements for hardware Trojan detection.

**FUTURE DIRECTIONS**

Hardware security has become a major security concern for IC designer across the globe. The cost of an in-house fabrication facility for new CMOS nodes is so high that quite a few companies can afford. There is just a handful of fabrication fundraise in the market, most of them in foreign countries. Companies have left with no choice other than outsourcing their fabrication needs. However, outsourcing creates opportunities for adversaries to add their hardware Trojans to fabricated circuits. Physical Unclonable Functions (PUFs) are emerged as viable solutions to enhance the hardware security.

PUFs are effective hardware primitives to many hardware security systems such as integrated circuit authentication, key storage, IC metering, and anti-counterfeiting. An
accurate and high-resolution time measurement scheme is an essential element for a reliable PUF implementation. This work can be extended to implement a robust PUF for hardware security applications.
Appendix A

US Patent:
Gage for Verifying Profile of Part and Method of Verifying Profile of Part

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Patent No.:
US 9,797,715 B2

Date of Patent:
Oct. 24, 2017

- Recognized as one of top 8 OCE supported project in Ontario (2017)
- Reported as a success story, Canadian Microelectronics Corporation (CMC), 2016
U.S. Patent No. 9,797,715
Issued October 24, 2017

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GAGE FOR VERIFYING PROFILE
OF PART AND METHOD OF
VERIFYING PROFILE OF PART

ABSTRACT
A method of verifying the roundness of a clutch hub includes placing the clutch hub adjacent a non-contact measuring device. The method includes rotating one of the clutch hub and non-contact measuring device about a central axis that is stationary relative to the non-contact measuring device. Distance measurements are measured between the non-contact measuring device and a surface of the clutch hub at discrete points along splines and slopes between the splines of the clutch hub as the clutch hub is rotated about the central axis. The method includes identifying some of the distance measurements as spline measurements associated with splines of the clutch hub. The roundness of the clutch hub is calculated based on the spline measurements.
A method of verifying the roundness of a clutch hub includes placing the clutch hub adjacent a non-contact measuring device. The method includes rotating one of the clutch hub and non-contact measuring device about a central axis that is stationary relative to the non-contact measuring device. Distance measurements are measured between the non-contact measuring device and a surface of the clutch hub at discrete points along splines and slopes between the splines of the clutch hub as the clutch hub is rotated about the central axis. The method includes identifying some of the distance measurements as spline measurements associated with splines of the clutch hub. The roundness of the clutch hub is calculated based on the spline measurements.

16 Claims, 12 Drawing Sheets
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FIG. 5
Load Clutch Hub

Rotate Clutch Hub about Central Axis of Clutch Hub

Measure Distance Measurements at Discrete Points along Splines and Slopes

Identify Some Distance Measurements as Spline Measurements

Calculate Roundness of Clutch Hub Based on Spline Measurements

FIG. 10
FIG. 11

100 Load Clutch Hub

102 Rotate Clutch Hub about Central Axis of Clutch Hub

104 Measure Distance Measurements at Discrete Points along Splines and Slopes

108 Compare Difference between Consecutive Distance Measurements with a Threshold Range

110 Categorize Consecutive Distance Measurements Inside Threshold Range as Spline Measurements and Categorize Consecutive Distance Measurements Outside of the Threshold Range as Unnecessary Measurements

122 Eliminate Unnecessary Measurements

128 Calculate Average of Spline Measurements

130 Categorize Spline Measurements above the Average as Outer Spline Measurements Categorize Spline Measurements below the Average as Inner Spline Measurements

132 Calculate Outer Roundness Based on Outer Spline Measurements and Calculate Inner Roundness Based on Inner Spline Measurements
FIG. 12
Load Clutch Hub

Rotate Clutch Hub about Central Axis of Clutch Hub

Measure Distance Measurements at Discrete Points along Spines and Slopes

Identify Some Distance Measurements as Spline Measurements

Separating at Least Some of the Spline Measurements into Discrete Data Sets Each Associated with One of the Splines

Determining an Average of the Distance Measurements for Each Discrete Data Set

For Each Discrete Data Set, Deleting Distance Measurements Below the Average of that Discrete Data Set

Calculate Roundness of Clutch Hub Based on Remaining Spline Measurements

FIG. 13
1

GAGE FOR VERIFYING PROFILE OF PART
AND METHOD OF VERIFYING PROFILE OF
PART

CROSS-REFERENCE TO RELATED
APPLICATIONS

The subject patent application claims priority to and all
the benefits of U.S. Provisional Patent Application No.
61/958,224 filed on Jul. 31, 2013, which is herein incorpo-
rated by reference in its entirety.

BACKGROUND

1. Field

The subject application is related to a method of verifying
the roundness of a part, such as a clutch hub. The subject
application is also related to a gage for verifying the round-
ness of the part.

2. Description of the Related Art

During a manufacturing process, sample parts may be
routinely removed from the manufacturing line and mea-
sured to ensure that selected dimensions fall within required
tolerances. One method of measuring parts includes the use
of a touch probe of a coordinate measuring machine (CMM).
Specifically, the touch probe is contacted with selected
surfaces of the part. Such a process can be time consuming
and, in fact, can take as much as 10-20 minutes for a part
such as a clutch hub. During the entire time that the part is
being measured, additional parts are being continuously
manufactured on the manufacturing line. As such, if it is
determined that the part is not within tolerance after the
10-20 minute measuring process, then the parts that were
manufactured during that 10-20 minute are likely also not
within tolerance and thus are scrapped, which is economi-
cally disadvantageous.

As one example, vehicle drivetrain components, e.g.,
avtomotive transmission components such as clutch hubs,
are subject to strict tolerance requirements. Such compo-
nents may include outer splines and inner splines and the
roundness of the part along these splines must be within
specific tolerances. As such, several data points are taken for
these splines with a touch probe and the roundness is
calculated from these data points. Slopes between the outer
splines and the inner splines, and designed ridges in the
outer splines and/or inner splines, are specifically not mea-
sured with the touch probe because such data points would
interfere with the roundness calculation. This process is time
consuming and is subject to operator error by requiring the
operator to only touch the touch probe to the outer splines
and inner splines without touching the slopes or designed
ridges.

Thus, there remains an opportunity to develop a measure-
ment device and method for quickly and effectively mea-
suring a surface dimension of a part.

SUMMARY AND ADVANTAGES

A method of verifying the roundness of a clutch hub
includes identifying some of the distance measurements as
spline measurements associated with splines of the clutch
hub. The method includes calculating roundness of the
clutch hub based on the spline measurements.

Accordingly, the clutch hub may be quickly and easily
measured by measuring distance measurements along both
the splines and the slopes without the need to distinguish
between splines and slopes during the measurement of the
distance measurements. Once the distance measurements
are measured, the spline measurements are identified and used
to calculate the roundness of the clutch hub. Since the
splines and slopes are not distinguished while the distance
measurements are measured, the distance measurements
may be quickly measured, thus decreasing the time and
complexity of the verification. Due to the reduction in time
and complexity, the roundness of a more frequent sampling
of clutch hubs may be verified during a production run of
clutch hubs to provide greater quality assurance.

BRIEF DESCRIPTION OF THE DRAWINGS

Other advantages will be readily appreciated, as the same
becomes better understood by reference to the following
detailed description when read in connection with the
accompanying drawings wherein:

FIG. 1 is a perspective view of a gage for verifying
roundness of a part such as a clutch hub mounted to the gage;
FIG. 2 is a perspective view of the clutch hub;
FIG. 3 is a top view of the clutch hub to identify
the splines and slopes of the clutch hub;
FIG. 4 is a magnified view of a portion of the clutch hub;
FIG. 5 is a block diagram of a portion of the gage;
FIG. 6 is a display area for displaying data associated
with the verification of the roundness of the clutch hub;
FIG. 7 is a graph of an example of distance measurements
for a clutch hub;
FIG. 8 is a graph showing an example of spline
measurements with unnecessary measurements eliminated;
FIG. 9 is a graph showing an example of outer spline
measurements and average lines;
FIG. 10 is a flow chart of a method of verifying the
roundness of the clutch hub;
FIG. 11 is another flow chart of the method of verifying
the roundness of the clutch hub;
FIG. 12 is a flow chart of a method of identifying some
distance measurements as spline measurements and identi-
fying some measurements as unnecessary measurements;
and
FIG. 13 is a flow chart of a method of eliminating distance
measurements associated with a designed ridge in a spline.

DETAILED DESCRIPTION

With reference to the Figures, wherein like numerals
indicate like parts throughout the several views, a gage 10,
i.e., a gage 10, for verifying the roundness of a part 12, such
as a clutch hub, is generally shown. The gage 10 measures
a surface dimension of the part 12 and compares the surface
dimension of the part 12 to predetermined dimensional
tolerances to determine whether the part 12 is acceptable,
i.e., within the predetermined dimensional tolerances, or
unacceptable, i.e., outside the predetermined dimensional
tolerances.

For example, the gage 10 shown in the Figures is con-
figured to measure an outer surface of the part 12 to
determine the roundness, run-out, and/or concentricity of the
outer surface. Alternatively, the gage 10 can be configured to
measure any surface of the part 12, e.g., inner surface, outer surface, etc., and any dimension of that surface, e.g., roundness, flatness, curve, RMS roundness, sector roundness, concentricity, eccentricity, eccentric angle, centre X, centre Y, average diameter, least square circle, maximum diameter, minimum diameter, minimum inscribed, and/or maximum circumscribed, etc. The part 12 shown in the Figures, and specifically in FIGS. 1-4, is a component of an automotive drivetrain such as the clutch hub, i.e., a clutch housing. However, it should be appreciated that the part 12 may be any type of part.

With reference to FIG. 1, the gage 10 includes a stage 14 for supporting the part 12, a non-contact measuring apparatus 16 that reads distance measurements of the surface dimension of the part 12, and a computer 18 coupled to at least one of the stage 14 and the measuring apparatus 16 for receiving the distance measurements. The non-contact measuring apparatus 16 may include, for example, a non-contact measuring device 32, e.g., a laser sensor, as set forth further below.

With reference to FIGS. 1-4, the non-contact measuring device 32 measures distance measurements (graphically shown as elements 28 in FIGS. 7-9) between the non-contact measuring device 32 and a surface of the part 12, e.g., the clutch hub, at discrete points along splines 66, 68 and slopes 70 between the splines 66, 68. The gage 10, e.g., the computer 18, identifies some of the distance measurements as spline measurements (graphically shown as elements 80 in FIGS. 8 and 9) associated with the splines 66, 68. The computer 18 also identifies the distance measurements other than the spline measurements as unnecessary measurements, i.e., the data points deleted between the spline measurements in FIG. 8 as compared to FIG. 7. The unnecessary measurements may be associated with slopes 70 between inner splines 66 and outer splines 68, designed holes 72, and holes 86.

The gage 10, i.e., the computer 18, may then calculate roundness of the part 12, e.g., the clutch hub 18, based on the spline measurements. In other words, the computer 18 does not use the unnecessary measurements, i.e., the measurements that are not associated with the splines 66, 68, to calculate the roundness of the part 12. As set forth below, inner spline measurements (graphically shown as elements 82 in FIG. 8) associated with an inner spline 66 may be used to calculate the inner spline roundness of the inner spline 66. Likewise, outer spline measurements (graphically shown as elements 84 in FIGS. 8 and 9) associated with the outer spline 68 may be used to calculate the outer spline roundness of the outer spline 68.

The gage 10 includes may include means, e.g., the computer 18 programmed with the filtering software described below, for performing any step of calculating the roundness of the part based on the distance measurements set forth herein. For example, the gage 10 may include means for comparing the difference between consecutive distance measurements with a threshold range and categorizing consecutive distance measurements having a distance outside of threshold range as unnecessary measurements. Specifically, the means for comparing and categorizing may be the computer 18, as set forth below, programmed with the filtering software discussed below.

The gage 10 may include means, e.g., the computer 18 programmed with the filtering software, for eliminating distance measurements other than the spline measurements. Specifically, the gage 10 may include means, e.g., the computer 18 programmed with the filtering software, for comparing the difference between consecutive distance measurements with a threshold range and categorizing consecutive distance measurements having a distance outside of threshold range as unnecessary measurements.

With reference to FIG. 1, the stage 14 may include a rotary turntable 22 and a chuck 20 on the rotary turntable 22 for engaging the part 12. The rotary turntable 22 may include a stationary base 24 and a rotatable platform 26 that is rotatable relative to the base 24 and supports the chuck 20. The rotary turntable 22 can be, for example, of the type commercially available from Aerotech Inc. of Pittsburgh, Pa., USA under the name APR2000DR-155. The stationary base 24 may be mounted to a table 28, as discussed further below. The rotary turntable 22 may include a controller.

The chuck 20 may be configured to releasably engage the part 12. The chuck 20 may be configured to be releasably engaged to releasably engage several different parts 12 having varying sizes. With reference to FIG. 1, the chuck 20, for example, may be a mechanical jaw chuck 20 that includes jaws that are moveable radially for engaging/disengaging the part 12. Alternatively, the chuck 20 may be any type of device for releasably holding the part 12 on the rotary turntable 22.

With continued reference to FIG. 1, the measuring apparatus 16 includes a stand 30 and a non-contact measuring device 32 mounted to the stand 30. The stand 30 is mounted to the table 28. As shown in FIG. 1, the measuring apparatus 16 is typically spaced from the stage 14 and the non-contact measuring device 32 is spaced from the part 12 and the stage 14, i.e., does not contact the part 12 or the stage 14, during measuring.

The stand 30 is adjustable to adjust the position of the non-contact measuring device 32 relative to the part 12 to accommodate parts 12 of varying size. Specifically, the stand 30 is linearly adjustable along two axes A1, A2, and more specifically, vertically and toward/away from the part 12. The stand 30 can include meters 34 for measuring the adjustment of the non-contact measuring device 32 along the two axes A1, A2.

In an alternative embodiment not shown in the Figures, the stand 30 includes motorized segments that are adjustable by the computer 18. In such a configuration, the computer 18 is programmed with dimensions of several parts 12 of varying size each having a unique identifier. The user inputs the identifier into the computer 18 and the computer 18 instructs the motorized segments of the stand 30 to automatically adjust to accommodate the identified part 12.

The non-contact measuring device 32 is configured to measure distance measurements between the non-contact measuring device 32 and the part 12. The non-contact measuring device 32 may be connected to the computer 18 to transfer the measurements from the non-contact measuring device 32 to the computer 18. The non-contact measuring device 32 may be a laser sensor, as shown in FIG. 1. The laser sensor may be a displacement triangulation laser. For example, the non-contact measuring device 32 may be of the type commercially available from Keyence Corporation of Osaka, Japan under the name LK-H1022. Alternatively, the non-contact measuring device 32 may be any type of displacement laser or confocal light.

One of the stage 14 and the non-contact measuring device 32 may be configured to provide relative rotation between the part 12 and the non-contact measuring device 32 for measuring distance measurements about the part 12, e.g., the clutch hub. Specifically, at least one of the stage 14 and the non-contact measuring device 32 rotates relative to the other to move the surface of the part 12 relative to the non-contact measuring device 32 for measurement of the surface dimension of the part 12. For example, in the embodiment shown
interface 44, which initiates rotation of the rotary turntable 22. Alternatively, the user may initiate the measurement by flipping a switch, to initiate rotation of the rotary turntable 22 relative to the stationary base 24 and the associated data collection.

The method includes rotating one of the part 12, e.g., the clutch hub, and non-contact measuring device 32 about the central axis A of the part 12, as shown in block 102 of FIG. 10. The method includes tracking the rotational position of the part 12 on the stage 14, e.g., by monitoring the rotational position of the rotary turntable 22 relative to the stationary base 24 with the rotary encoder. The method includes sending a signal from the stage 14, e.g., the rotary encoder, to the control unit 36, e.g., the processor 38, at predetermined rotational intervals. For example, the method includes sending a signal from the stage 14 to the control unit 36 at every 0.1 degree of rotation of the rotary turntable 22 relative to the stationary base 24.

The method includes measuring distance measurements between the non-contact measuring device 32 and a surface of the part 12, e.g., the clutch hub, at discrete points along splines 66, 68 and slopes 70 between the splines 66, 68 as the part 12, e.g., the clutch hub, is rotated about the central axis A, as shown at block 104 of FIG. 10. The distance measurements may be measured at evenly spaced intervals of rotation of the part 12, e.g., the clutch hub, such as at every 0.1 degree of rotation as set forth above. Specifically, the method may include opening the non-contact measuring device 32 based on the signals received by the processor 38 from the stage 14. In particular, the method may include instructing the controller 23 with the processor 38 to instruct the non-contact measuring device 32 to read a measurement in response to every signal received by the processor 38 from the stage 14.

The part 12, e.g., the clutch hub, may be rotated 360 degrees and the distance measurements are the distance measurements during 360 degrees of rotation of the part 12 about the central axis A, as shown graphically in FIG. 7. In other words, distance measurements at discrete points along an entire periphery of the part may be measured. Alternatively, distance measurements may be taken along only a predetermined portion of the part 12.

The part 12, e.g., the clutch hub, may be continuously rotated during measurement of the distance measurements. In other words, the part 12 may be rotated at a constant rotational speed and the distance measurements may be measured as the part 12 rotates. Alternatively, the rotation of the part 12 may be slowed or stopped for each distance measurement.

The method includes communicating each measurement reading from the non-contact measuring device 32 to the filtering software programmed to the computer 18. Typically, the non-contact measuring device 32 saves each distance measurement during the reading and communicates all data points together to the filtering software. Alternatively, the non-contact measuring device 32 may communicate individual distance measurements to the filtering software one data point at a time. The method includes displaying the distance measurements on the graphical user interface 44.

With continued reference to FIGS. 10-14, the method includes filtering the distance measurements with the filtering software. In particular, the filtering software applies an algorithm to distance measurements to filter unnecessary measurements and spline measurements. The method includes removing distance measurements associated with the slopes 70, designed ridges 72, and holes 84, along with abnormal readings that exceed a calculated reference distance with the filtering software. For example, the filtering software analyzes consecutive distance measurements in series and compares that series to distance measurements before and after the series to identify extreme outliers, i.e., unnecessary measurements, that are not associated with the inner spline 66 or the outer spline 68. The filtering software eliminates these unnecessary measurements.

Specifically, with reference to FIG. 10, the method includes identifying some of the distance measurements as spline measurements associated with splines 66, 68, as shown in block 106 of FIG. 10, and identifying some of the distance measurements as unnecessary measurements. As one example, after identifying some of the measurements as spline measurements, the method may identify the distance measurements other than the spline measurements as unnecessary measurements. The calculation of the roundness of the clutch hub is based on the spline measurements.

With reference to FIG. 11, the step of identifying some distance measurements as spline measurements, as shown in block 106 of FIG. 10, may include comparing the difference between consecutive distance measurements with a threshold range, as shown in block 108. The method includes categorizing consecutive distance measurements having a difference outside of threshold range as unnecessary measurements and categorizing consecutive distance measurements within the threshold range as spline measurements, as shown in block 110 of FIG. 11.

The threshold range may be ±4 microns, i.e., ±0.004 mm. In such a configuration, the method includes comparing consecutive distance measurements and, if the second distance measurement is more than 0.004 mm greater than or less than the first distance measurement, then the two consecutive distance measurements are identified as unnecessary measurements. If the second distance measurement is within 0.004 mm of the first distance measurement, then the first of the two consecutive distance measurements is identified as a spline measurement. The threshold range may be any suitable magnitude.

The steps of comparing the difference and categorizing, as shown in blocks 108 and 110, respectively, of FIG. 11, may be further defined with the steps of FIG. 12, which may be performed by application of the algorithm to the distance measurements by the filtering software or on the computer 18. The method may include assembling a list of the distance measurements, as shown in block 112 of FIG. 12. The first two consecutive distance measurements of the list are first considered as a data subset, as shown in block 114 of FIG. 12. The difference between the two distance measurements of the data subset is determined, as shown in block 116 of FIG. 12.

With continued reference to FIG. 12, the difference between the distance measurements is compared to the threshold range, as shown in block 108. As shown in decision block 118, the method includes determining whether the difference is within the threshold range. If the difference is within the threshold range, the first distance measurement of the two consecutive distance measurements is identified as a spline measurement and, as shown in block 120, the data subset is redefined as the last distance measurement of the previous data subset and the next consecutive distance measurement of the list. As shown in FIG. 12, the steps shown in blocks 116, 108, and 118 are performed on the new data subset.

With continued reference to FIG. 12, as shown in block 122, if the difference is not within the threshold range, both distance measurements of the data subset may be eliminated.
Next, as shown in block 124, the data subset is redefined as the next two consecutive distance measurements on the list. As shown in FIG. 12, the steps shown in blocks 116, 108, and 118 are performed on the new data subset.

As set forth above, the method may eliminate the unnecessary measurements from the spline measurements, as shown in block 122 of FIGS. 11 and 12. For example, the algorithm of the filtering software may delete the unnecessary measurements, leaving only the spline measurements. Alternatively, the algorithm of the filtering software may ignore the unnecessary measurements, i.e., without deleting the unnecessary measurements. As set forth above, a graphical representation of the spline measurements without the unnecessary measurements is shown in FIG. 8.

As set forth above and as shown in block 128 of FIG. 11, the method includes calculating the roundness of the part 12, e.g., the clutch hub, based on the spline measurements. For example, as set forth above, the dimensional software analyzes the roundness of the part 12, e.g., the clutch hub, based on the spline data.

As set forth above, the part 12 includes an inner spline 66 and an outer spline 68. The method may determine the roundness of the inner splines 66 and/or the outer splines 68 without data interference from unnecessary measurements, such as those associated with slopes 70 between the inner splines 66 and the outer splines 68, designed ridges 72, and/or holes 86. Specifically, the method may include classifying the distance measurements as outer spline measurements and inner spline measurements and calculating at least one of an outer roundness of the part 12 based on the outer spline measurements and an inner roundness of the part 12 based on the inner spline measurements. For example, the outer spline measurements and the inner spline measurements may be classified before the spline measurements are provided to the dimensional software for calculation of the roundness.

With reference to block 128 of FIG. 11, the step of classifying the distance measurements as outer spline measurements and inner spline measurements includes calculating the average of the spline measurements. The method includes categorizing the spline measurements above the average as outer spline measurements and categorizing the spline measurements below the average as inner spline measurements, as shown in block 130 of FIG. 11. Based on the outer spline measurements and the inner spline measurements categorized in block 130, the method includes calculating at least one of the outer roundness of the part 12 and the inner roundness of the part 12, respectively, as shown in block 132.

The inner spline measurements may be stored in one data array along with their position in terms of degrees and outer spline measurements may be stored in a separate data array along with their position in terms of degrees. The method may include saving the data arrays in a file for exportation to the dimensional software. For example, the data arrays may be saved in a .csv file format or .sog file format.

The method may include exporting the file including the two data arrays to the dimensional software. The method may include calculating and analyzing dimensions of the measured part 12 with the dimensional software based on the two data arrays. As set forth above, the dimension analyzed by the dimensional software may be roundness, flatness, curve, RMS roundness, sector roundness, concentricity, eccentricity, eccentric angle, centre X, centre Y, average diameter, least square circle, maximum diameter, minimum diameter, minimum inscribed, and/or maximum circumscribed, etc.

With reference to FIG. 13, the method may eliminate distance measurements associated with the designed ridges 72. For example, in the embodiment shown in FIGS. 2 and 9, the designed ridges 72 are formed in the outer spline 68. The method may include separating the spline measurements, e.g., the outer spline measurements in the embodiment shown in the Figures, into discrete data sets each associated with one of the splines, as shown in block 134 of FIG. 12. Two such data sets are shown graphically in FIG. 9. The method may include determining an average of the distance measurements for each discrete data set, as shown in block 136. The average, for example, is graphically depicted in FIG. 9 and identified with element number 138. For each discrete data set, the method includes deleting distance measurements below the average of that discrete data set to delete the distance measurements associated with the designed ridges 72, as shown in block 140 of FIG. 13. The remaining spline measurements are then used to calculate the roundness of the part 12, as shown in block 142 of FIG. 13.

As set forth above, as shown in FIG. 6, the method includes displaying the calculated dimensions on the display area 62 and the results area of the graphical user interface 44. The method includes displaying identification that the measured part 12 is within the predetermined tolerance or outside of the predetermined tolerance. For example, the method includes displaying a graph depicting the roundness of the part 12 and color coding sections of the graph as acceptable/unacceptable.

The disclosure has been described in an illustrative manner, and it is to be understood that the terminology which has been used is intended to be in the nature of words of description rather than of limitation. Many modifications and variations of the present disclosure are possible in light of the above teachings, and the disclosure may be practiced otherwise than as specifically described.

What is claimed is:

1. A method of verifying the roundness of a clutch hub, the method comprising:
   - selecting the clutch hub after the clutch hub is manufactured on a manufacturing line;
   - placing the clutch hub adjacent a non-contact measuring device;
   - rotating one of the clutch hub and non-contact measuring device;
   - measuring distance measurements between the non-contact measuring device and a surface of the clutch hub at discrete points along splines and slopes between the splines of the clutch hub as one of the clutch hub and non-contact measuring device is rotated;
   - comparing a difference between consecutive distance measurements with a threshold range and categorizing consecutive distance measurements having a difference outside of threshold range as unnecessary measurements;
   - identifying some of the distance measurements as spline measurements associated with splines of the clutch hub;
   - calculating roundness of the clutch hub based on the spline measurements;
   - comparing the roundness of the clutch hub to a predetermined dimensional tolerance;
   - determining that the roundness is outside the predetermined dimensional tolerance; and
   - as a result of determining that the roundness is outside the predetermined dimensional tolerance, scrapping the clutch hubs manufactured during the time between

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selecting the clutch hub from the manufacturing line and determining that the roundness is outside the predetermined dimensional tolerance.

2. The method as set forth in claim 1 further comprising identifying the distance measurements other than the spline measurements as unnecessary measurements.

3. The method as set forth in claim 2 further comprising eliminating the unnecessary measurements from the spline measurements.

4. The method as set forth in claim 1 further comprising eliminating the unnecessary measurements from the spline measurements.

5. The method as set forth in claim 1 further comprising calculating the average of the spline measurements and categorizing the spline measurements above the average as outer spline measurements and categorizing the spline measurements below the average as inner spline measurements.

6. The method as set forth in claim 5 wherein calculating roundness of the clutch hub includes calculating at least one of an outer roundness of the clutch hub based on the outer spline measurements and an inner roundness of the clutch hub based on the inner spline measurements.

7. The method as set forth in claim 1 further comprising separating the spline measurements into discrete data sets each associated with one of the splines, determining an average of the distance measurements for each discrete data set, and, for each discrete data set, deleting distance measurements below the average of that discrete data set.

8. The method as set forth in claim 1 further including classifying the distance measurements as outer spline measurements and inner spline measurements and wherein calculating roundness of the clutch hub includes calculating at least one of an outer roundness of the clutch hub based on the outer spline measurements and an inner roundness of the clutch hub based on the inner spline measurements.

9. The method as set forth in claim 1 wherein the distance measurements are measured at evenly spaced intervals of rotation of the clutch hub.

10. The method as set forth in claim 1 wherein rotating the clutch hub includes rotating the clutch hub 360 degrees.

11. The method as set forth in claim 1 wherein the clutch hub is continuously rotated during measurement of the distance measurements.

12. A system comprising:
    a gage including a stage for supporting the clutch hub;
    the gage including a non-contact measuring device configured to measure distance measurements between the non-contact measuring device and the clutch hub, one of the stage and non-contact measuring device being configured to provide relative rotation between the clutch hub and the non-contact measuring device for measuring distance measurements about the clutch hub; and
    the gage including a computer configured to identify some of the distance measurements as spline measurements associated with the splines of the clutch hub;
    the computer being configured to compare a difference between consecutive distance measurements with a threshold range and categorizing consecutive distance measurements having a difference outside of threshold range as unnecessary measurements;
    the computer being configured to calculate roundness of the clutch hub based on the spline measurements;
    the computer being configured to compare the roundness of the clutch hub to a predetermined dimensional tolerance;
    the computer being configured to determine that the roundness is outside the predetermined dimensional tolerance;
    the computer being configured to display that the clutch hub is outside of the predetermined dimensional tolerance;
    and
    a manufacturing line from which, as a result of determining that the roundness is outside the predetermined dimensional tolerance, clutch hubs manufactured during the time between a selection of the clutch hub from the manufacturing line and determining that the roundness is outside the predetermined dimensional tolerance are scrapped.

13. The gage as set forth in claim 12 wherein the computer is configured to eliminate the unnecessary measurements from the spline measurements.

14. The gage as set forth in claim 13 wherein the computer is configured to eliminate the unnecessary measurements from the spline measurements.

15. A system comprising:
    a gage including a stage for supporting the clutch hub;
    the gage including a non-contact measuring device configured to measure distance measurements between the non-contact measuring device and the clutch hub, one of the stage and non-contact measuring device being configured to provide relative rotation between the clutch hub and the non-contact measuring device for measuring distance measurements about the clutch hub; and
    the gage including means for comparing a difference between consecutive distance measurements with a threshold range and categorizing consecutive distance measurements having a difference outside of threshold range as unnecessary measurements;
    the gage including means for comparing the roundness of the clutch hub to a predetermined dimensional tolerance;
    the gage including means for determining that the roundness is outside the predetermined dimensional tolerance; and
    a manufacturing line from which, as a result of determining that the roundness is outside the predetermined dimensional tolerance, clutch hubs manufactured during the time between a selection of the clutch hub from the manufacturing line and determining that the roundness is outside the predetermined dimensional tolerance are scrapped.

16. The gage as set forth in claim 15 further comprising means for eliminating the unnecessary measurements.

* * * *
Appendix B

List of other Published Journal and Conference Papers during my PhD

<table>
<thead>
<tr>
<th>Title of the Publication</th>
<th>Publication Type</th>
</tr>
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</table>
Vita Auctoris

NAME: Esrafil Jedari
PLACE OF BIRTH: Tabriz, Iran
YEAR OF BIRTH: 1974
EDUCATION:

Ph.D in Electrical and Computer Engineering
University of Windsor, Windsor, ON, Canada, 2018

M.Sc in Electrical Engineering (Telecommunications)
Tarbiat Modares University, Tehran, Iran, 2001

B.Sc. in Electrical Engineering
University of Tabriz, Tabriz, Iran, 1998
Esrafil Jedari

University of Windsor
Software/Hardware Solution Developer
Department of Electrical and Computer Engineering
CEI Building, 401 Sunset Ave. Windsor, Ontario Canada N9B 3P4
Email: jedaris@uwindsor.ca

Working Experiences

University of Windsor/LandauGage
(09/2010 – 10/2018)

- Design, simulate, fabricated and test various Analog, mixed-signal, and RF Integrated Circuits, including Delay Locked Loop based Time to Digital Converter at CMOS 65 nm and 180 nm CMOS technology using Cadence, Agilent ADS.
- Design and implement a non-contact coordinate measuring system to characterize transmission parts by developing metrology algorithms using Visual C#, Matlab, machine vision techniques.
- Developed WiFi based Indoor location positioning system, used Weka, Matlab, SQL, C#, Machine Learning techniques i.e. classification, feature selection, rule extraction, and clustering.
- Research Associate on contactless heart monitoring system for vehicle seats. Developed a circuit to monitor heart beats of driver. ADS Simulations has been performed on designed circuit.
- Research Associate on Micro Electromechanical Systems (MEMS) to investigate and design automotive Radar.
- Implemented a propagation channel model for vehicle to vehicle (V2V) communication systems based on DSRC.

Iran Telecommunication Research Center
(03/1999 – 09/2010)

- Faculty member and senior research project team leader at communications technology institute
- Designed, implemented Antenna Time Domain Measurement Laboratory, used instruments from Rohde & Schwarz, Tektronix, such as Network Analyzers, Mixed Signal Oscilloscopes, Tektronix CSA 8000 series, pulse generator
- Designed, fabricated and test wideband antenna for time-domain measurements
- Developed and implemented a Propagation Channel Model in CDMA technology for smart antennas applications (2001-2002).
- Performed adaptive antenna array signal processing & beamforming algorithms in WLAN and CDMA communication systems.

Duties:
- Worked with Business/Technology Owners to ensure that the deliverables achieve the business result that enables value creation;
- Developed integrated baseline project plans applying estimated models; documents estimating assumptions, refines plans and manages performance against them.
- Determined quality standards and oversees the execution / production of management documents.
- Identified and managed project costs and budgets.
- Raised and tracked issues and conflicts, removes barriers, resolved project issues and escalated to immediate manager when required.
- Facilitated schedule and cost forecasting; mentored project managers/team members in determining risk based provisions.
- Managed project communications including status reports to executives, stakeholders, business units, vendors, project team, etc.
### Education

**Ph.D.**
University of Windsor  
(Fall, 2018)
Electrical and Computer Engineering

**M.Sc.**
Tarbiat Modares University, Tehran, Iran.  
(2001)
Electrical engineering (Tele-communications Engineering)  
Thesis: Propagation Problems between LEO Satellites and Earth Stations in Urban Areas

**B.Sc.**
University of Tabriz, Tabriz, Iran.  
(1997)
Electrical Engineering  
Thesis: Voice Command Recognition using Fuzzy Logic

### Summary of skills

- Professional in Advanced Design System (ADS) and Cadence to design and analysis wireless communication systems and analog integrated circuits. WirelessInsite for Remcom to analysis wireless propagation channels. EMPro, HFSS to design and study electromagnetic structures, Cadence to design analog and digital circuits.
- Programming languages/Tools: Microsoft office (Word, Powerpoint, Excel,…), C++; C; C#.NET; SQL; Visual Studio; MySql; ADS; Cadence; EMPro; Wireless InSite; HFSS; Matlab; Weka
- Solid understanding to scope hardware for the implementation of signal processing algorithms
- Ability to coordinate and manage group of junior engineers to meet project deadlines
- Superior coding, presentation and communication skills
- Excellent organizational and analytical skills
- Expert in digital, analog and embedded system circuit design and analysis
- Lead cross-functional project teams to develop or improve new or current products.
- Generate & support new project/grant approval details, budget and time line.
- Participate and initiate the innovation of new concepts, designs, and novel new projects, including the use of new and improved processes and new technologies.
- Assist and participate in visitor presentations including entertainment. Prepare materials when necessary.
- Languages: Fluent in English, Persian and Turkish, familiar with French and Arabic

### Honors

- Recipient the Canadian "Exemplary Small Section Award" for excellent leadership, management and administration for 2017.
- Executive director of selected Canada wide OCE project, OCE annual General Meeting, 2017.
- Recipient Fredrick Atkins Graduate Award, 2017.
- Recipient Graduate Student Scholarship, 2015-2016.
- Iran Telecommunication Company researcher award (2006).
- Full Scholarship for Master of Science in Electrical Engineering from Iran Telecom. Research Center 1999-2000.
**Leadership & professional Activities**

- Vice-Chair, IEEE Windsor Section, Since Jan. 2017.
- Secretary, IEEE Windsor Section, since Nov. 22, 2014.
- Organizer of three hands on workshop for ECE students at UWindsor sponsered by National Instruments and Rohde and Shwartz Inc.
- Cofounder of 5 chapters/affinity groups at UWindsor:
  • IEEE student branch, Joint chapter of Communications and Signal Processing societies, Joint chapter of Circuit and Systems & Computer societies, WIE affinity group, and Young professional affinity group – 2015
- Funder of Student Branch of IEEE at Tarbiat Modares University, 2009.
- Journal Papers Reviewer
  • IEEE Transactions on Vehicular Technology, 2015-2016
  • IEEE Transactions on Circuits and Systems II, 2016
- Reviewer of papers at the following conferences:
- Student Representative in the ECE department council, Electrical and Computer Engineering Department, University of Windsor, 2015.
- Director of appointments at the IEEE SEM Section Nominations Committee- 2013
- Academic Mentor of the IEEE student branch at the UWindsor- Since May 2013
- IEEE active Member since 2006

**Creative activities**

- Founder of a Telegram group in social media to help persian new commers to Windsor (2016), serving more than 400 members Sept. 2018.
- Judge at Western Regional Science, Technology and Engineering Fair, 2015
- Organizer of social events for Persian residents/student in Windsor, Canada, 2010-2016.
- Giles campus french immersion public school parents board member, 2014
- Founder and admin of askinabroad.com to help newcomers to Canada, Since 2012.
- Designed a forum using Mybb forum platform to help newcomers to settle down in Canada
- Prepare and publish a booklet containing necessary information to settle down in Canada for newcomes and students, summer 2011, and 2013.
- Volunteer in YMCA to help new commers to Canada, since 2013.
- Organizer of technical and general seminars/workshops at UWindsor since 2013.
- Expert on knotting hand Persian Tableau rug, knotted 2 Persian Tableau rug, 1991
- Photographer since 2010

**Publications**

1 US patent, 2 books and more than 35 journal and conference papers. (please see the following pages for detailed list)
Teaching Experiences

- Summer 2017, Graduate/Teaching assistance, *Energy Storage systems for HEV-EV Applications*, Dr. Nazri, University of Windsor
- Fall 2016, Graduate/Teaching assistance, *Circuit analysis (Undergraduate Course)*, Dr. Abdel-Raheem, University of Windsor
- Winter 2016, Graduate/Teaching assistance, *Treatment of Experimental Data (Undergraduate Course)*, Dr. Zhang, University of Windsor
- Fall 2015, Graduate/Teaching assistance, *Special Topics ; Advanced Energy Storage System for Hybrid electrical Vehicles*, Dr. Nazri, University of Windsor
- Winter 2015, Graduate/Teaching assistance, *Signals and systems (Undergraduate Course)*, Dr. Shahrrava, University of Windsor
- Summer 2015, Graduate/Teaching assistance, *Electromagnetic Waves & Radiating Systems II*, Dr. Muscedere, University of Windsor
- Fall 2014, Graduate/Teaching assistance, *Special Topics ; Advanced Energy Storage System for Hybrid electrical Vehicles*, Dr. Nazri, University of Windsor
- Winter 2014, Graduate/Teaching assistance, *Analog Integrated Circuit Design*, Dr. Muscedere, University of Windsor
- Summer 2013, Graduate/Teaching assistance, *Electromagnetic Waves & Radiating Systems II*, Dr. Rashidzadeh, University of Windsor
- Fall 2008 – Fall 2010, Teaching Assistant (TA) of Dr. G. Dadashzadeh for “Engineering Mathematics,” as MS course, Department of Eng., Shahed University, Tehran, Iran.
- Fall 2009, Teaching Assistant (TA) of Prof. Hakkak for “Satellite communications,” as MS course, Department of Engineering, Tarbiat Modares University, Tehran, Iran.
- Fall 2008-Fall 2009, Lecturer for “Computer Networks, CCNA,” as BS course, Department of Engineering, Sadra Institute of Higher Education, Tehran, Iran.
- Fall 1996 to summer 1998- Lecturer for “Computer Programming Languages/OS, BASIC, Fortran, PASCAL, MS- DOS”, “Computer Basics” Azad University, Tabriz, Iran.
# Esrafil Jedari
**List of Publications and Scholarly Activities**

## Publications

### Patents

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### Book(s)

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### Journal Papers

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Conference Papers


**Supervised University Thesis**


**Presented workshops**

[1] E. Jedari, "Introduction to Matlab", Workshop at University of Windsor, Sep. 2015,
