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Design of a wideband low-power continuous-time sigma-delta (ΣΔ) analog-to-digital converter (ADC) in 90nm CMOS technology

Fang Chen
University of Windsor

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Design of a Wideband Low-Power Continuous-Time Sigma-Delta ($\Sigma\Delta$) Analog-to-Digital Converter (ADC) in 90nm CMOS Technology

by

Fang Chen

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Design of a Wideband Low-Power Continuous-Time Sigma-Delta ($\Sigma\Delta$) Analog-to-Digital Converter (ADC) in 90nm CMOS Technology

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Abstract

The growing trend in VLSI systems is to shift more signal processing functionality from analog to digital domain to reduce manufacturing cost and improve reliability. It has resulted in the demand for wideband high-resolution analog-to-digital converters (ADCs). There are many different techniques for doing analog-to-digital conversions. Oversampling ADC based on sigma-delta ($\Sigma\Delta$) modulation is receiving a lot of attention due to its significantly relaxed matching requirements on analog components. Moreover, it does not need a steep roll-off anti-aliasing filter. A $\Sigma\Delta$ ADC can be implemented either as a discrete time system or a continuous time one. Nowadays growing interest is focused on the continuous-time $\Sigma\Delta$ ADC for its use in the wideband and low-power applications, such as medical imaging, portable ultrasound systems, wireless receivers, and test equipments. A continuous-time $\Sigma\Delta$ ADC offers some important advantages over its discrete-time counterpart, including higher sampling frequency, intrinsic anti-alias filtering, much relaxed sampling network requirements, and low-voltage implementation. Especially it has the potential in achieving low power consumption.

This dissertation presents a novel fifth-order continuous-time $\Sigma\Delta$ ADC which is implemented in a 90nm CMOS technology with single 1.0-V power supply. To speed up design process, an improved direct design method is proposed and used to design the loop filter transfer function. To maximize the in-band gain provided by the loop filter, thus maximizing in-band noise suppression, the excess loop delay must be kept minimum. In this

design, a very low latency 4-bit flash quantizer with digital-to-analog (DAC) trimming is utilized. DAC trimming technique is used to correct the quantizer offset error, which allows minimum-sized transistors to be used for fast and low-power operation. The modulator has sampling clock of 800MHz. It achieves a dynamic range (DR) of 75dB and a signal-to-noise-and-distortion ratio (SNDR) of 70dB over 25MHz input signal bandwidth with 16.4mW power dissipation. Our work is among the most improved published to date. It uses the lowest supply voltage and has the highest input signal bandwidth while dissipating the lowest power among the bandwidths exceeding 15MHz.

Acknowledgments

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I am deeply grateful to my husband, Till Kuendiger, for his endless support and encouragement through the most difficult time during my graduate program. I would like to thank my parents, Yanfen Fang and Huidao Chen, for believing me every time I said I was graduating "next year". I would also like to thank my sister, Yue Chen, and my brother, Dong Chen, for always being there for me.

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List of Symbols and Abbreviations

Δt ..... Time perturbation in sampling instant

Δ ..... The quantization step

$\overline{v^2}$ ..... Averaging noise power per unit bandwidth (V^2/Hz)

Ψ ..... The in-band gain function of the loop filter $G(s)$

$\Sigma\Delta\mathbf{M}$ ..... Sigma-delta modulator

σ_e ..... Standard deviation of error signal e

$E(s)$ ..... Noise signal in s-domain

$e[n]$ ..... Quantizer error sequence

f_b ..... Input signal bandwidth

f_s ..... System sampling frequency

$G(s)$ ..... The transfer function of a loop filter

$G_m - C$ ..... Transconductance-Capacitor

k ..... Boltzmann constant ($1.38 \times 10^{-23} J/K$)

$p(e)$ ..... Probability density function of signal e

P_{jitter} ..... Power of clock jitter

$S_x(f)$ ..... Power spectrum density function

T_s ..... System sampling clock rate

V_{REF} ..... Full-scale input signal range of a quantizer

$x(nT_s)$ ..... Sampled discrete-time signal

$X(s)$ ..... Input signal in s-domain

$x(t)$ ..... Analog input signal

$y(n)$ ..... Output digital signal

$Y(s)$ ..... Output signal in s-domain

ADC ..... Analog-to-digital converter

BC ..... Binary code

BW ..... Signal bandwidth

CMFB ..... Common-mode feedback

CMOS ..... Complementary metal-oxide-semiconductor

CQFP ..... Ceramic quad flat pack

CT ..... Continuous-time

DAC ..... Digital-to-analog converter

DC ..... Direct-current

DEM ..... Dynamic element matching

DR ..... Dynamic range

DT ..... Discrete-time

FFT ..... Fast Fourier transform

FOM ..... Figure of merit

GBW ..... Gain-bandwidth-product

HRZ ..... Half-delay-return-to-zero

MASH ..... Multi-stage noise shaping

MOSFET ..... Metal-oxide-semiconductor field-effect transistor

N ..... Resolution (number of bits) of a quantizer

NCF ..... Noise cancellation filter

NMOS ..... N-type MOSFET

NRZ ..... Non-return-to-zero

NTF ..... Noise transfer function

Op-amp ..... Operational Amplifier

OSR ..... Oversampling ratio

OTA ..... Operational transconductance amplifier

PDF ..... Probability density function

PMOS ..... P-type MOSFET

PSD ..... Power spectrum density

Q ..... The symbol of a quantizer

RC ..... Resistor-capacitor

RZ ..... Return-to-zero

SC ..... Switched-capacitor

SI ..... Switched-current

SNDR ..... Signal-to-noise-and-distortion ratio

SNR ..... Signal-to-noise ratio

STF ..... Signal transfer function

TC ..... Thermometer code

ZOH ..... Zero-order-hold

Chapter 1

Introduction

1.1 Motivation

Wideband low-power analog-to-digital converters (ADCs) find many useful applications such as medical imaging, portable ultrasound systems, wireless receivers, and test equipments. Using wideband ADC means more signal processing functionality can be shifted to digital domain achieving low-cost, high-yield, and higher re-configurable devices. Low power feature is crucial especially for portable devices since it not only improves battery life and reduces system weight but also keeps device temperature at reasonable level.

There is increasing interest in continuous-time (CT) sigma-delta ($\Sigma\Delta$) ADCs for wideband low-power applications [2, 3, 4]. CT $\Sigma\Delta$ ADCs offer some important advantages over their discrete-time (DT) counterparts. They may operate at higher frequencies as no settling behavior is involved in continuous-time filtering. They have much relaxed sampling network requirements since sampling error is suppressed by noise shaping and oversampling. All these enable CT $\Sigma\Delta$ modulators to increase signal bandwidth with low power consumption.

Recent research has pushed signal bandwidth of CT $\Sigma\Delta$ modulators to 20MHz bandwidth range with 9 to 13-bit resolution using CMOS technology. Caldwell *et al.* [5] designed

a time-interleaved $\Sigma\Delta$ modulator in 0.18μm CMOS. The modulator achieves 55.2dB dynamic range (DR) over 20MHz bandwidth with 103mW power consumption. Most recently, Mitteregger *et al.* [6] presented a $\Sigma\Delta$ modulator with 20mW power consumption in a 0.13μm CMOS technology. The modulator has 80dB DR and 74dB SNDR over 20MHz bandwidth. This research has targeted at 75dB DR (corresponding to 12-bit resolution) over 25MHz input signal bandwidth with under 20mW power consumption using continuous-time $\Sigma\Delta$ modulation techniques.

1.2 Research Goals

This dissertation seeks to address design issues of wideband low-power continuous-time $\Sigma\Delta$ modulators at system, architecture, and circuit level. The emphasis is on the implementation in low supply voltage technology such as nanometer CMOS . The obtained conclusions are used to implement a continuous-time $\Sigma\Delta$ modulator in 90nm CMOS with target specifications of 25MHz bandwidth, 12-bit resolution, and less than 20mW power consumption. Some key research results are summarized below:

- The design of continuous-time $\Sigma\Delta$ modulators has been explored with an emphasis on increasing bandwidth and reducing power consumption while maintaining their high resolution.
- An improved direct design method has been proposed, which allows the direct design of the loop filter transfer function. It speeds up the design process by eliminating discrete-time to continuous-time transformation and by analyzing stability directly in continuous-time domain.
- On-chip automatic RC tuning scheme has been employed and implemented to overcome large process variation and mismatch in CMOS technology.
- DAC trimming scheme has been implemented to minimize the DC offset in the internal quantizer caused by process mismatch.

- A fifth-order continuous-time $\Sigma\Delta$ modulator with 4-bit internal quantizer has been realized in a 90nm 7M2T CMOS technology, with chip area of $0.5 \times 0.5mm^2$.
- The results show that the modulator achieves 75dB dynamic range over 25MHz signal bandwidth, dissipating 16.4mW from 1.0-V power supply.
- This work has demonstrated the feasibility of implementing a wideband high-resolution continuous-time $\Sigma\Delta$ modulator in nanometer (90nm) CMOS technology with very low power consumption.

1.3 Organization of the Dissertation

This dissertation is focused on analysis, design, and implementation of wideband low-power continuous-time $\Sigma\Delta$ modulators. It is organized into six chapters, including this introduction. The remaining chapters are organized as following.

Chapter 2 briefly reviews some fundamental issues related to $\Sigma\Delta$ ADCs. Two main operations of an ADC including sampling and quantization are described and modelled. Operation principles of a $\Sigma\Delta$ ADC including oversampling and noise-shaping are examined. Design choices for a $\Sigma\Delta$ modulator are also discussed.

Chapter 3 is devoted to the system-level design of wideband low-power $\Sigma\Delta$ modulators. Survey on state-of-the-art wideband continuous-time $\Sigma\Delta$ modulators is given. An improved direct design method is proposed to speed up the iterative design process. Modulator architectures and loop filter topologies which are suitable for wideband low-power implementations are analyzed. A fifth-order experimental continuous-time $\Sigma\Delta$ modulator with 4-bit internal quantizer is then proposed.

Chapter 4 discusses the circuit design details of the proposed experimental modulator. Building blocks of the modulator include a fifth-order loop filter with automatic RC constant tuning, a 4-bit internal flash quantizer with DAC trimming, and two feedback current-steering DACs.

Chapter 5 presents the layout design, test setup, and a discussion of the performance in the context of the state-of-the-art wideband continuous-time $\Sigma\Delta$ modulators. A summary

of the results, conclusions, as well as suggestions for further research work are presented in Chapter 6.

Chapter 2

Continuous-Time ΣΔ Modulator Fundamentals

In this chapter we review some of the fundamental issues related to continuous-time (CT) ΣΔ modulators. The discussion begins with sampling and quantization, which are the two main operations of an analog-to-digital converter. Then, operating principles of ΣΔ modulators involving oversampling and noise-shaping techniques are discussed, followed by two examples illustrating how a modulator works. A variety of performance metrics used to evaluate a ΣΔ modulator are given. Design choices of CT ΣΔ modulators are then examined. Finally, the impacts of clock jitter on a CT modulator is analyzed.

2.1 Sampling and Quantization

Converting analog signals to digital signals is the function of an analog-to-digital converter (ADC). Analog signals are defined as the signals which are continuous in both time and amplitude. Digital signals refer to the signals which are discrete with respect to time and amplitude. Figure 2.1 shows the fundamental operations of an ADC. Analog input signal $x(t)$ first passes an anti-alias filter to remove any high frequency component in $x(t)$ which

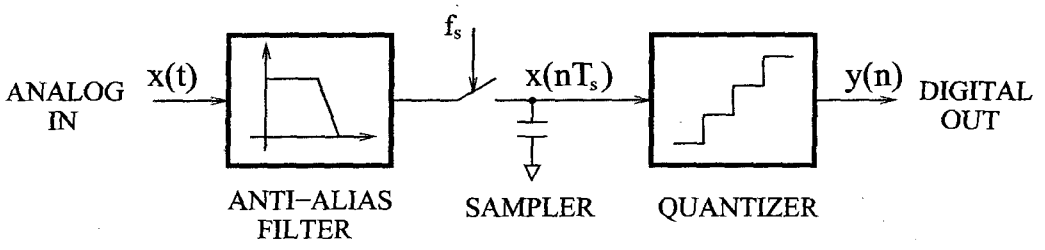


Figure 2.1: Basic operations of an ADC.

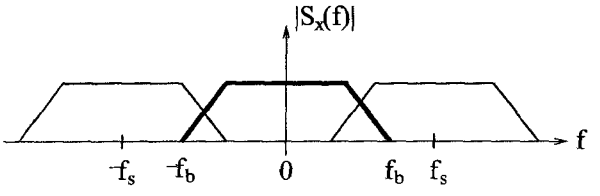


Figure 2.2: Aliasing caused by sampling.

might alias back to the signal band. The output of the filter is the band-limited analog signal, which is then sampled and yielding discrete-time signal $x(nT_s)$. $x(nT_s)$ is still continuous in amplitude. It is then quantized in amplitude by a quantizer before being encoded to the output digital signal $y(n)$. As can be seen, analog-to-digital conversion contains two main operations: sampling in time and quantization in amplitude.

2.1.1 Sampling

The operation of the analog signal $x(t)$ sampled at discrete time is called sampling, which is a memoryless linear operation. According to Nyquist sampling theorem [7], $x(t)$ must be sampled at a frequency twice higher than the $x(t)$ bandwidth f_b to avoid information loss. Otherwise, distortion caused by aliasing will occur as shown in Figure 2.2, whereas f_b is the bandwidth of analog signal $x(t)$ and f_s is the sampling frequency.

If the sampling frequency f_s is at or slightly higher than the Nyquist rate $2f_b$, the converter is called Nyquist-rate converter. f_s can be chosen much higher than the Nyquist rate the converter is said to be oversampling converter. And the oversampling ratio OSR

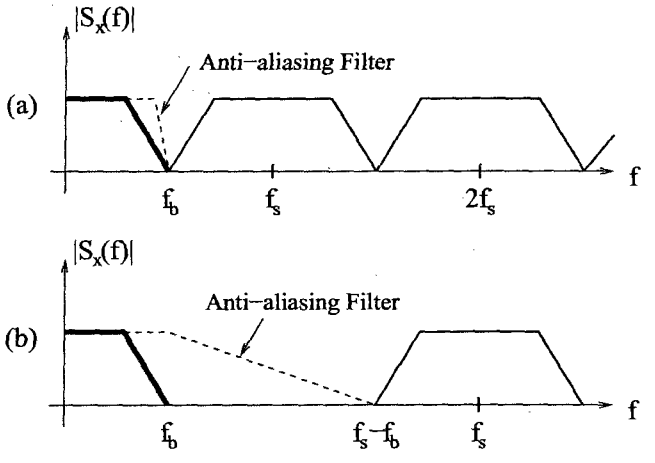


Figure 2.3: An analog signal is (a) sampled at Nyquist rate (b) oversampled.

is defined as $OSR = f_s/2f_b$. Two types of sampling, Nyquist sampling and oversampling, are depicted in Figure 2.3.

2.1.2 Quantization

Quantization of signals is inherently nonlinear operation. During the quantization, an amplitude continuous signal is mapped onto a set of discrete values by means of rounding or truncation. The operation is irreversible and causes information loss. For a quantizer with number of bits (binary-weighted) of N , there are total $2^N - 1$ quantization steps. Each quantization step Δ is determined by

$$\Delta = \frac{V_{REF}}{2^N - 1} \tag{2.1}$$

where N is the number of bits of the quantizer, and V_{REF} is the full-scale input range of the quantizer.

Figure 2.4 shows the quantization of a signal $x(t)$ at the amplitude level of x_i. The signal $x(t) = x_i - e$ is ideally quantized into level x_i as long as $-0.5\Delta < e \leq 0.5\Delta$. Signals that are larger than $x_i + 0.5\Delta$ are quantized into the next quantization level x_{i+1}. And signals that are smaller than $x_i - 0.5\Delta$ are mapped to the previous quantization level x_{i-1}. Therefore, quantization error never exceeds $\pm 0.5\Delta$.

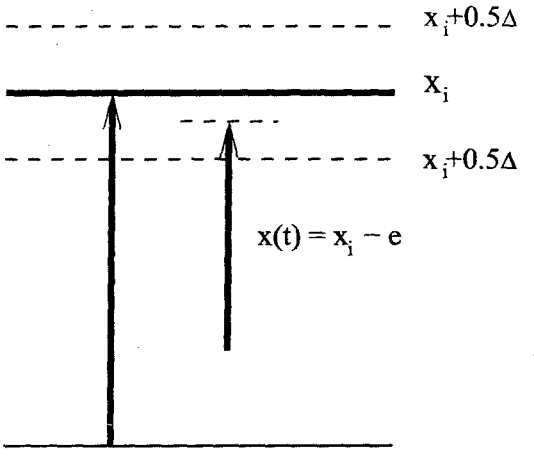


Figure 2.4: Quantization of a signal at level x_i.

An eight-level (the number of bits $N = 3$) quantizer in/out transfer characteristic is shown in Figure 2.5(a) and corresponding quantization error is shown in Figure 2.5(b).

To simplify the analysis, quantization error is commonly approximated as an independent additive white noise source. According to Bennett's theorem [8, 9], this approximation is valid if the following conditions are hold:

- The quantizer does not overload.
- The quantizer has a large number of quantization levels.
- The input signal is active over many quantization levels.
- The joint probability density function (PDF) of the input signal at different sample times is smooth.

Under these conditions, the quantization error sequence $e[n]$ is approximately uniformly distributed and has PDF of

$$p(e) = \begin{cases} \frac{1}{\Delta} & \text{if } e \in (-0.5\Delta, 0.5\Delta] \\ 0 & \text{otherwise} \end{cases} \tag{2.2}$$

as shown in Figure 2.6. As a result, the quantizer can be replaced by a linearized stochastic model as shown in Figure 2.7.

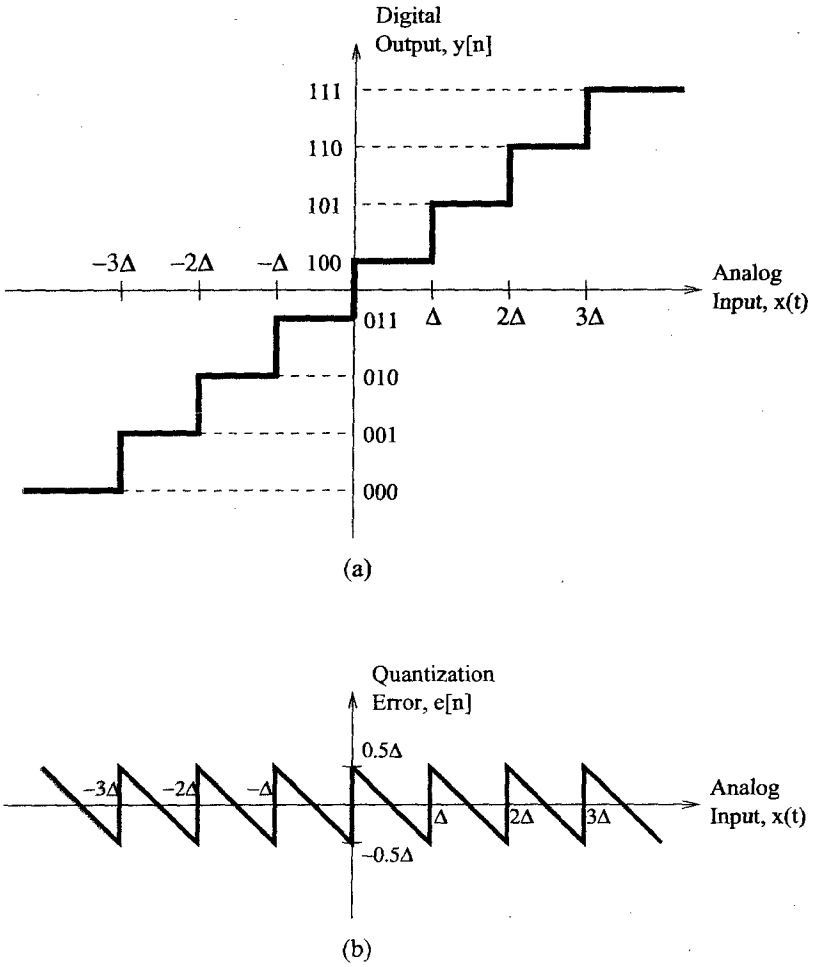


Figure 2.5: (a) Quantizer transfer characteristic (b) Quantization error.

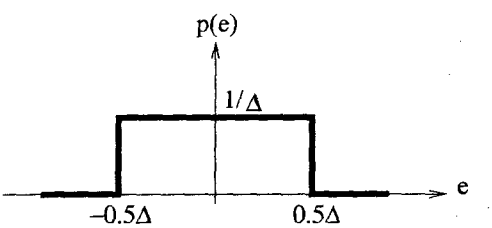


Figure 2.6: Probability density function (PDF) of uniformly distributed quantization error.

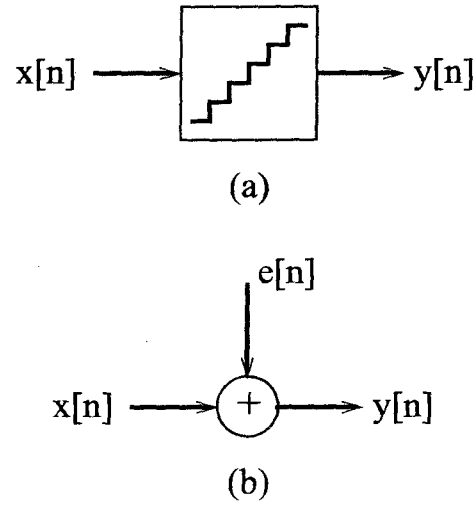


Figure 2.7: (a) Nonlinear model of a quantizer. (b) Linearized stochastic model of a quantizer.

The total power of the quantization error signal is equal to its variance and is calculated by [10]

$$\sigma_e^2 = \int_{-\infty}^{\infty} e^2 p(e) de = \frac{1}{\Delta} \int_{-\Delta/2}^{\Delta/2} e^2 de = \frac{\Delta^2}{12} \tag{2.3}$$

Limitations of this additive white noise model of a quantizer are depicted in details in [11].

2.2 Operating Principles of ΣΔ Modulators

Operations of ΣΔ modulators are based on two principles including oversampling and noise shaping. Oversampling is achieved by adopting much higher sampling frequency f_s than Nyquist rate $2f_b$. Noise shaping is achieved by embedding a quantizer in a feedback loop. Due to the feedback and oversampling, the quantization process of a ΣΔ converter differs fundamentally from that in a Nyquist-rate converter. A signal is no longer quantized to the full resolution of the converter. Each sample of the input signal does not correspond to only one output sample. Figure 2.8 shows a complete ΣΔ ADC, which has a loop filter with transfer function of G . The output of the loop filter is sampled and quantized by an

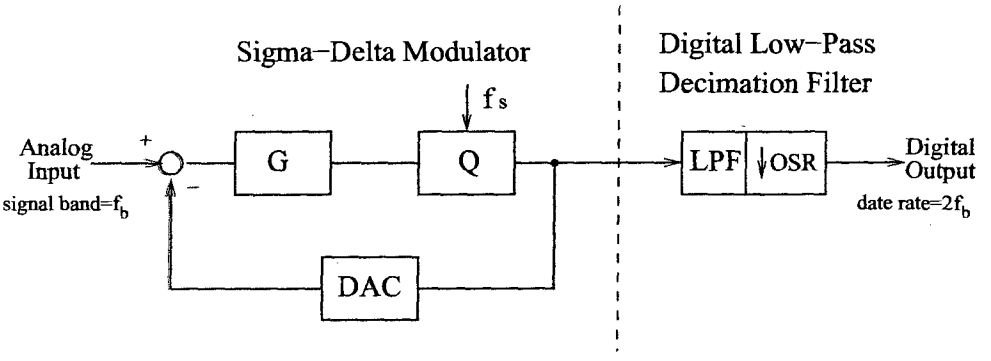


Figure 2.8: Complete ΣΔ ADC block diagram including decimation filter.

internal quantizer Q. The digital output of the quantizer Q is subtracted from the analog input via a digital-to-analog converter (DAC) in the feedback path. In the following digital decimation filter, many coarsely quantized samples from the output of the Q are processed to produce a more precise estimate of the analog input signal at a lower sampling rate. An example of digital low-pass decimation filter design can be found in Appendix A.

2.2.1 Oversampling

Quantization error is modeled as additive white noise. The total quantization noise power of $\Delta^2/12$ is uniformly distributed across the sampling bandwidth $(-f_s/2, f_s/2)$. By oversampling, even though the total quantization noise remains the same, the amount of noise that falls within the signal band is much lower. The power spectral density (PSD) of the quantization noise is calculated by

$$S_e(f) = \frac{\Delta^2/12}{f_s} \tag{2.4}$$

The total quantization noise power that falls into the signal bandwidth is:

$$\sigma_e^2 = \int_{-f_b}^{f_b} S_e(f)df == \frac{\Delta^2/12}{f_s} \cdot 2f_b = \frac{\Delta^2}{12} \cdot \frac{1}{OSR} \tag{2.5}$$

In Figure 2.9, shaded area is the total quantization noise power falls in the signal band. As can be seen, oversampling reduces in-band quantization noise by a factor of OSR.

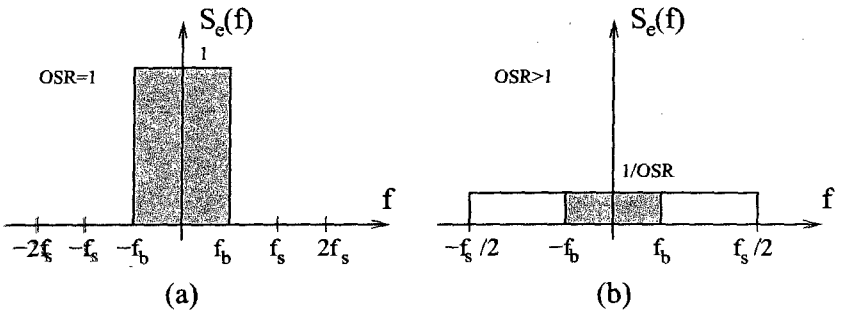


Figure 2.9: PSD of quantization noise for an ADC sampled at (a) $OSR = 1$. (b) $OSR > 1$.

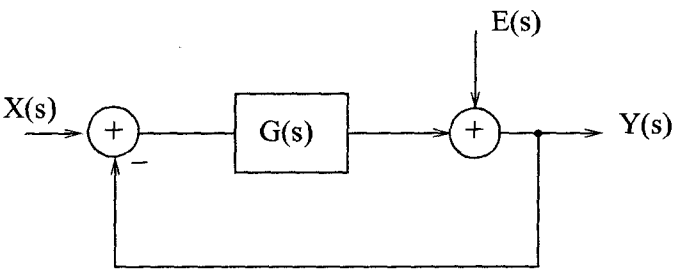


Figure 2.10: Simplified linear model of a continuous-time ΣΔ modulator.

2.2.2 Noise Shaping

Even though oversampling can reduce the in-band quantization noise, the reduction is not significant. ΣΔ ADC mainly uses noise shaping to reach large noise suppression by pushing noise out of signal band. For low frequencies, the DAC in the feedback path approximately has a gain of 1. Figure 2.10 shows a simplified linear model of a continuous-time ΣΔ modulator. The output of the modulator $Y(s)$ can be expressed as:

$$\begin{aligned} Y(s) &= \frac{G(s)}{1+G(s)} \cdot X(s) + \frac{1}{1+G(s)} \cdot E(s) \\ &= STF \cdot X(s) + NTF \cdot E(s) \end{aligned} \tag{2.6}$$

where $X(s)$ is the analog input, $E(s)$ is the noise added by quantizer, and $G(s)$ is the loop filter transfer function. Signal transfer function (STF) is defined as $STF(s) = Y(s)/X(s)$ and noise transfer function (NTF) is defined as $NTF(s) = Y(s)/E(s)$. If $G(s)$ has a

lowpass filter characteristic with high DC gain, then for low-frequencies, the STF is close to 1 and NTF is close to 0. It means the input signal will go through without attenuation, while the quantization noise is greatly attenuated. For frequencies close to half the sampling frequency, the input signal is filtered and the quantization noise becomes large.

2.3 Low-pass ΣΔ Modulator

It is possible to shape the noise away from any region of the sampling bandwidth, $-f_s/2$, $f_s/2$. Modulators with noise shaping in baseband (0, f_b) is called low-pass modulators. Modulators with noise shaping in other than baseband are called band-pass modulators. In the thesis, we focus on low-pass modulators. The s-domain representation of a first-order low-pass ΣΔ modulator is depicted in Figure 2.11. As can be seen, the loop filter is actually an integrator. By using additive white quantization noise model for $E(s)$ and simplified

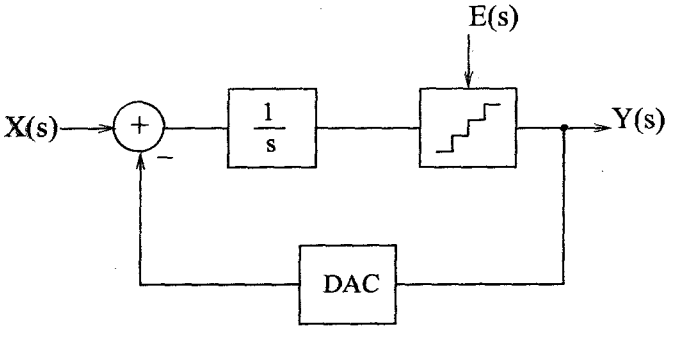


Figure 2.11: Example of a first-order ΣΔ modulator.

DAC model, the STF and NTF can be derived.

$$\begin{aligned} Y(s) &= STF \cdot X(s) + NTF \cdot E(s) \\ &= \frac{1}{1+s} \cdot X(s) + \frac{s}{1+s} \cdot E(s) \end{aligned} \tag{2.7}$$

The s-domain representation of a third-order low-pass ΣΔ modulator is shown in Figure 2.12. In s-domain the output of the modulator $Y(s)$ is

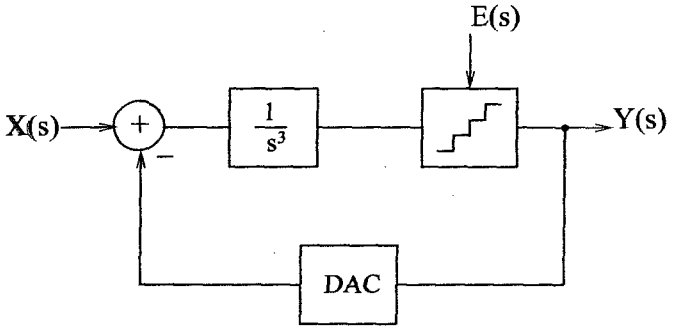


Figure 2.12: Example of a third-order ΣΔ modulator.

$$\begin{aligned} Y(s) &= STF \cdot X(s) + NTF \cdot E(s) \\ &= \frac{1}{1+s^3} \cdot X(s) + \frac{s^3}{1+s^3} \cdot E(s) \end{aligned} \tag{2.8}$$

The NTFs and STFs for the first-order and third-order ΣΔ modulators are plotted in Figure 2.13 and Figure 2.14, respectively. As can be seen in Figure 2.13, noise transfer functions (NTFs) exhibit high-pass transfer characteristics, pushing noise out of baseband. Moreover, the third-order shaping suppresses the quantization noise more effectively in the baseband than first-order shaping. In general, as the order of the noise shaping increases, the level of quantization noise present in the signal passband decreases. Although the quantization noise is suppressed more effectively through the use of higher-order modulators, the order of a modulator cannot be increased arbitrarily because it is difficult to guarantee the stability of third- and higher-order modulators. More details about stability of high-order modulator will be analyzed in later chapters. Signal transfer functions (STFs) in Figure 2.14 show low-pass transfer characteristics.

2.4 Performance Metrics

ΣΔ modulators are characterized in a number of different ways to indicate the performance capability. Some of the most important characteristics are introduced below.

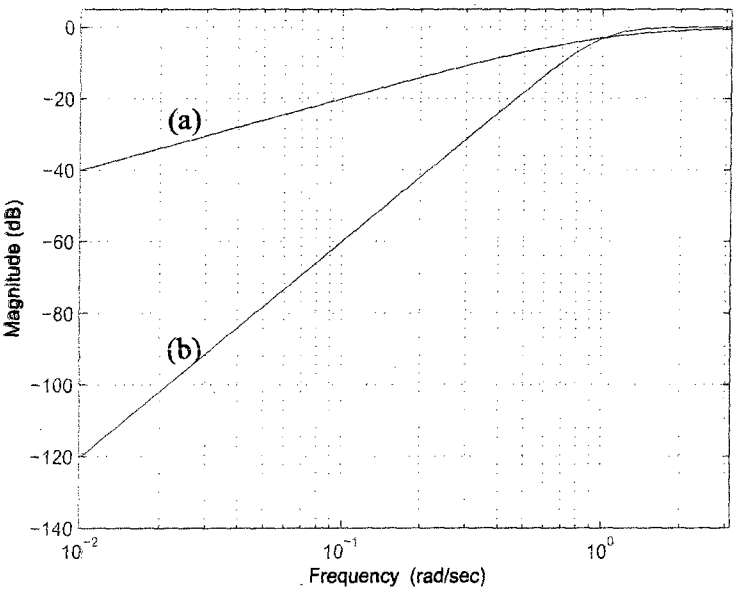


Figure 2.13: NTFs of (a) first-order (b) third-order ΣΔ modulator.

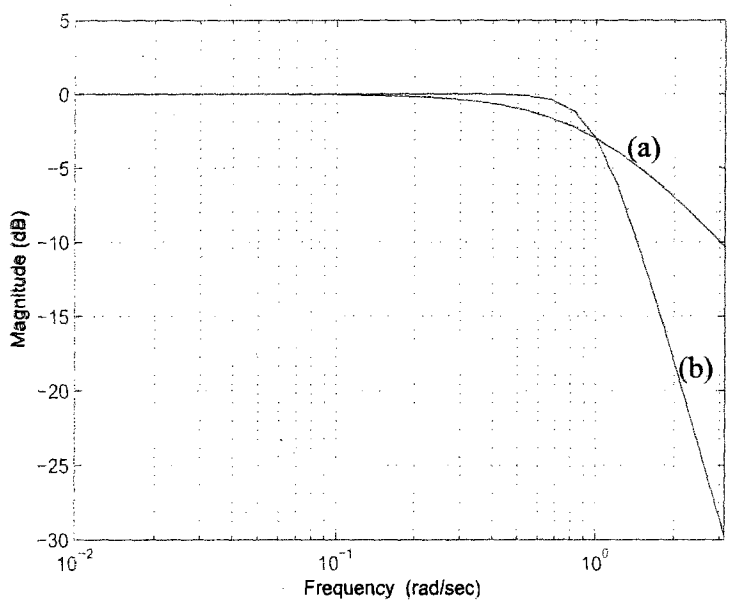


Figure 2.14: STFs of (a) first-order (b) third-order ΣΔ modulator.

2.4.1 SNR/SNDR and Dynamic Range (DR)

The signal-to-noise ratio (SNR) is defined as the ratio of signal power to in-band noise power, including quantization noise and circuit noise. The signal-to-noise-and-distortion ratio (SNDR) measures the degradation due to the combined effect of noise and harmonic distortion within a specified bandwidth. Another useful performance benchmark is dynamic range (DR). It is the ratio in power between the maximum input signal level and the minimum detectable input signal level. Figure 2.15 shows how to determine peak SNDR and DR from a plot of SNDR versus input power level.

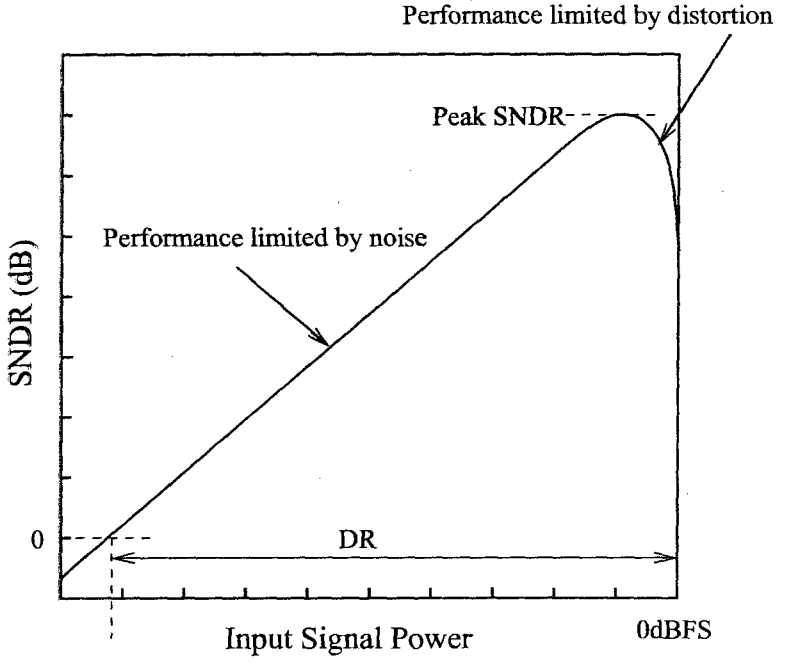


Figure 2.15: SNDR versus input signal power level for a modulator.

Dynamic range (DR specified in dB) is equivalent to the resolution of the modulator as an ADC. It can be converted to the resolution in bits by relating a ΣΔ modulator to a Nyquist-rate converter using:

$$N = \frac{DR - 1.76}{6.02} \tag{2.9}$$

where N is the resolution in number of bits.

To obtain SNR, SNDR, and DR, power spectrum estimation of the modulator output is required. In this thesis, periodogram method based on Fast Fourier Transform (FFT) is used to find power spectra at the output of the modulator. Appendix B shows the details of the method.

2.4.2 Input Signal Swing and Bandwidth

Input signal swing is the allowable input signal range. It indicates the maximum and minimum values that the input signal may have without driving the modulator out of range or resulting in an unacceptable distortion. Input bandwidth is the maximum input signal frequency at which the modulator remains the same resolution and signal swing. It is used to evaluate the speed of the modulator.

2.4.3 Power Dissipation

Power dissipation becomes an important performance metric because many ΣΔ ADCs are being implemented in battery powered portable devices. Reduced power dissipation means lower system weight and improved battery life. Minimizing power consumption can also make it easier to keep the temperature of the devices at a reasonable level.

2.4.4 Figure of Merit (FOM)

To compare the overall performance of different types of ADCs, figure-of-merit (FOM) is introduced and is defined as [12, 13, 14]:

$$FOM = \frac{P}{2^N \cdot 2f_b} \tag{2.10}$$

It takes the relation of overall power dissipation (P) over modulator resolution (N) and input signal bandwidth (f_b). Smaller the FOM value is, better the overall performance of the modulator is.

2.5 Design Choices of a Low-Pass ΣΔ Modulator

2.5.1 Modulator Order

The order of a ΣΔ modulator is determined by the order of its loop filter $G(s)$, which is the maximum power of s in the $G(s)$ denominator. In this work we define any order higher than two as high-order. First and second-order modulators are considered as low-order modulators. A high-order modulator provides higher in-band gain than a low-order modulator. Therefore, for a fixed signal bandwidth f_b, better noise suppression and higher resolution can be achieved through adopting high-order loop filter. The main drawback of a high-order modulator is that stability of the system becomes conditional [15]. This is because of the high gain of NTF at high frequencies. It causes the quantizer and internal nodes overload. Maximum input range must be restricted to ensure stability.

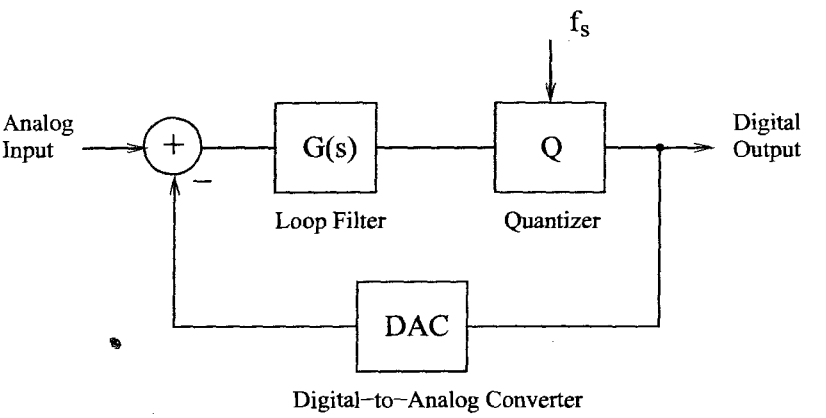


Figure 2.16: General system diagram of a ΣΔ modulator.

2.5.2 Oversampling Ratio

Increasing oversampling ratio (OSR) decreases in-band quantization noise as described in Section 2.2.1. However, high OSR increases the circuits complexity, area, and power consumption. Moreover, the maximum sampling clock rate is determined by the specific technology used to implement the circuit and the circuit architecture.

2.5.3 Quantizer Resolution

The resolution of the internal quantizer Q (as shown in Figure 2.16) can be one-bit or multi-bit. There are several benefits for a modulator to adopt a multi-bit quantizer. First, SNDR is improved due to reduced quantization noise. As a result, higher resolution can be achieved; Second, it tends to make a high-order modulator more stable because a multi-bit quantizer is not as easy to overload as an one-bit quantizer; Third, quantization noise tends to be more white with less idle tones. The drawbacks associated with using a multi-bit quantizer include requiring a multi-bit DAC in the feedback loop and more complex circuit design. Compared to one-bit DAC, multi-bit DAC is not inherently linear. Any non-linearities in the DAC are directly added to the modulator input signal without any attenuation, which can cause significant performance reduction. Methods are proposed to compensate for multi-bit DAC level errors including dynamic element matching (DEM) techniques [16], automatic on-chip current calibration [17], and careful DAC design [6].

2.5.4 Modulator Architecture

Two main architectures have been used to implement a high-order ΣΔ modulator including single-stage (as shown in Figure 2.16) and multi-stage. The main concern related to single-stage high-order ΣΔ modulator is the stability [18]. Multi-stage architecture solves the stability problem by cascading two or more low-order modulators to realize a high-order modulator. It is known as "MASH" topology, which stands for Multistage Noise-Shaping [19]. The main advantage of this architecture is that since low-order modulators are unconditionally stable, the stability of the overall modulator is guaranteed. In a multi-stage cascaded ΣΔ modulator, the quantization noise from a preceding stage is the input to the following stage. The quantization errors of all stages except the last one are cancelled by subsequent noise cancellation filters (NCFs) . Therefore, the modulator output contains only the input signal and the quantization noise of the last stage, which is noise-shaped by a NTF of the order equal to the overall order of the cascaded modulator.

Figure 2.17 shows a 1-1 second-order cascaded ΣΔ modulator, which is realized by cascading two first-order modulators. The output of the first and second stage Y_1, Y_2 can

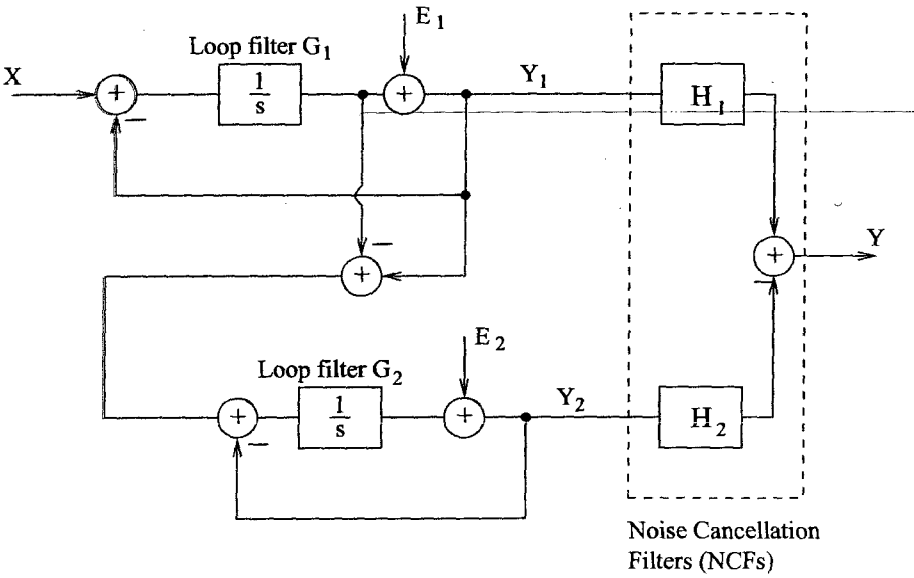


Figure 2.17: Linearized 1-1 second-order cascaded ΣΔ modulator.

be derived as follows:

$$Y_1 = X \cdot \frac{1}{1+s} + E_1 \cdot \frac{s}{1+s} \tag{2.11}$$

$$Y_2 = E_1 \cdot \frac{1}{1+s} + E_2 \cdot \frac{s}{1+s} \tag{2.12}$$

The final output of the modulator Y is:

$$\begin{aligned} Y &= Y_1 \cdot H_1 - Y_2 \cdot H_2 \\ &= \frac{1}{1+s} \cdot H_1 \cdot X + (\frac{s}{1+s} \cdot H_1 - \frac{1}{1+s} \cdot H_2) \cdot E_1 - \frac{s}{1+s} \cdot H_2 \cdot E_2 \end{aligned} \tag{2.13}$$

To cancel the first stage quantization noise E_1, the required transfer functions of the NCFs can be expressed in s-domain as follows:

$$H_1 = \frac{1}{1+s} \tag{2.14}$$

$$H_2 = \frac{s}{1+s} \tag{2.15}$$

Substituting Equation (2.14) and (2.15) into (2.13), the final output of the modulator is:

$$Y = \frac{1}{(1+s)^2} \cdot X - \frac{s^2}{(1+s)^2} \cdot E_2 \tag{2.16}$$

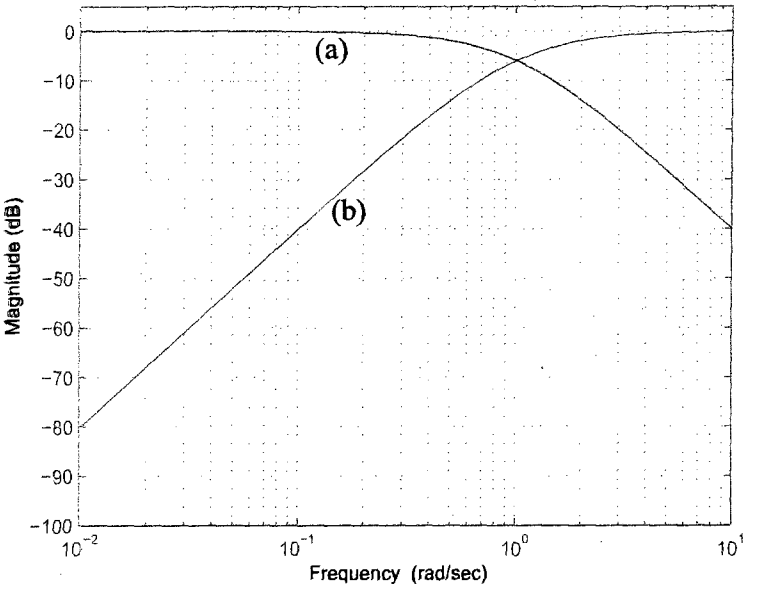


Figure 2.18: (a) STF and (b) NTF of the 1-1 second-order cascaded ΣΔ modulator.

According to Equation (2.16), the quantization noise E_2 of the second stage in the output of the modulator is now shaped away from baseband by a second order noise transfer function, while the input signal X is filtered by a low-pass transfer function. Figure 2.18 shows the NTF and STF of the modulator. The main disadvantage of a MASH modulator is that it is very sensitive to mismatch. For example, any deviation in the transfer function of the filters G_1, G_2 and H_1, H_2 will cause a mismatch in the elimination of the quantization noise E_1. As a result, the final output of the MASH modulator will contain the quantization noise of the first stage, which will significantly degrade the performance of the modulator. In theory, a MASH modulator can extend to as many stages as needed to achieve better noise suppression and higher resolution without stability concern. However, mismatch among different stages in practice limits the maximum number of stages.

2.5.5 Discrete-Time (DT) vs Continuous-Time (CT) Modulator

When the loop filter of a ΣΔ modulator is implemented using discrete-time circuits such as switched-capacitor (SC) [20] or switched-current (SI) circuits [21], the modulator is called discrete-time (DT) modulator. When it is implemented using continuous-time circuits such as transconductor-based integrators [22], the modulator is called continuous-time (CT) modulator. Compared with DT implementation, CT implementation has many advantages including relaxed sample-and-hold requirements, higher-speed operation, lower power consumption, and intrinsic anti-alias filtering. Moreover, unlike a DT modulator which is only suitable on MOS technology, a CT modulator can be implemented on MOS, BiCMOS, and bipolar technologies. However, the disadvantages of a CT modulator include higher clock jitter sensitivity, non-zero excessive loop delay [23, 24], and more sensitive to process variations. Figure 2.19 shows the simplified system-level block diagrams of a DT and CT modulator.

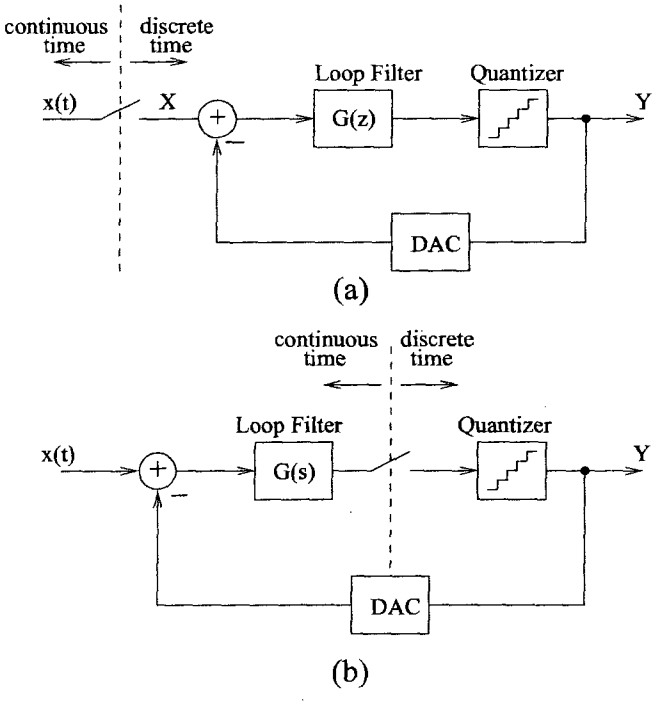


Figure 2.19: Block diagram of (a) a discrete-time modulator and (b) a continuous-time modulator.

The comparison between DT and CT modulators is shown in Figure 2.20.

DT modulator	CT modulator
Advantages • Less sensitive to process variation • Better clock jitter sensitivity • Loop filter scalble with clock	Advantags • Higher speed operation • Lower power consumption • Relaxed sampling circuit design • Intrinsic anti–aliasing filteing • Suitable for MOS, BiCMOS, bipolar
Drawbacks • Limited operation speed • High power consumption • High accuracy sampling network • Requiring off–chip anti–aliasing filter • Only suitable for MOS technology	Drawbacks • More sensitive to process variation • More sensitive to clock jitter sensitivity • Non–zero excess loop delay • Loop filter not scalble with clock

Figure 2.20: Comparison of DT and CT ΣΔ modulators.

Sampling Network Requirements

As can be seen in Figure 2.19, for the continuous-time modulator, the sampler is moved from the input of the discrete-time modulator to inside of the loop ahead of the quantizer. For the discrete-time modulator, sampling happens at the input of the modulator, any noise and distortion of the sampler is directly added to the input signal without any attenuation. As a result, the front-end sampler sets an upper limit on the performance of the entire modulator and has the most stringent noise and linearity requirements. Moreover, combination of a high oversampling clock rate and a low supply voltage of modern VLSI

technologies put tremendous design challenges on sampling switches. Due to the signal-dependent overdrive voltage, on-resistance and junction capacitances of a sampler switch also become signal-dependent [25]. This non-linear behavior seriously distorts the sampled signal. Boot-strapped switches have been proposed to alleviate the problem. However, it results in complex design and large power consumption [26]. Whereas for the continuous-time ΣΔ modulator, since sampling takes place inside of the loop, the noise and distortion of the sampling network is suppressed together with quantization noise by high in-band gain of the loop filter. Thus CT modulators have much more relaxed design requirements on sampling network when compared with discrete-time modulators.

Operating Clock Frequency

For discrete-time circuits such as switched-capacitor circuits, amplifiers are required to have high enough unit-bandwidth for internal signals to settle to a certain accuracy within half clock period. Usually the unity-bandwidth of the amplifiers must be five times the clock frequency to satisfy settling accuracy requirements [27]. On the contrary, there is no settling behavior involved in continuous-time circuits. Continuous-time modulators can potentially operate at much higher clock rate without worrying signal settling error. In [28, 29], it has been demonstrated that continuous-time ΣΔ modulators can operate at a clock as high as 2GHz to 4GHz. Whereas discrete-time ΣΔ modulators usually are clocked at below 200MHz [30, 31].

Power Consumption

For both DT and CT modulators, the most power consuming components are the op-amp based integrators in loop filters. Because DT op-amps are required to have bandwidth five times the clock frequency, they have high power consumption. On the other hand, there is no settling problems, the bandwidth of CT op-amps can be as low as the clock frequency. In general, continuous-time are 3 or 5 times more power efficient than DT integrators [32]. As a result, for the same signal bandwidth and resolution requirements, CT modulators need much less power than DT modulators.

Intrinsic Anti-Aliasing Filtering

For a DT modulator, an anti-aliasing filter in front of the modulator is required to sufficiently attenuate the frequency in aliasing band due to front-end sampling operation. For a high-speed modulator, the anti-aliasing filter design is not trivial and the filter might consume significant power which is undesirable in low-power systems. However, for CT modulators, as can be seen in Figure 2.11 and Figure 2.12, STFs show a low-pass transfer characteristic, which serves as an inherent anti-aliasing filter for input signals. Therefore, front-end anti-aliasing filters are normally not needed [33]. Even if they are needed in some cases, the requirements become so relaxed that it is very easy to implement the filters on-chip with low power consumption.

2.6 Clock Jitter Impact on a CT ΣΔ Modulator

Clock jitter is caused by sampling uncertainty, which increases noise power to the system [34]. In a CT ΣΔ modulator, jitter can occur at two places: sampler ahead of the internal quantizer and the DAC in the feedback loop. Since the jitter noise at the quantizer is heavily suppressed by the loop filter. This portion of noise presents little problem to the system. On the contrast, jitter noise induced at the DAC in the feedback loop is directly added to the signal path and go through STF without any attenuation. It has dominant effect on the overall performance of the CT ΣΔ modulator. Figure 2.21 shows an one-bit CT ΣΔ modulator with a non-return-to-zero (NRZ) DAC.

The output bit stream of the NRZ DAC with jitter is equivalent to an unjittered bit stream plus a stream of error sequence, resulting from the jitter as shown in Figure 2.22. The error sequence of the NRZ DAC is represented by [28]

$$e_{DAC}[n] = (y[n] - y[n-1]) \cdot \frac{\Delta t}{T_s} = \Delta y \cdot \frac{\Delta t}{T_s} \tag{2.17}$$

where T_s is the clock period, Δt (jitter) is the timing perturbation in the sampling instant, $y[n]$ is the n^{th} modulator output bit, and $\Delta y = y[n] - y[n-1]$.

Assuming Δt is not correlated to $\Delta y[n]$, error sequence $e_{DAC}[n]$ is almost white with

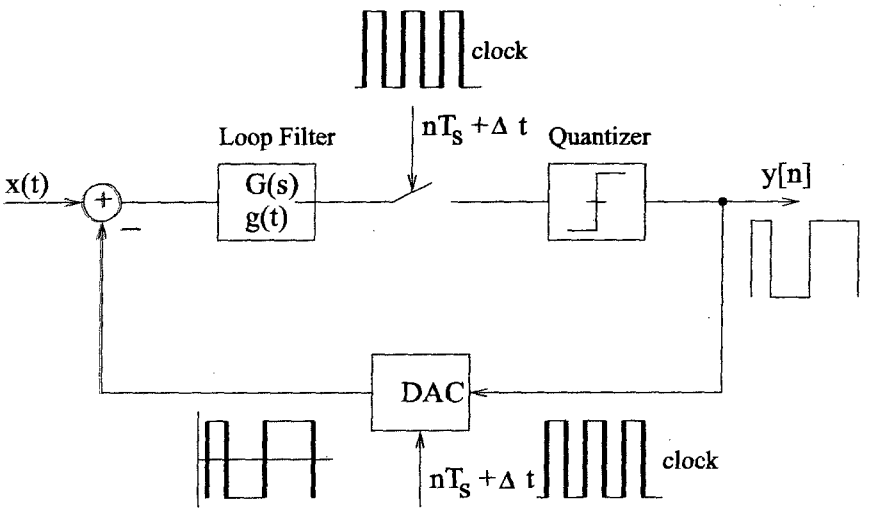


Figure 2.21: Clock jitter occurrence in a CT ΣΔ modulator.

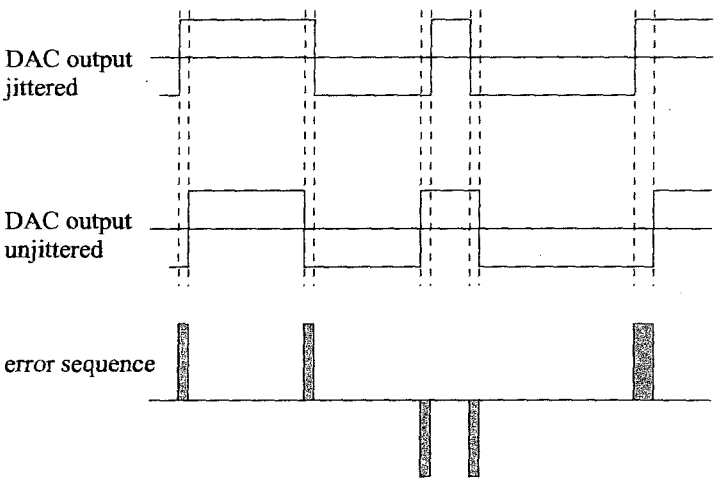


Figure 2.22: Equivalent representation of a jittered NRZ DAC output bit stream.

variance of:

$$\sigma^2_{e_{DAC}} = \sigma^2_{\Delta y} \cdot \frac{\sigma^2_{\Delta t}}{T_s^2} \tag{2.18}$$

The noise power of clock jitter within signal bandwidth f_b can be expressed as:

$$P_{jitter} = \frac{\sigma^2_{e_{DAC}}}{f_s/2} \cdot f_b = \frac{\sigma^2_{e_{DAC}}}{OSR} = \frac{\sigma^2_{\Delta y} \cdot \sigma^2_{\Delta t}}{OSR \cdot T_s^2} \tag{2.19}$$

Studies [35, 36] have shown that for high-performance continuous-time ΣΔ modulators, clock jitter surpasses quantization noise and becomes the limiting factor of performance. Many methods have been proposed to reduce the modulator sensitivity to clock jitter. Since jitter-induced noise is directly proportional to the pulse area of the DAC output, [37] suggests that adopting multi-bit quantizer and DAC can greatly reduce SNR degradation due to clock jitter.

There are three commonly used rectangular DAC feedback pulses including non-return-to-zero (NRZ), return-to-zero (RZ) and half-delay-return-to-zero (HRZ) . Their impulse responses are shown in Figure 2.23. So far we have only discussed jitter effect on a NRZ DAC. Research has shown that both RZ and HRZ DACs are more susceptible to jitter than NRZ DACs [28]. The reason is that clock jitter only causes errors when the output changes. RZ and HRZ DACs have both rising and falling edges occur every clock cycle so that they are affected by clock jitter more frequently. Figure 2.24 shows one-bit NRZ, RZ and HRZ DAC outputs affected by clock jitter with solid thick lines indicating the edges affected by clock jitter.

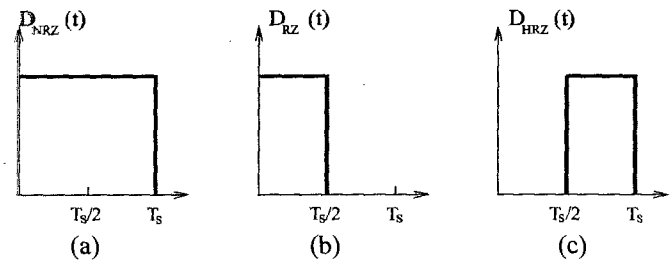


Figure 2.23: DAC feedback impulse responses of (a) NRZ (b) RZ (c) HRZ.

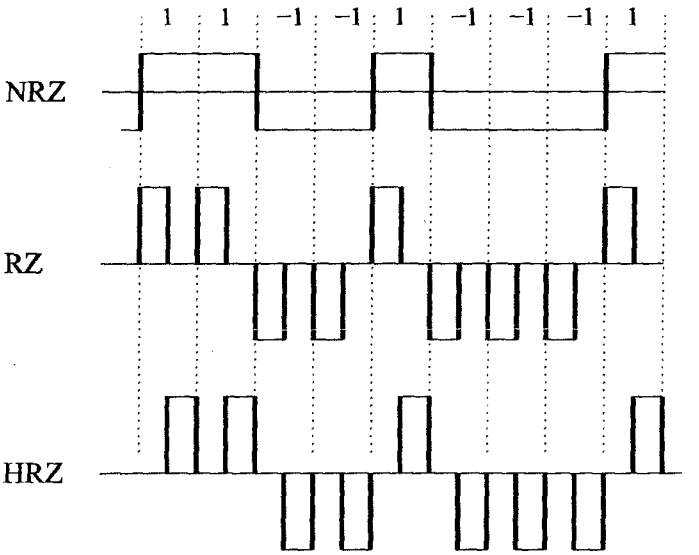


Figure 2.24: One-bit NRZ, RZ and HRZ DAC output with clock jitter noise.

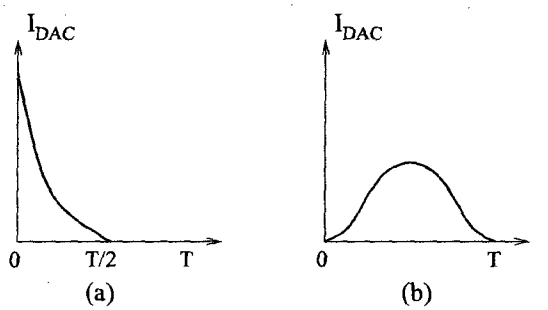


Figure 2.25: Alternative DAC output pulse shapes (a) exponential decaying (b) sine-shaped.

Alternative DAC shapes other than rectangular have been proposed to reduce jitter sensitivity in CT modulators as shown in Figure 2.25. The basic idea is to reduce the feedback signal amplitude near the edges of the clock so that clock perturbation in time has less effect compared with constant feedback amplitude shapes such as NRZ, RZ or HRZ. [38] analyzed a multi-bit DAC with exponential decaying pulse shape. Even though DAC with decaying pulse reduces the clock jitter sensitivity, it puts more stringent slew rate requirements on integrators and hence higher power consumption. [39] presented a sine-shaped DAC to alleviate the slew rate problem. However, it needs additional synchronization circuitry and introduces extra phase noise into the system.

2.7 Summary

In this chapter, some fundamental issues of CT ΣΔ modulators were reviewed. An analog-to-digital converter has two main operations including sampling and quantization. Sampling is a linear operation and can be lossless, whereas quantization is a nonlinear operation and causes information loss. It was shown that when certain conditions are met, a nonlinear quantizer model can be replaced by a linear stochastic model. Oversampling ADCs based on ΣΔ modulation work on two basic principles: oversampling and noise-shaping. Oversampling is achieved by using a sampling clock rate much higher than Nyquist rate, which reduces in-band quantization noise and relaxes anti-aliasing filter design. And noise-shaping is achieved by placing a quantizer in a feedback loop, which forces input signal and quantization noise to go through different transfer functions. There are many choices to be made when designing a ΣΔ modulator, including loop filter order, oversampling ratio, quantizer resolution, modulator architecture, and DT or CT implementation. For high-performance CT modulators, it is known that clock jitter limits the overall system performance. The methods that have been proposed to reduce jitter sensitivity were reviewed.

Chapter 3

System Level Design of a Wideband Low-Power CT ΣΔ Modulator

This chapter is mainly concerned with system-level design of a low-power CT ΣΔ modulator with 25MHz signal bandwidth. A survey on state-of-the-art continuous-time ΣΔ modulators with 10MHz+ signal bandwidth is given. Modulator architectures that are suitable for wideband applications are considered and compared. Following the discussion of the system architecture, an improved direct design methodology is presented to speed up the design process. Loop filter topologies are also examined for better power performance. Then, a fifth-order CT ΣΔ modulator with a 4-bit internal quantizer is proposed.

3.1 State of the Art

ΣΔ modulators are well known for their ability to achieve high resolution for low-to-medium speed applications. With the fast growing market of broadband wire-line and wireless communication services and systems, efforts have been made to extend the use of ΣΔ modulators to high-speed applications. Recent research has pushed signal bandwidth of CT ΣΔ modulators to 10MHz+ bandwidth range with 9 to 13-bits resolution using CMOS

Table 3.1: Performance Summary of State-of-the-Art Wideband (10MHz+) CT ΣΔ ADCs

Work	CMOS(μm)/ Supply(V)	BW (MHz)	Power(mW)/ DR(dB)	SNDR (dB)	Architecture order(bits)	F_s (MHz)	FOM (pJ)
Bre04/[2]	0.18/1.8	10	122/67	57	2-2(4b)cas.	160	3.42
Sch07/[3]	0.18/1.8	10	7.5/72	66	3(1b)	640	0.11
Pat04/[4]	0.13/1.5	15	70/67	63.7	4(4b)	300	1.31
Cal06/[5]	0.18/1.8	20	103/55.2	48.8	3(4b) inter.	200	5.39
Mit06/[6]	0.13/1.2	20	20/80	74	3(4b)	640	0.061

technology.

Breems *et al.* [2] designed a 2-2 cascaded CT modulator with 10MHz bandwidth in 0.18μm CMOS technology. The modulator achieves 67dB DR and 57dB SNDR with a clock frequency of 160MHz, consuming 122mW power. Digital noise cancellation filter with digital calibration circuit is required for matching purpose, which increases the power consumption of the modulator. Another modulator with 10MHz bandwidth by Schoolf *et al.* [3] has a dynamic range of 72dB and SNDR of 66dB with only 7.5mW power consumption. It is a third-order single-stage modulator implemented in 0.18μm CMOS with clock frequency of 640MHz. Low power feature is achieved through using G_m-C integrators and single stage architecture. Paton *et al.* [4] presented a modulator with 67dB DR over 15MHz bandwidth, dissipating 70mW power. It is implemented in 0.13μm CMOS technology and has sampling clock running at 300MHz.

Caldwell *et al.* [5] further increased signal bandwidth to 20MHz range. The modulator is time-interleaved realized in 0.18μm CMOS. It achieves 55.2dB DR 48.8dB SNDR with 103mW power consumption . Most recently, Mitteregger *et al.* [6] presented a ΣΔ modulator with 20mW power consumption in a 0.13μm CMOS technology. The modulator has 80dB DR and 74dB SNDR over 20MHz bandwidth. The performance summary of the state-of-the-art wideband (10MHz+) low-pass CT ΣΔ modulators is shown in Table 3.1.

3.2 System Design Techniques

3.2.1 Architecture Considerations

There are several architectures that have been successfully used to design wideband (10MHz+) low-pass continuous-time ΣΔ modulators, including cascaded topology with multi-bit quantization [2], time-interleaved multi-bit topology [5], and multi-bit single-loop topology [3, 4, 6].

Cascaded Multi-Bit Topology

Cascaded multi-bit sigma-delta modulators offer high resolution at relatively low oversampling ratios [31]. They use multiple stages in a cascaded configuration. By combining the digital outputs of all stages, higher order noise shaping can be achieved with low-order loop filters. For increased input bandwidth, desired resolution can be achieved by extending the number of stages without stability concern. Traditionally, cascaded ΣΔ modulators have been implemented solely with switched-capacitor (SC) circuits. This is because discrete-time ΣΔ modulators have the inherently good matching between the analog and digital filter coefficients, which is required to have good noise cancellation and hence high-order noise shaping in cascaded modulators.

The first continuous-time cascaded multi-bit sigma-delta modulator was proposed by Breems [2]. The block diagram of the modulator is shown in Figure 3.1. Compared with discrete-time cascaded modulator, it eliminates anti-alias filter [40]. However, matching between analog loop filter $G_{1,2}(s)$ and digital noise cancellation filter NCF becomes a problem. The coefficients of loop filter $G_{1,2}(s)$ are determined by absolute RC value which can vary in the order of 20% ,whereas coefficients of NCF are determined by capacitor ratios with matching in the order of 0.1% to 1%. As a result, calibration of either the analog filter $G_{1,2}(s)$ or the NCF is necessary to obtain high-order noise shaping. In [2], digital calibration of the NCF is employed. The proposed modulator achieves 67dB DR and 57dB SNDR over 10MHz bandwidth with 122mW power consumption.

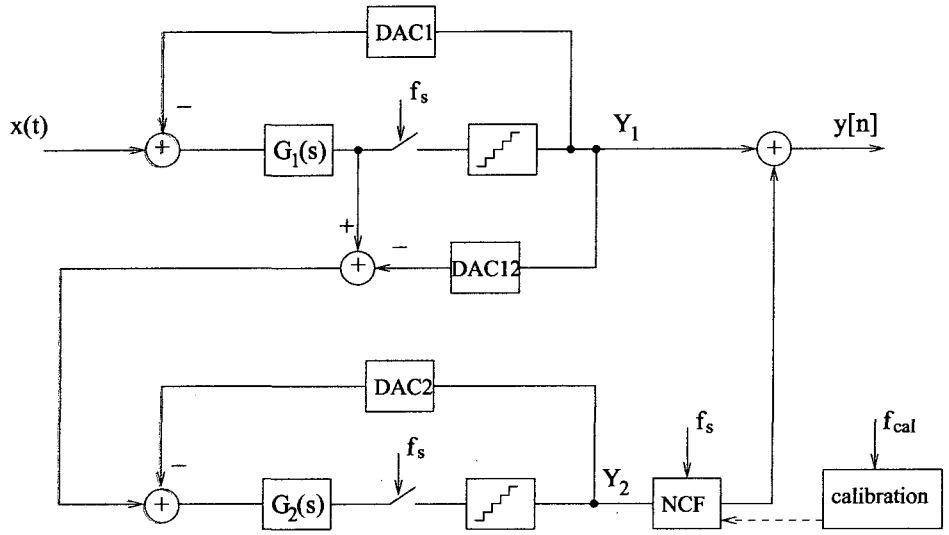


Figure 3.1: Cascaded multi-bit continuous-time sigma-delta modulator.

Time-Interleaved Multi-Bit Topology

Time-interleaved modulators use parallel structures to increases the effective sampling frequency without having to operate the circuits at higher frequencies [41]. By using interconnected M modulators working in parallel, the effective sampling rate becomes M times the clock rate of each modulator. In other words, required sampling rate can be achieved not by running higher clock rate but by increasing the number of modulators. As a result, the required resolution can be obtained for a desired signal bandwidth without utilizing a faster clock or using a higher order modulator. The idea here is to use block digital filtering in which a single-input single-output transfer function is realized by an equivalent block filter. A block digital filter is basically a multi-rate system using parallelism to reduce speed requirements on each processing element [42]. When an appropriate block digital filter is used for M parallel ΣΔ modulators, it was shown that the digital filters, the internal quantizers and feedback DACs in each parallel branch operate at 1/M of the original rate and the effective OSR of the time-interleaved configuration is

$$OSR_{eff} = M \times OSR \tag{3.1}$$

where OSR_{eff} is effective oversampling ratio of the time-interleaved modulator and OSR is the original oversampling ratio of the modulator. Figure 3.2 shows a conventional ΣΔ modulator and its equivalent modulator time-interleaved by 2. $\bar{G}(z)$ is the equivalent 2×2 block filter for $G(z)$.

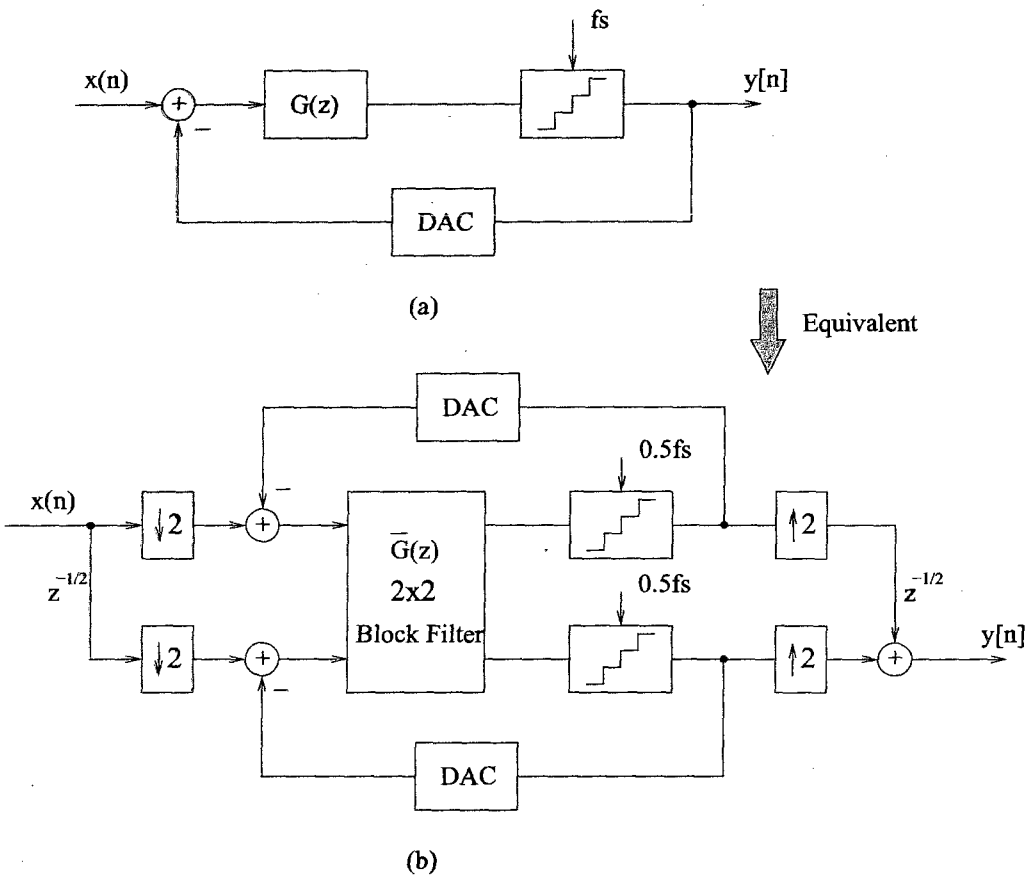


Figure 3.2: (a) Conventional modulator (b) Time-interleaved by 2 equivalent modulator.

As can be seen in Figure 3.2, the cost of increased effective OSR is an increase in hardware complexity since the circuit size increases by about the same factor that the effective OSR is increased. In [43, 44], some hardware reduction schemes were proposed to reduce hardware complexity and obtain more efficient architectures.

The first continuous-time ΣΔ time-interleaved modulator was proposed and imple-

mented by Caldwell [5]. The author demonstrated how a time-interleaved continuous-time ΣΔ modulator can be derived from a time-interleaved discrete-time ΣΔ modulator. The modulator achieves 55.2dB DR and 48.8dB SNDR over 20MHz signal bandwidth with 103mW power consumption. It operates at clock rate of 200MHz in 0.18μm CMOS technology. Carldwell [5] discovered that DAC feedback path matching requirement is much higher than non time-interleaved modulator. To obtain the desired 10-bit resolution, at least 0.5% DAC matching and much higher op-amp DC gain are necessary [5].

Single-Stage Multi-Bit Architecture

Single-stage architecture is the most common one used to build high resolution low speed ΣΔ modulators [29, 45, 46]. To use it in high speed applications while maintaining its high resolution, a higher order loop filter and a multi-bit internal quantizer must be utilized. For single-stage modulators with single-bit quantizer, the integrator gain has to be reduced to maintain the stability when the loop order is increased. As a result, little resolution and signal bandwidth improvement can be gained by simply increasing the loop filter order. By using multi-bit internal quantizer instead of single-bit quantizer, the stability of modulators is significantly improved [18]. Hence, more aggressive noise-shaping transfer function is allowed. Employing multi-bit internal quantizer also provides additional $20log_{10}(2^L - 1)dB$ resolution (where L is the bit number of internal quantization) improvement over single-bit quantization [47]. With more noise suppressed, signal bandwidth can be expanded with a desired resolution.

Yan [1] proposed a third-order single-stage CT modulator with a 5-bit internal quantizer as shown in Figure 3.3. The difference between Yan's modulator and commonly used single-stage modulators is that a second feedback path with DAC (DAC_B) is added. Additionally, one clock delay is inserted in front of the main feedback DAC (DAC_A) and a half clock delay is added in front of DAC_B. These purposely introduced delays are necessary to accommodate the nonzero time delay of the internal quantizer. Yan demonstrated that by doing so performance degradation due to the nonzero excess loop delay [24] and signal-dependent delay of the internal quantizer [23] can be eliminated. In the other words, the

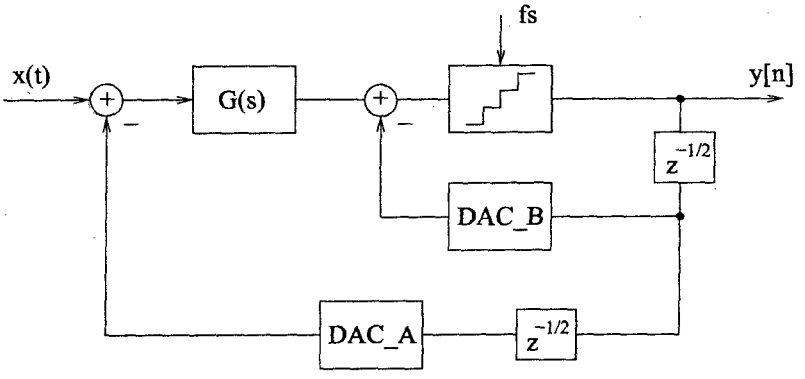


Figure 3.3: Single-stage multi-bit CT ΣΔ modulator proposed by Yan [1].

nonzero excess loop delay is accommodated at the architecture level design.

Non-idealities such as noise, offset, and nonlinearity of DAC_B are suppressed by high gain of the loop filter. Hence DAC_B nonlinearity due to mismatch is not a concern. As a result, power consumption contributed by DAC_B is insignificant. However, non-idealities of DAC_A are directly added on the input signal without any shaping. DAC_A requires an accuracy better than the target resolution of the modulator.

Table 3.2: Architecture Comparison for Wideband CT ΣΔ Modulators

	Cascaded	Time-Interleaved	Single-Stage
Achievable Bandwidth	High	High	High
Achievable DR	High	High	High
Have stability problem?	No	Yes	Yes
Matching Requirement	High	Modest	Low
Hardware Complexity	Modest	High	Low
Power Consumption	High	High	Low

The comparison between three wideband architectures is listed in Table 3.2. As can be seen in the table, single-stage multi-bit architecture has much simpler structure, less

matching requirements, and low power consumption. For these reasons we choose single-stage architecture in this work.

3.2.2 Design Methodology

ΣΔ Modulator Design Flow

Due to the complex nature of a ΣΔ modulator, design process is iterative hence time consuming [48]. The system-level design flow of a continuous-time ΣΔ modulator used in this work is shown in Figure 3.4.

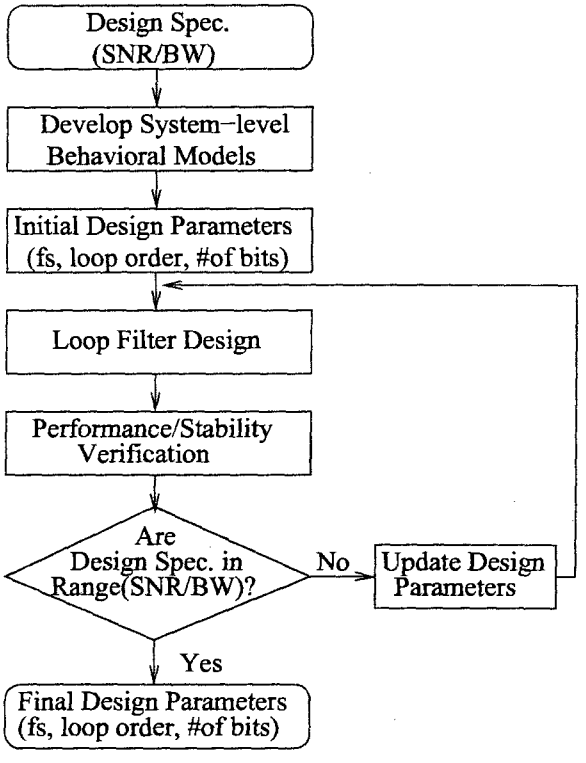


Figure 3.4: System-level design flow of a ΣΔ modulator.

During the design process, there are three design parameters need to be determined. They are sampling frequency f_s, loop filter order, and internal quantizer resolution(# of

bits). The transfer function of the loop filter needs to be designed once f_s and loop filter order are known. The design flow starts with the target specifications including desired signal-to-noise ratio (SNR) and signal bandwidth (BW) . Behavioral model of the modulator is then developed using hardware description language *Verilog-A*. With the initial design parameters f_s, loop filter order, and # of bits, loop filter transfer function $G(s)$ is designed using a method described in the following section. Simulations are conducted on the behavioral model in *Cadence Analog-Artist* design environment using *Spectre* simulator to verify the stability and performance. If the modulator is not stable and/or the target design specifications are not met, design parameters are updated and the loop filter is redesigned. Stability and performance are verified again with the new design parameters and loop filter. The process goes on until the modulator is stable and the target performance is achieved. Loop filter transfer function $G(s)$ design is the most important step in the design flow because not only it is the most time-consuming step but also $G(s)$ is directly related to noise shaping performance and system stability [18]. Process variations of the design technology affect the implementation of the loop filter transfer function, which is dealt with in the next chapter.

An Improved Direct Design Method

There are two ways to design a CT loop filter: DT to CT mapping method [40, 49] and direct design method [4]. DT to CT mapping is the most commonly used design technique. A DT filter is first designed to meet both stability and performance requirements. Then, an impulse-invariant transformation is applied to find the corresponding CT filter transfer function. This design method takes advantage of the large existing literature regarding DT ΣΔ modulator design. In this work, we prefer the direct design method, in which a stable loop filter is directly designed in CT domain. This method speeds up the design process by eliminating DT to CT transformation and by analyzing stability directly in CT domain.

The existing direct design method described in [4] gives no details on how the loop filter transfer function $G(s)$ is obtained. Moreover, stability is tested in DT domain, which requires CT to DT transformation [50]. In this work we propose a direct design method

in which poles and zeros of $G(s)$ are placed directly in s-domain to meet stability and performance criteria. It follows three steps. First, we place the poles of $G(s)$ at the optimal position for best noise performance. Second, we find zeros with which the modulator is marginally stable. The last step is to find the actual zeros with which the modulator is stable for the desired input signal range. Detailed design process is described below followed by a design example.

We define in-band gain of the loop filter $G(s)$ as the function Ψ with

$$\Psi = \int_0^{\omega_b} |G(j\omega)|^2 d\omega \tag{3.2}$$

where $\omega_B = 2\pi f_b/f_s$ is the normalized signal bandwidth with the desired signal bandwidth f_b and the sampling frequency of f_s. $G(s)$ can be written as

$$G(s) = \frac{h(s)}{g(s)} \tag{3.3}$$

where $h(s)$ is the numerator and $g(s)$ is the denominator of $G(s)$. For better in-band noise suppression, function Ψ must be maximized. Since in-band gain is mainly determined by the denominator $g(s)$ instead of numerator $h(s)$ [51], we have the equation as follows

$$\begin{aligned} \max(\Psi) &= \max\Big(\int_0^{\omega_B} |G(j\omega)|^2 d\omega\Big) \\ &= \max\Big(\int_0^{\omega_B} \Big|\frac{h(j\omega)}{g(j\omega)}\Big|^2 d\omega\Big) \\ &\approx \min \int_0^{\omega_B} |g(j\omega)|^2 d\omega \end{aligned} \tag{3.4}$$

Optimal locations of poles of the loop filter $G(s)$ can be found for maximal in-band noise performance by using the above equation.

Zeros of $G(s)$ are determined by system stability and placed as far as stability allows [52]. In this work, we first present an extended s-domain stability model for a single-stage multi-bit ΣΔ modulator with second DAC feedback loop. Added delay elements in both DAC feedback paths are modeled. An algorithm is presented to generate the root-locus diagram of the modulator with time delay elements. Using the time delay root locus, we locate the zeros of $G(s)$ with which the modulator is stable. The root locus of a ΣΔ modulator is different from that of a linear system, for which a choice can be made to fix the closed-loop

system poles at a desired location on the locus. For a ΣΔ system the closed-loop poles can not be fixed since the variable gain k of the internal quantizer moves the poles along the locus [53]. Small signl stability of a ΣΔ modulator is defined as: there must be a non-empty range of inputs for the gain parameter k for which all the roots of the system characteristic equation reside in the left-hand side of the imaginary axis in the s-plane [54].

Figure 3.5 is the redrawn of the modulator from Figure 3.3. The corresponding s-domain stability model of the modulator is shown in Figure 3.6.

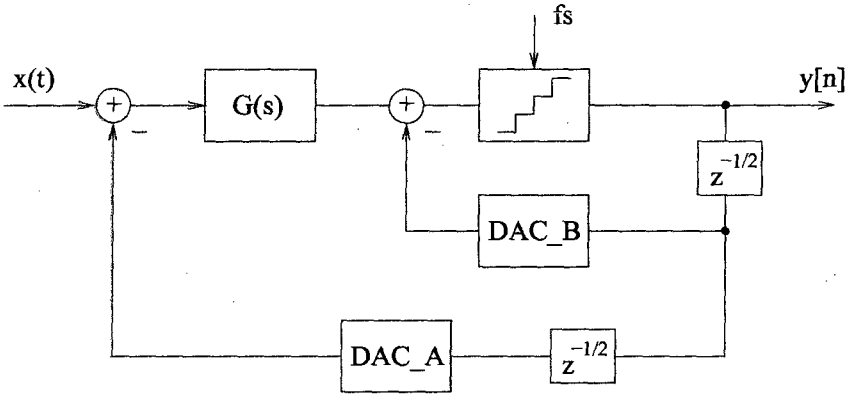


Figure 3.5: Wideband single-stage multi-bit CT ΣΔ modulator (Redrawn of Figure 3.3).

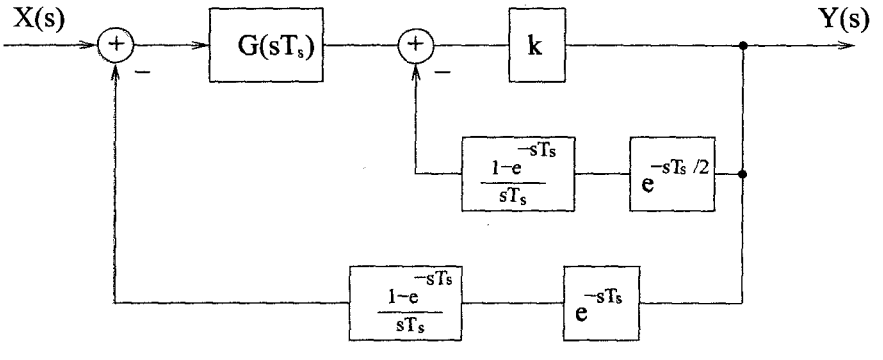


Figure 3.6: Corresponding stability model of the modulator in Figure 3.5.

The multi-bit quantizer is modeled as a variable gain k [53]. The half clock delay element is modeled in s-domain as $e^{-sT_s/2}$ and one clock delay is modeled as e^{-sT_s}. Both DAC_A and DAC_B are NRZ with zero-order-hold (ZOH) transfer characteristic [7]. Since sampling operation introduces a gain of $1/T_s$ into the system, we combine the sampling gain and the DACs together to form the transfer function as follows:

$$DAC(s) = \frac{1}{T_s} \cdot \frac{1 - e^{-sT_s}}{s} \tag{3.5}$$

The normalized characteristic equation of the modulator can be written as follows:

$$1 + G(s) \cdot k \cdot e^{-s} \cdot \frac{1 - e^{-s}}{s} + k \cdot e^{-s/2} \cdot \frac{1 - e^{-s}}{s} = 0 \tag{3.6}$$

Due to the time delay elements, there is no closed-form solution to (3.6). A numerical root finding method is required. The algorithm presented here to generate the time-delay root locus of the modulator is based on the theorem by Krall [55, 56]. It is described as follows:

1. Dividing both sides of (3.6) by ke^{-2s}.

$$\frac{1}{ke^{-2s}} = \frac{G(s)}{s} \cdot (1 - e^{s}) + \frac{1}{s} \cdot (e^{\frac{1}{2}s} - e^{\frac{3}{2}s}) \tag{3.7}$$

2. Substituting $s = x + jy$ into the above equation.

$$\begin{aligned} \frac{1}{k} \cdot \left[e^{2x}cos(2y) + je^{2x}sin(2y)\right] &= Re\Big(\frac{G(s)}{s} \cdot (1 - e^{s}) + \frac{1}{s} \cdot (e^{\frac{1}{2}s} - e^{\frac{3}{2}s})\Big) \\ &+ Im\Big(\frac{G(s)}{s} \cdot (1 - e^{s}) + \frac{1}{s} \cdot (e^{\frac{1}{2}s} - e^{\frac{3}{2}s})\Big) \end{aligned} \tag{3.8}$$

We define a new function Φ as:

$$\Phi = \frac{G(s)}{s} \cdot (1 - e^{s}) + \frac{1}{s} \cdot (e^{\frac{1}{2}s} - e^{\frac{3}{2}s}) \tag{3.9}$$

The equation (3.8) can be rewritten as:

$$\frac{1}{k} \cdot \left[e^{2x}cos(2y) + je^{2x}sin(2y)\right] = Re(\Phi) + jIm(\Phi) \tag{3.10}$$

where $Re(\Phi)$ is the real part of Φ and $Im(\Phi)$ is the imaginary part of the Φ.

3. Taking the real and imaginary parts of (3.10) and eliminating k.

$$\frac{1}{k} \cdot e^{2x} \cdot cos(2y) + j\frac{1}{k} \cdot e^{2x} \cdot sin(2y) = Re(\Phi) + jIm(\Phi) \tag{3.11}$$

$$\Longrightarrow \begin{cases} \frac{1}{k} \cdot e^{2x} \cdot cos(2y) &= Re(\Phi) \\ \frac{1}{k} \cdot e^{2x} \cdot sin(2y) &= Im(\Phi) \end{cases} \tag{3.12}$$

$$\Longrightarrow \frac{cos(2y)}{sin(2y)} = \frac{Re(\Phi)}{Im(\Phi)} \tag{3.13}$$

4. The point $s = x + jy$ is on the root locus if and only if (x, y) satisfies the following equation:

$$Re(\Phi) \cdot sin(2y) = Im(\Phi) \cdot cos(2y) \tag{3.14}$$

5. The value of k which is corresponding to the point (x, y) on root locus can be calculated using

$$k = \frac{e^{2x} \cdot cos(2y)}{Re(\Phi)} \tag{3.15}$$

or

$$k = \frac{e^{2x} \cdot sin(2y)}{Im(\Phi)} \tag{3.16}$$

Bisection numerical method [57] is implemented in C/C++ to find roots of (3.14). The root locus of the modulator can subsequently be plotted. The C/C++ program code developed in this work is listed in Appendix C.

The root locus diagram gives us the zeros of $G(s)$ with which modulator is marginally stable. They serve as the starting point for a design process. Further time-domain simulations are necessary to find the actual zeros with which the modulator is stable for the desired input signal range.

Design Example

A third order $G(s)$ is used here to illustrate how loop filter transfer function is designed using the proposed method. The $G(s)$ has the following form:

$$G(s) = \frac{s^2 + r \cdot s + r^2}{s \cdot (s^2 + p^2)} \tag{3.17}$$

where $G(s)$ has three poles at 0 and $\pm jp$. It also has two zeros determined by the value of r. The pole-zero diagram of $G(s)$ is shown in Figure 3.7.

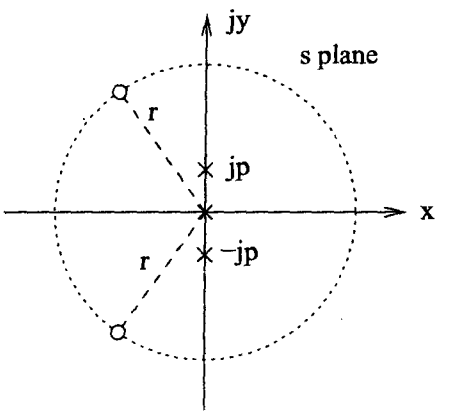


Figure 3.7: Pole-zero diagram of loop filter $G(s)$ in (3.17).

To design $G(s)$, we first calculate the optimal poles $\pm jp$ using (3.4).

$$\begin{aligned} \max(\Phi) &= \max\Big(\int_0^{\omega_B} |G(j\omega)|^2 d\omega\Big) \\ &\Longrightarrow \min \int_0^{\omega_B} |j\omega \cdot ((j\omega)^2 + p^2)|^2 d\omega \\ &\Longrightarrow \pm jp = \pm j0.7745967 \cdot \omega_B \end{aligned} \tag{3.18}$$

where $\omega_B = 2\pi f_b/f_s$ is the normalized signal bandwidth. We have $\omega_B = \pi/16 = 0.19634954$ wiht OSR=16. The optimal poles are then calculated as $\pm jp = j0.7745967 \cdot \omega_B = \pm j0.1521$.

With the optimal $G(s)$ poles, $G(s)$ zeros are located by using time-delay root locus algorithm. Three closed-loop pole trajectories as a function of k are plotted in Figure 3.8 with loop filter parameters $r = 0.2, 0.352, 0.574$. Since the root locus is symmetric around the real axis, only the top half is shown. The outermost root locus in Figure 3.8 is for $r = 0.574$. This modulator is of no use since it is unstable for all input signals. The innermost pole trajectory has parameter of $r = 0.2$, which intersects the imaginary axis. The poles of this system will enter the left-hand side for moderate values of k. This system can be considered stable for small signals. For $r = 0.352$, the root locus is tangent to the

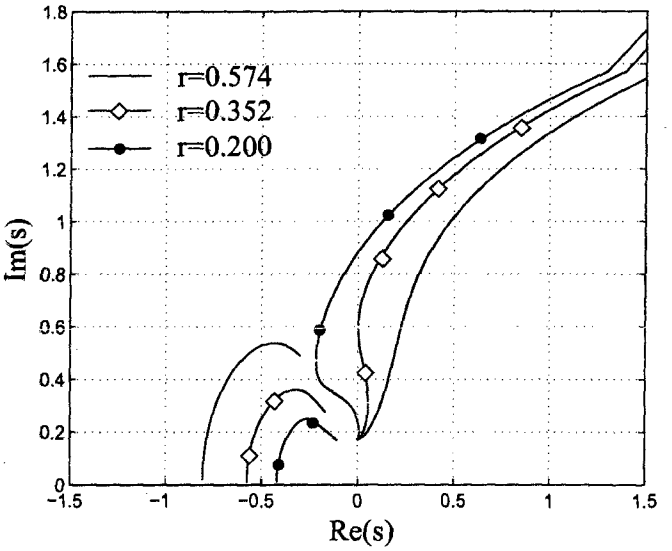


Figure 3.8: Root locus of the third-order ΣΔ modulator for different values of r.

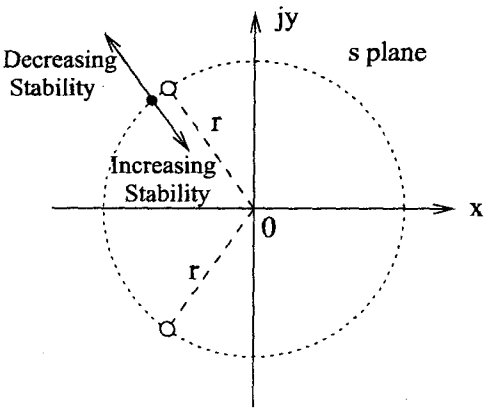


Figure 3.9: Impact of the zeros of $G(s)$ on system stability.

imaginary axis. This modulator is marginally stable for small signals. As can be seen, increasing r will decrease the system stability and decrease r will increase the stability as shown in Figure 3.9. The value of r, with which the root locus is tangent to the imaginary axis, may serve as the starting point for the design process.

3.2.3 Proposed Fifth-Order CT ΣΔ Modulator

In this work we employ the single-stage multi-bit architecture for the reasons discussed in previous section. The design target for this research is to achieve better than 70dB dynamic range over 25MHz signal bandwidth with very low power consumption. Table 3.3 shows the preliminary design specifications of this work.

Table 3.3: Preliminary Design Specifications of This Work

Singal Bandwidth	$25MHz$
Dynamic Range	$> 70dB$
SNDR	$70dB$
Voltage Supply	$1.0V$
Power Consumption	$< 20mW$
Technology	STM 7M2T 90nm CMOS

After the architecture and design target specifications are known, system-level design parameters including sampling frequency (f_s), loop filter order, and quantizer resolution (# of bits) are determined using the design flow shown in Figure 3.4. The peak SNDR is set to 76dB to allow 6dB margin for circuit implementation. The system is modeled using *Verilog-A* in *Cadence Design Framework II* ™. The final design parameters which meet our design target are listed in Table 3.4.

Loop Filter Transfer Function Design

The improved direct design method is applied to find the optimal poles/zeros of the fifth-order loop filter $G(s)$, which has the general form of:

Table 3.4: Final Design Parameters

Sampling Frequency f_s	$800MHz$
Loop Filter Order	5
Quantizer Resolution(# of Bits)	4

$$G(s) = k \cdot \frac{(s^2 + \frac{r_1}{q_1}s + r_1^2)(s^2 + \frac{r_2}{q_2}s + r_2^2)}{s(s^2 + p_1^2)(s^2 + p_2^2)} \tag{3.19}$$

Pole-zero diagram of the loop filter $G(s)$ is shown in Figure 3.10 with $\theta_1 = arccos(1/2q_1)$ and $\theta_2 = arccos(1/2q_2)$.

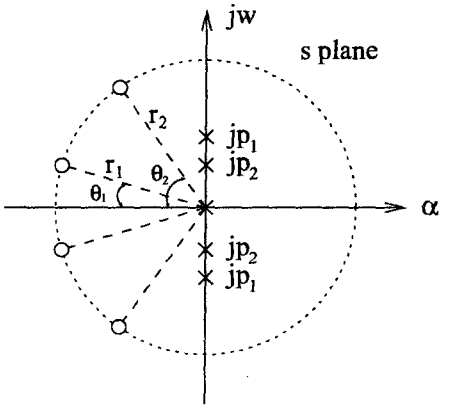


Figure 3.10: Pole-zero diagram of the loop filter $G(s)$ in Eq. (3.19).

Poles are placed in optimal positions so that the gain provided by the loop filter for in-band signals is maximized. Optimal poles can be found by maximizing the function Ψ.

$$\begin{aligned} \max(\Psi) &= \max\Big(\int_0^{\omega_B} |G(j\omega)|^2 d\omega\Big) \\ &\Longrightarrow \min\Big(\int_0^{\omega_B} \omega^2 \cdot (p_1^2 - \omega^2)^2 \cdot (p_2^2 - \omega^2)^2 d\omega\Big) \\ &\Longrightarrow p_1^2 = 0.8211619\omega_B^2 \qquad p_2^2 = 0.2899492\omega_B^2 \end{aligned} \tag{3.20}$$

where $\omega_B = 2\pi f_b/f_s$ with $f_b = 25MHz$ and $f_s = 800MHz$.

Zeros are placed as far as stability allows. The time-delay root locus algorithm is used to find the zeros with which the modulator is marginally stable. Within this stability boundary, time-domain simulations are conducted to find the values of zeros that can accommodate the desired input signal range. The final loop filter of the modulator has the transfer function of:

$$\begin{aligned} G(s) &= \frac{a_4 s^4 + a_3 s^3 + a_2 s^2 + a_1 s + a_0}{s(s^2 + p_1^2)(s^2 + p_2^2)} \\ &= \frac{1.2s^4 + 0.4725s^3 + 0.14718375s^2 + 0.02083725s + 0.00233377}{s(s^2 + 0.0317)(s^2 + 0.0112)} \end{aligned} \tag{3.21}$$

Loop Filter Topology Consideration

There are two general topologies which may be used to implement the modulator with the $G(s)$ of (3.21). They are known as feed-forward topology and feedback topology [58]. For the feed-forward topology, the weighted sum of all integrator outputs is fed forward to the quantizer and the latter's output is fed back to the first integrator, as shown in Figure 3.11. For the feedback topology, only the output of the last integrator is fed to the quantizer, and the latter's output is fed back to the input of each integrator, as shown in Figure 3.12. We compare these two filter topologies in terms of overall STF, NTF, and internal NTFs, and internal signal swing.

For both topologies, $X(s)$ is the input, $Y(s)$ is the output, and $E(s)$ is the quantization noise. n_1, n_2, n_3, n_4, n_5 are the internal nodes at each integrator's input. We have $Y(s)$ as

$$Y(s) = STF(s) \cdot X(s) + NTF(s) \cdot E(s) \tag{3.22}$$

and loop filter $G(s)$ as

$$G(s) = \frac{a_4 s^4 + a_3 s^3 + a_2 s^2 + a_1 s + a_0}{s(s^2 + p_1^2)(s^2 + p_2^2)} = \frac{h(s)}{g(s)} \tag{3.23}$$

where $h(s)$ is the nominator equal to $a_4 s^4 + a_3 s^3 + a_2 s^2 + a_1 s + a_0$ and $g(s)$ is the denominator equal to $s(s^2 + p_1^2)(s^2 + p_2^2)$ with:

$$\begin{aligned} p_1^2 &= g_1 k_2 k_3 \\ p_2^2 &= g_2 k_4 k_5 \end{aligned} \tag{3.24}$$

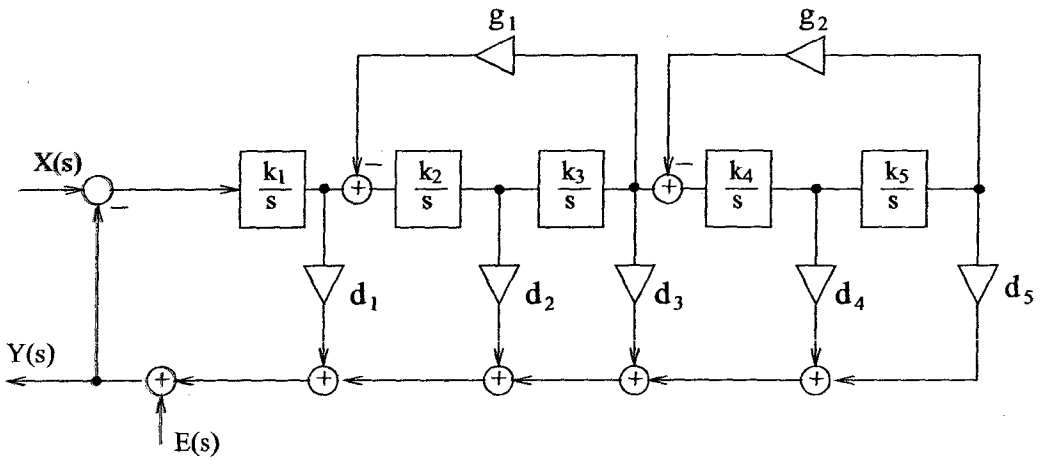


Figure 3.11: Feed-forward filter topology.

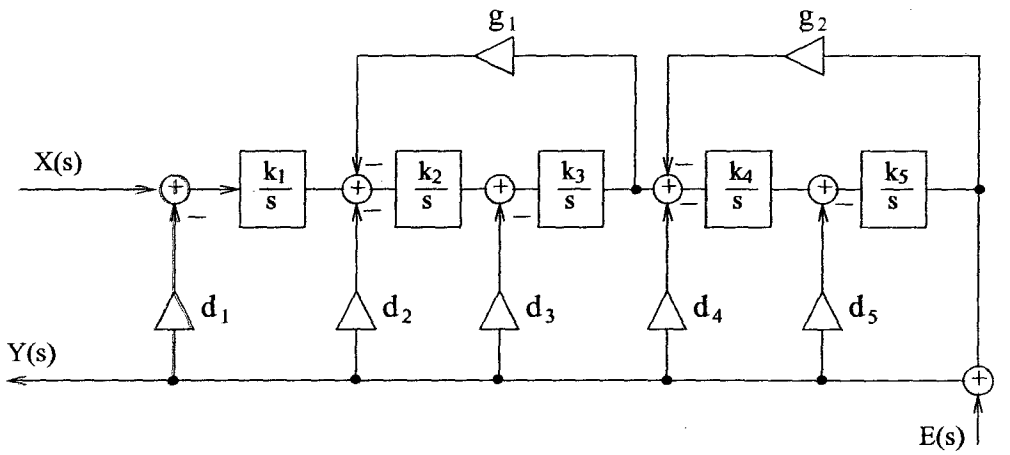


Figure 3.12: Feedback filter topology.

For feed-forward topology, the coefficients of the modulator can be derived from:

$$\begin{aligned} a_4 &= d_1k_1 \\ a_3 &= d_2k_1k_2 \\ a_2 &= d_1k_1(p_1^2+p_2^2)+d_3k_1k_2k_3 \\ a_1 &= d_2k_1k_2p_2^2+d_4k_1k_2k_3k_4 \\ a_0 &= d_1k_1p_1^2p_2^2+d_3k_1k_2k_3p_2^2+d_5k_1k_2k_3k_4k_5 \end{aligned} \tag{3.25}$$

Similarly, the coefficients of the feedback topology can be derived from:

$$\begin{aligned} a_4 &= d_5k_5 \\ a_3 &= d_4k_4k_5 \\ a_2 &= d_3k_3k_4k_5+d_5k_5p_1^2 \\ a_1 &= d_2k_2k_3k_4k_5+d_4k_4k_5p_1^2 \\ a_0 &= d_1k_1k_2k_3k_4k_5 \end{aligned} \tag{3.26}$$

As we can see in the above equations, the roles played by gains associated with each integrator in determining the nominator coefficients are reversed in the two topologies. For example, the coefficient of a_4 is given by the gain of the first integrator in feed-forward topology. The same coefficient is given by the gain of the last integrator in the feedback topology. It has been proven [31] that in the feed-forward topology, it follows $k_1 > k_2 > k_3 > k_4 > k_5$ and $k_1 < k_2 < k_3 < k_4 < k_5$ for feedback topology. As far as input-referred noise is concerned, the closer an integrator is to the input, the higher its gain needs to be to scale down the contributions of all subsequent noise sources. A feed-forward topology therefore has a better chance of achieving lower noise for the same power consumption.

For feed-forward topology (Figure 3.11), NTF and STF are derived as following:

$$\begin{aligned} NTF(s) &= \frac{1}{1+G} \\ STF(s) &= \frac{G}{1+G} = \frac{h(s)}{h(s)+g(s)} \end{aligned} \tag{3.27}$$

For feedback topology (Figure 3.12), NTF and STF are derived as following:

$$\begin{aligned} NTF(s) &= \frac{1}{1+G} \\ STF(s) &= \frac{k_1 k_2 k_3 k_4 k_5}{h(s)+g(s)} \end{aligned} \tag{3.28}$$

As can be seen in (3.27) and (3.28), two topologies share the same NTF but have different STF. For feed-forward topology, signal transfer function has five poles and four zeros with roll-off $-20dB/dec$ near signal alias region. For feedback topology, signal transfer function has five poles and no zeros with $-100dB/dec$ roll-off. Feedback topology therefore has much stronger anti-alias filtering than feed-forward topology.

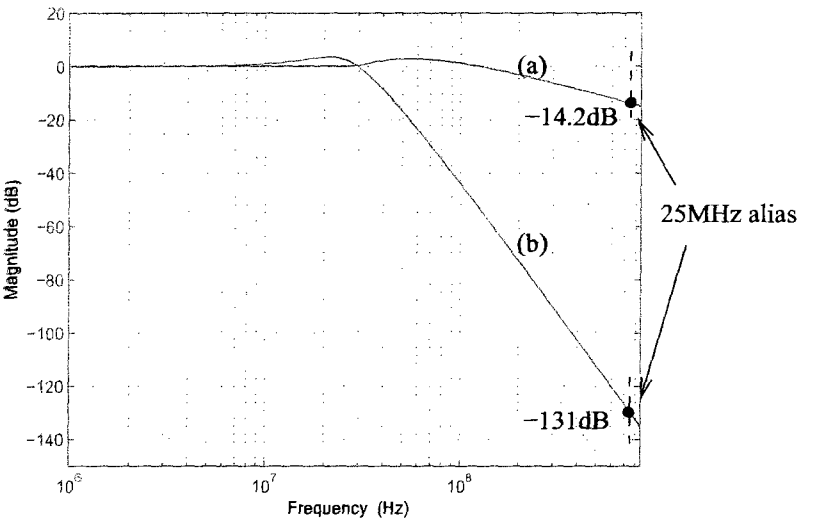


Figure 3.13: Signal transfer function of (a) feed-forward (b) feedback topology.

The signal transfer functions for both topologies are plotted in Figure 3.13. For the modulator with 800MHz sampling clock rate, 25MHz alias appears at 775MHz. Figure 3.13 shows that -14.2dB suppression on the 25MHz alias frequency in feed-forward configuration, whereas feedback topology provides -131dB suppression on the same alias frequency.

Noise transfer functions at internal nodes n_1, n_2, n_3, n_4, and n_5 are denoted as NTF_1,

NTF_2, NTF_3, NTF_4, NTF_5, respectively. NTF_1 is the NTF for any noise added at the input of the first integrator; NTF_2 is the NTF for any noise added at the input of the second integrator and so on. It is important to know the internal NTFs because they determine the design requirements for the integrators.

For feed-forward topology (Figure 3.11):

$$\begin{aligned} NTF_1(s) &= \frac{h}{h+g} \\ NTF_2(s) &= \frac{h \cdot s}{(h+g) \cdot k_1} \\ NTF_3(s) &= \frac{h \cdot (s^2+p_1^2)}{(h+g) \cdot k_1 k_2} \\ NTF_4(s) &= \frac{h \cdot s(s^2+p_1^2)}{(h+g) \cdot k_1 k_2 k_3} \\ NTF_5(s) &= \frac{h/(k_1 k_2 k_3 k_4)}{s(1+G(s))} \end{aligned} \tag{3.29}$$

For feedback topology (Figure 3.12):

$$\begin{aligned} NTF_1(s) &= \frac{k_1 k_2 k_3 k_4 k_5}{h+g} \\ NTF_2(s) &= \frac{k_2 k_3 k_4 k_5 \cdot s}{h+g} \\ NTF_3(s) &= \frac{(s^2+p_1^2) \cdot k_3 k_4 k_5}{h+g} \\ NTF_4(s) &= \frac{s(s^2+p_1^2) \cdot k_4 k_5}{h+g} \\ NTF_5(s) &= \frac{k_5}{s(1+G(s))} \end{aligned} \tag{3.30}$$

The internal noise transfer functions are plotted in Figure 3.14 and Figure 3.15. Comparing the two figures, it is obvious that feed-forward topology has much higher internal noise suppression than the feedback topology. It translates to much relaxed circuit requirements, which may save significant power consumption.

Due to the extremely low power supply voltage (1.0V) of 90nm CMOS technology, the internal signal swings must be kept small for the modulator not to overload. For feed-forward topology, only the first integrator has a large feedback input. Hence it has much smaller internal signal swing than the feedback one. Moreover, feed-forward filter can be

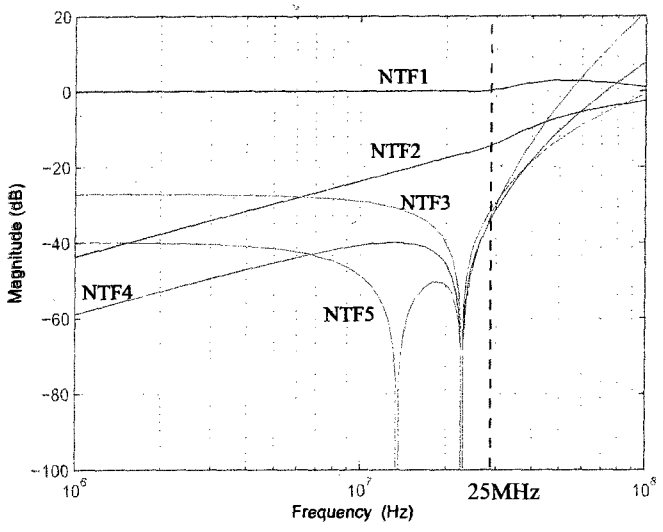


Figure 3.14: Internal noise transfer functions of feed-forward topology.

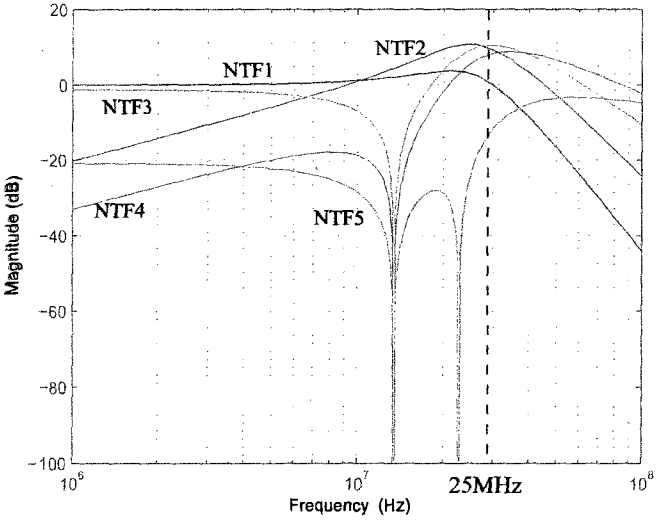


Figure 3.15: Internal noise transfer functions of feedback topology.

designed to remain stable during overload [32]. While the feedback filter needs overload detection and reset circuit to remain stable.

Table 3.5: Comparison of Two Filter Topologies

	Feed-Forward Topology	Feedback Topology
Anti-Alias Filtering	Weak	Strong
Circuit Requirements	Relaxed	High
Internal Signal Swing	Small	Large
Stability	Remain Stable	Overload Detection and Reset
Power Consumption	Low	High

Comparison of these two filter topologies are listed in Table 3.5. Feedback topology has very strong anti-alias filtering. However, feed-forward topology has advantages of low power consumption and much relaxed circuit requirements. Additionally, it has lower internal signal swing which is well suited for nanometer CMOS implementation. Moreover, by careful design, a feed-forward modulator can remain stable without using any overload detection and reset circuit. For these reasons, we choose feed-forward filter topology in this work.

The Proposed ΣΔ Modulator

The proposed fifth-order CT ΣΔ modulator is shown in Figure 3.16. The modulator has oversampling ratio of 16 with 800MHz sampling clock. The corresponding signal transfer function (STF) and noise transfer function (NTF) plots are shown in Figure 3.17. The gain of STF within 25MHz signal bandwidth varies less than 0.2dB.

As can be seen in Figure 3.16, a second DAC (DAC_B) is looped around the quantizer to compensate its delay. A feed-forward path with gain of d_0 is added to further reduce the internal signal swings, which allows us to scale up the integrator coefficients k_1 to k_5 to suppress circuit noise. Half clock delay is added in front of DAC_A to absorb signal-dependent delays. The coefficient values of the proposed modulator are listed in Table 3.6.

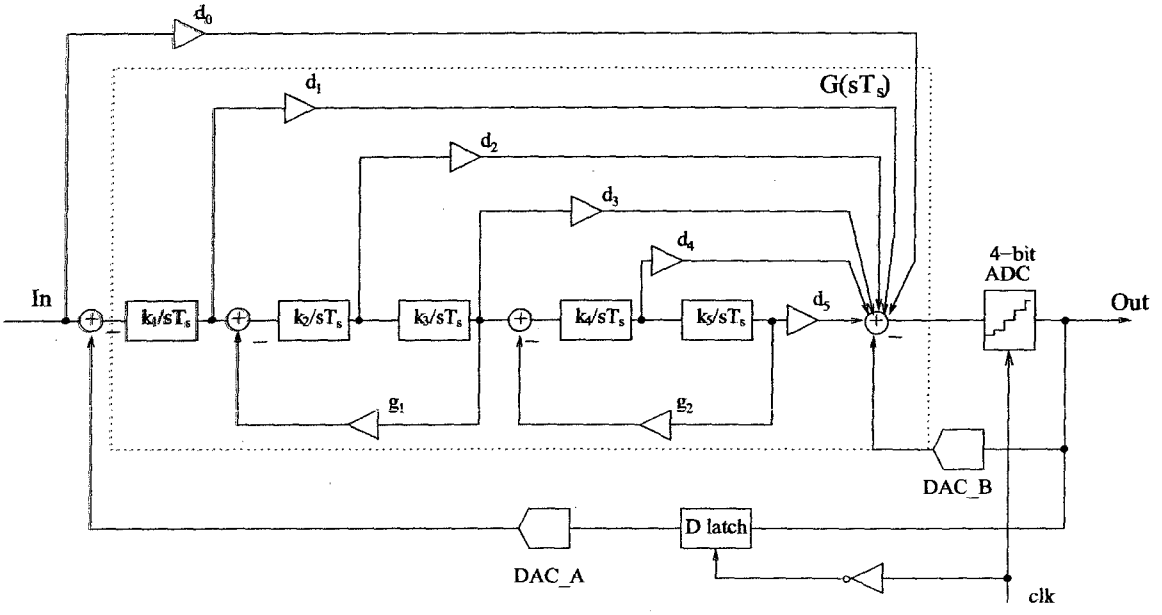


Figure 3.16: Proposed 5^{th}-order ΣΔ modulator with feed-forward topology.

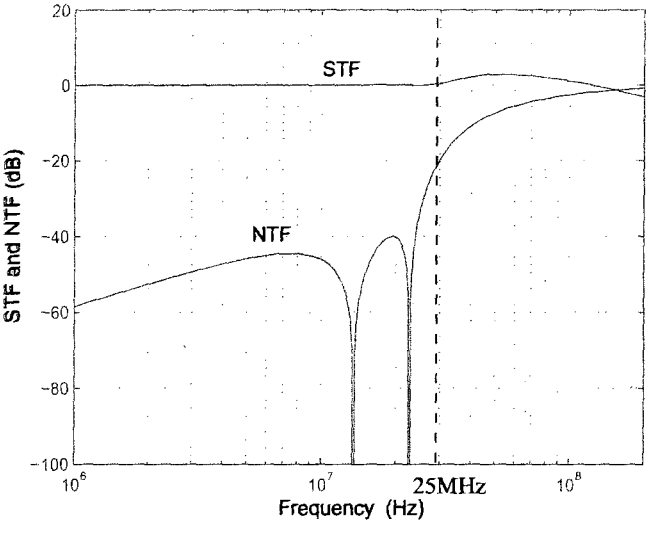


Figure 3.17: STF and NTF of the proposed ΣΔ modulator.

Table 3.6: Coefficient Values of the Proposed ΣΔ Modulator

k_1	1.2	d_1	1	g_1	0.176
k_2	0.6	d_2	0.656	g_2	0.875
k_3	0.3	d_3	0.443	k_{DAC_A}	1
k_4	0.16	d_4	0.45	k_{DAC_B}	0.6
k_5	0.08	d_5	0.302	d_0	1.25

k_{DAC_A} and k_{DAC_B} are the gain of DAC_A and DAC_B, respectively.

3.3 Summary

This chapter has examined the system-level design issues of wideband low-power continuous-time ΣΔ modulators. Modulator architectures that have been successfully used in building wideband (10MHz+) CT ΣΔ modulators were compared. It was shown that single stage multi-bit architecture is best suited for low-power high-performance applications. A system-level design flow along with an improved direct design method were presented which speed up design process. Two general filter topologies including feed-forward and feedback topologies were compared in terms of performance and power consumption. It was proven that feed-forward one has better power consumption and is more compatible with 90nm CMOS implementation. Finally, a fifth-order 4-bit CT modulator was proposed. The target of the modulator was set to have the highest signal bandwidth ($25MHz$) with lowest power consumption ($< 20mW$) and high resolution ($12bit$).

Chapter 4

Circuit Level Design and Implementation

This chapter describes the circuit-level design and implementation of the fifth-order CT $\Sigma\Delta$ modulator proposed in Chapter 3. The objective of this design is to demonstrate the feasibility of implementing a wideband CT $\Sigma\Delta$ modulator in nanometer CMOS technology with very low power consumption.

The most important circuit block in this design is the loop filter. It consumes the most power and may degrades the overall system performance if it is not designed carefully. As can be seen in Figure 3.14, integrators of the loop filter have different design requirements. The first integrator of the loop filter has the most stringent design requirements because any noise and/or distortion added at this stage are not subject to noise shaping. Active-RC integrator is required for the first stage. Progressively relaxed circuit requirements along the integrator chain allow us to use different types integrators such as G_m-C instead of active-RC to save power without degrading the overall performance. Since the loop filter coefficients are implemented using the absolute value of RC, large process variation will cause large RC variation which subsequently degrades the system performance. On-chip automatic RC tuning is necessary to minimize the impact.

Another design concern is the speed of the internal quantizer. Since the excess loop delay degrades the performance or even causes the system instability, minimum-sized transistors

are used in the flash quantizer to minimize the excess loop delay. However process mismatch causes large DC offset in the quantizer which has to be compensated. In this work, digital-to-analog (DAC) trimming technique is used to calibrate the quantizer.

The experimental modulator is implemented in a 90nm single-poly seven-metal CMOS technology. It operates at a clock frequency of 800MHz with a supply voltage of 1.0V. The input signals have full scale differential range of $0.96V_{pp}$. Figure 4.1 shows the circuit diagram of the modulator. The implementation of this modulator involves the circuit design of the loop filter with on-chip RC constant tuning, 4-bit flash quantizer with DAC trimming, and current-steering DACs.

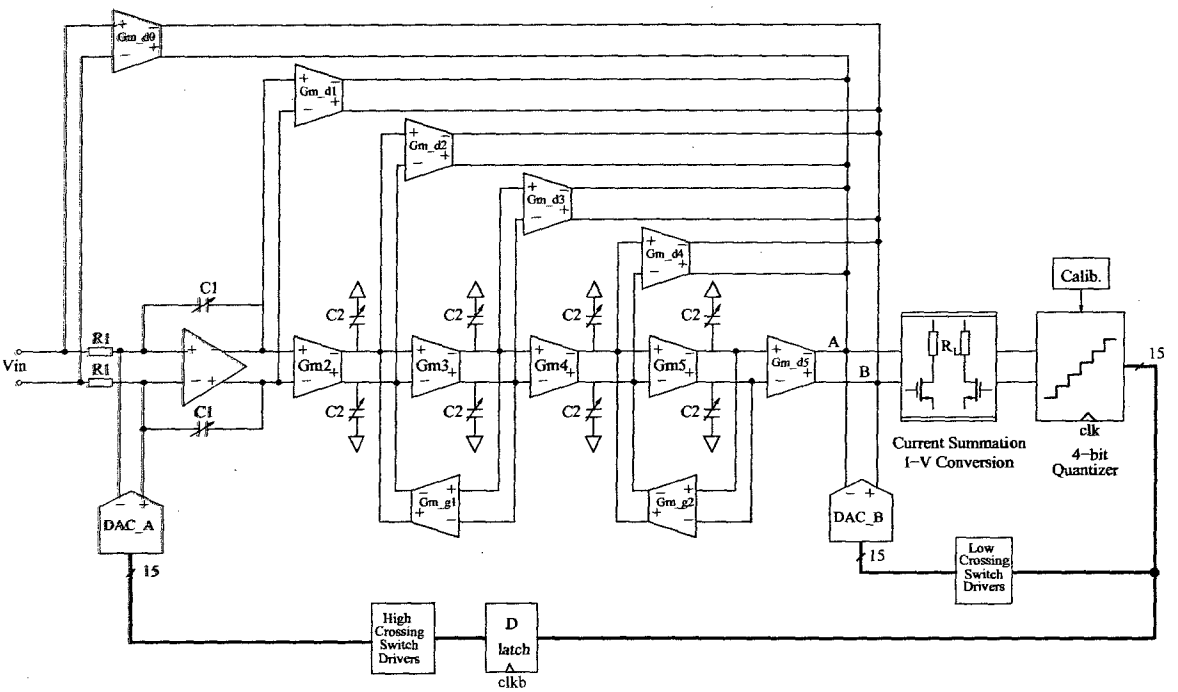


Figure 4.1: Circuit diagram of the proposed $\Sigma\Delta$ modulator.

4.1 Loop Filter

An active-RC integrator is chosen for the first stage of the fifth-order loop filter due to its high linearity and ease interface with feedback current-steering DAC. The second-, third-, fourth-, and fifth-stage integrators are G_m-C type for relaxed linearity requirements and to save power. The circuit parameters of the loop filter are listed in Table 4.1

Table 4.1: Loop Filter Circuit Parameters

R_1	480Ω	G_{m_d1}	$333.3\mu S$	G_{m_g1}	$84.5\mu S$
G_{m1}	$480\mu S$	G_{m_d2}	$218.8\mu S$	G_{m_g2}	$112\mu S$
G_{m2}	$240\mu S$	G_{m_d3}	$147.6\mu S$	G_{m_d0}	$416.7\mu S$
G_{m3}	$128\mu S$	G_{m_d4}	$150\mu S$	C_1	$2.17pF$
G_{m4}	$64\mu S$	G_{m_d5}	$100.7\mu S$	C_2	$1.0pF$

4.1.1 The First-Stage Integrator

The overall circuit structure of the first-stage integrator is shown in Figure 4.2. Common-mode feedback (CMFB) circuit is required to maintain the output common-mode voltage. The feedback current-steering DAC_A injects differential output current to the virtual ground inputs of the integrator.

Compensation for Finite Op-Amp GBW

The op-amp is a crucial component in an active-RC integrator. If we assume the op-amp is ideal (having infinite gain-bandwidth-product (GBW)) , the implemented integrator has an ideal transfer function of

$$INT(s) = \frac{V_o}{V_i} = -\frac{1}{sR_1C_1} \tag{4.1}$$

where R_1C_1 is the integrator time constant. However, a realizable op-amp does not have infinite GBW. Assuming the transfer function of a real op-amp is $A(s)$, which can be

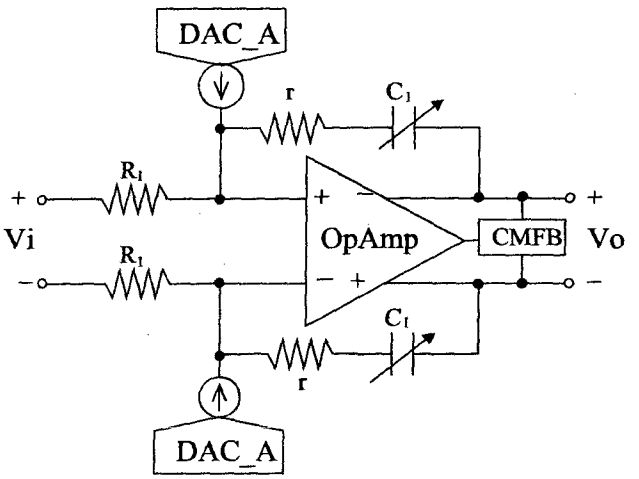


Figure 4.2: Overall circuit structure of the first-stage integrator.

approximated [59] as

$$A(s) \approx \frac{\omega_t}{s} \tag{4.2}$$

where ω_t is the unity GBW of the real op-amp. The actual implemented integrator has the transfer function of

$$\begin{aligned} INT(s) &= -\frac{1}{s \cdot R_1 C_1} \cdot \frac{1}{1 + (1 + 1/(sR_1C_1))/A(s)} \\ &\approx -\frac{1}{sR_1C_1} \cdot \frac{1}{1 + s/\omega_t} \end{aligned} \tag{4.3}$$

As it can be seen in (4.3), a parasitic pole $s = -\omega_t$ is introduced to the integrator transfer function. Assuming the non-ideal op-amp has unity GBW of 800MHz, the frequency responses of an ideal integrator vs non-ideal integrator are plotted in Figure 4.3. From the magnitude response, we see that finite GBW reduces the gain of the integrator at high frequency. From the phase response, it is observed that non-ideal op-amp introduces extra phase shift, which translates to extra time delay that is added to the modulator. The impact of non-ideal op-amp on overall modulator performance was studied in [60]. It was shown that non-ideal integrators due to finite op-amp GBW not only reduce the loop filter passband gain but also shift the loop filter poles away from their optimal locations. As a result, noise shaping ability of the $\Sigma\Delta$ modulator is reduced significantly.

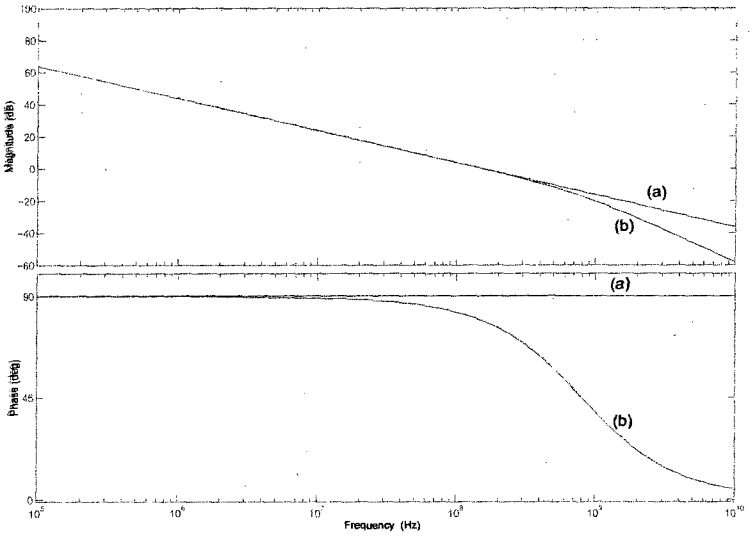


Figure 4.3: Frequency response of (a) ideal (b) non-ideal active-RC integrator.

To remedy the problem and design a better integrator, we create a zero at $s = -\omega_t$ to cancel the parasitic pole at $s = -\omega_t$. The compensation resistors r are employed as shown in Figure 4.2. This gives

$$\begin{aligned} INT(s) &= \frac{V_o}{V_i} = -\frac{1+srC}{sR_1C_1} \cdot \frac{1}{1+s/\omega_t+(1+srC_1)/(\omega_t R_1 C_1)} \\ &= -\frac{1}{sR_1C_1} \cdot \frac{1+srC_1}{1+1/(\omega_t R_1 C_1)+s(1+r/R_1)/\omega_t} \end{aligned} \tag{4.4}$$

This expression shows that pole-zero cancellation occurs when the compensation resistor is

$$r = \frac{1}{\omega_t C_1} \tag{4.5}$$

which results in :

$$INT(s) = \frac{V_o}{V_i} \approx -\frac{1}{SR_1C_1} \tag{4.6}$$

Thus a better active-RC integrator is achieved through small resistors r in series with the integrating capacitor C_1.

Op-Amp Design

The integrator following the first-stage is G_m-C type, which has extremely high input impedance. Hence the amplifier of the first-stage integrator does not need to drive a pure resistive load. Single-stage amplifier can be used for fast operation and low power consumption.

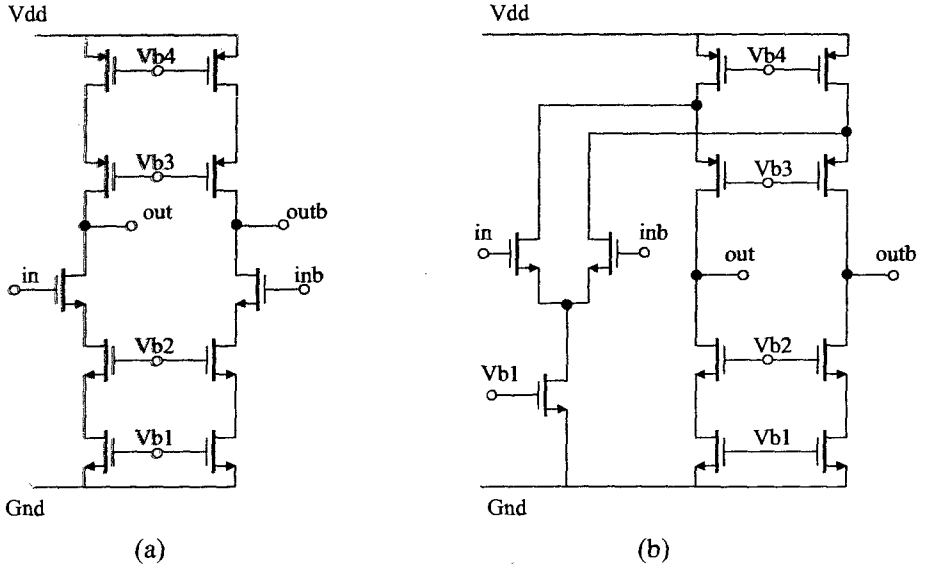


Figure 4.4: (a) Telescopic-cascode and (b) folded-cascode single-stage op-amp.

There are two types of single-stage amplifiers, including telescopic-cascode topology and folded-cascode topology [61], as shown in Figure 4.4. The telescopic one has two current branches, whereas folded one has four current branches. Compared to the telescopic one, the folded one consumes twice as much power. However, for the folded one, the input and output common-mode levels are decoupled from one another and can be set independently. Moreover, the folded amplifier uses less voltage headroom and hence has larger output signal swing, which outweighs its drawbacks especially in the low voltage implementation such as nanometer CMOS. For these reasons the folded-cascode topology is used in this work.

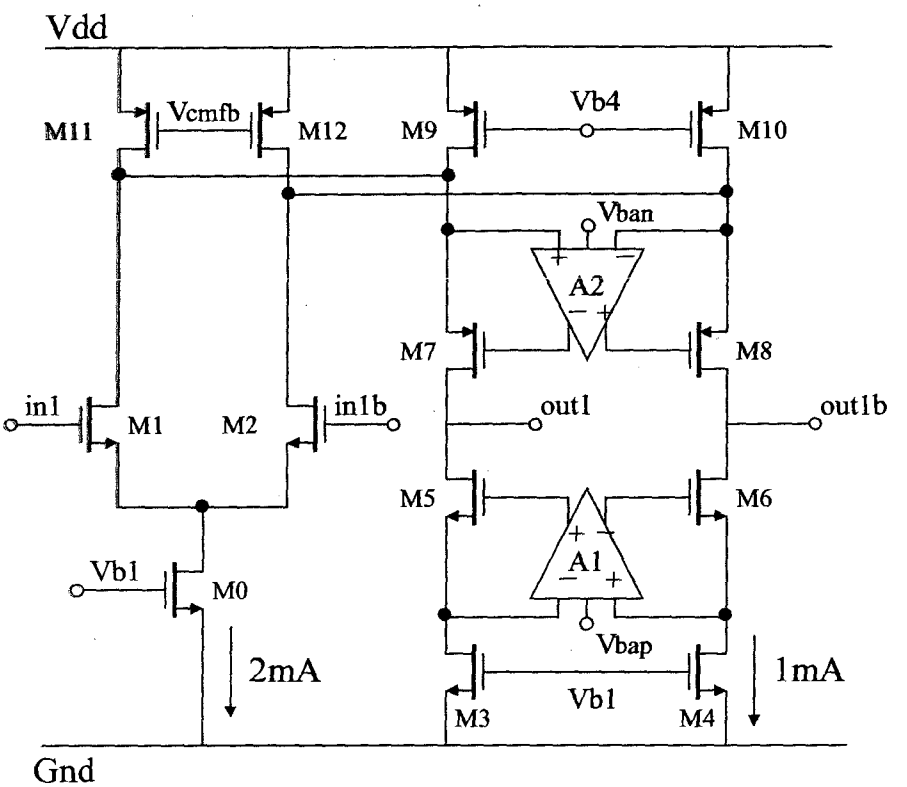
The fully differential folded-cascode operational amplifier for the first-stage integrator is shown in Figure 4.5. For a single-stage amplifier in 90nm CMOS technology, the DC gain can hardly exceed 40dB. To achieve over 60dB gain, two gain-boosting auxiliary amplifiers $A1$ and $A2$ are used to increase the gain without compromising signal swing and GBW of the original amplifier [61, 62]. These boosting amplifiers $A1$ and $A2$ are also fully differential and have folded-cascode configuration. The difference of these two is the transistor type of a differential input pair. $A1$ has N-type and $A2$ has P-type input stage as shown in Figure 4.6 and Figure 4.7. An additional transistor M_3 is used to set the common mode voltages for $A1$ and $A2$.

The common-mode feedback (CMFB) circuit is required for the fully differential folded-cascode main amplifier to set up the common mode output voltage. The CMFB schematic is shown in Figure 4.8. The two differential pairs M3-M4 and M5-M6 sense the amplifier output common-mode voltages, compare them with the desired output common-mode voltage V_{cm}, and generate the proper control voltage V_{cmfb}. When the common mode output voltage of the amplifier is too high, the control voltage V_{cmfb} goes up. Then, it brings up the gate voltage of M_{11} and M_{12} decreasing the common mode output voltage back to the required V_{cm}. V_{cm} is set to be 0.5 V in this design. The CMFB circuit has DC gain of 3dB, 142 MHz unity gain bandwidth with better than 60 degrees of phase margin, which ensures a stable common-mode output voltage. The CMFB circuits for the remaining integrators are similar to that of the first stage. They control NMOS current sources instead of PMOS current source for better phase margin.

The simulation results show that the gain-enhanced folded-cascode op-amp (Figure 4.5) achieves a DC gain of 78.8 dB, a phase margin of 52.6°, an unity-gain bandwidth of 745 MHz with load of $C_1 = 2.17pF$ on each output. Simulation results are shown in Figure 4.9.

Circuit Noise Consideration

The first stage of the loop filter has the most stringent noise requirement because the noise is directly added to the signal without any attenuation. The design of this stage is mainly concerned with noise requirements instead of power consumption. There are two



Transistor	W/L(μm)	Transistor	W/L (μm)
M0	250/0.4	M7,M8	245/0.2
M1,M2	80/0.2	M9,M10	960/0.4
M3,M4	118/0.4	M11,M12	176/0.4
M5,M6	51/0.2		

Figure 4.5: The gain-boosted folded-cascode op-amp for the first-stage integrator.

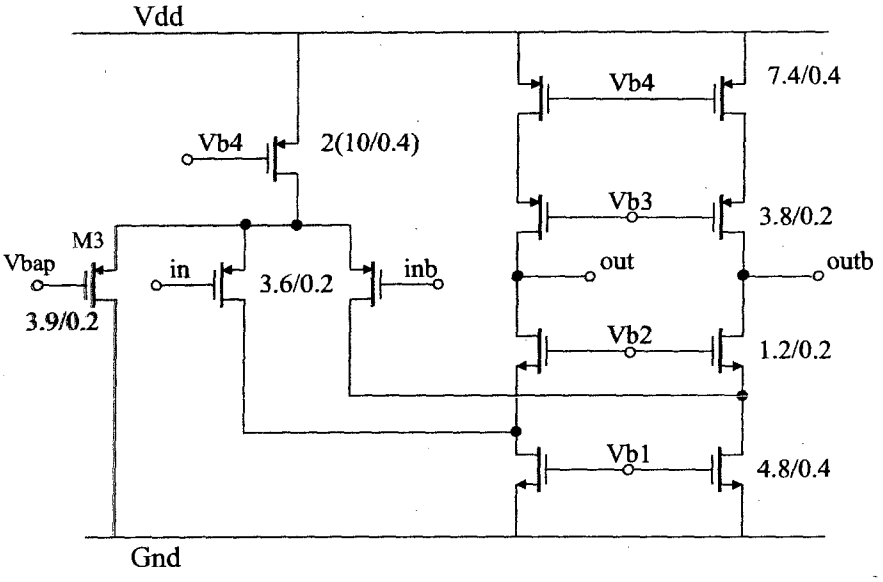


Figure 4.6: P-type gain-boosting auxiliary amplifier A1.

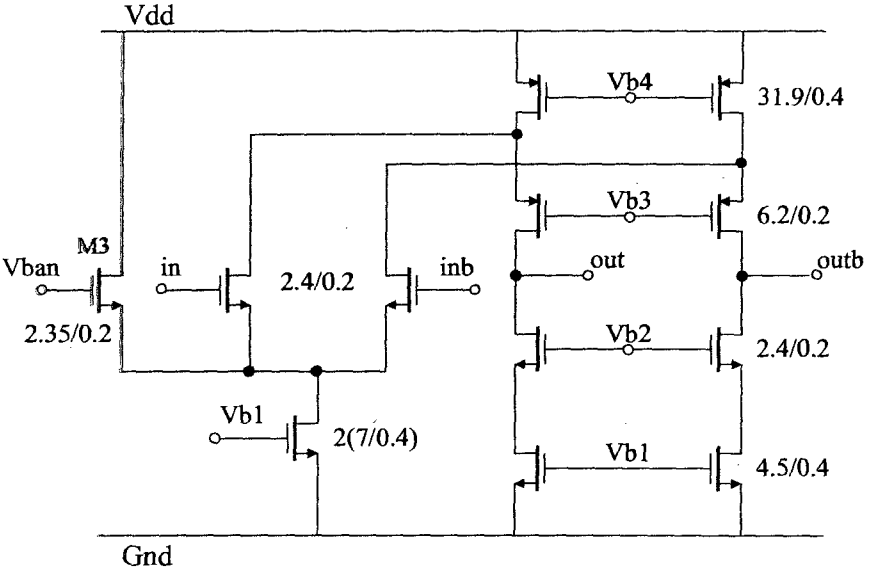


Figure 4.7: N-type gain-boosting auxiliary amplifier A2.

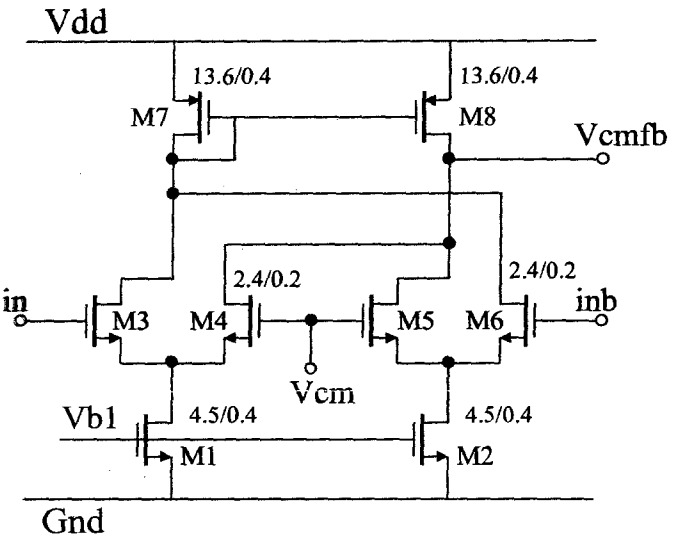


Figure 4.8: CMFB circuit for the folded-cascode op-amp.

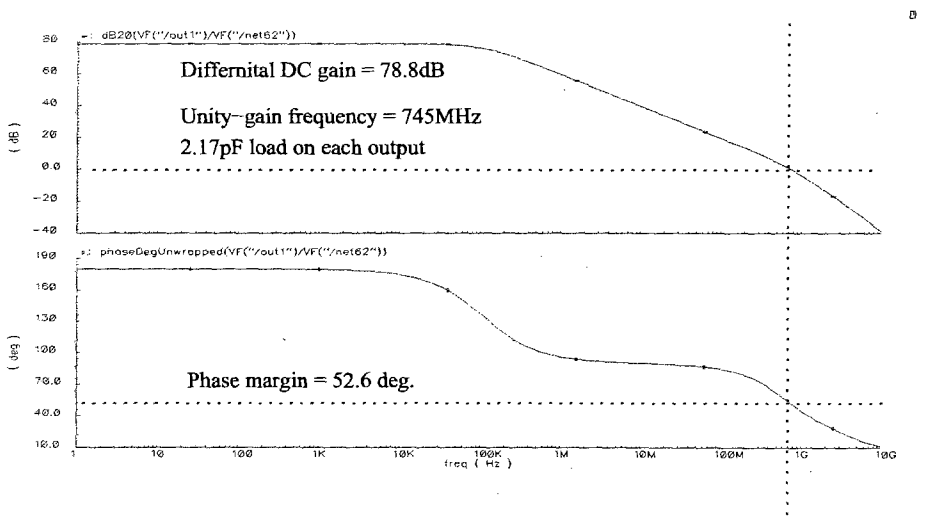


Figure 4.9: Simulated frequency response of the folded-cascode op-amp with 2.17pF load on each output.

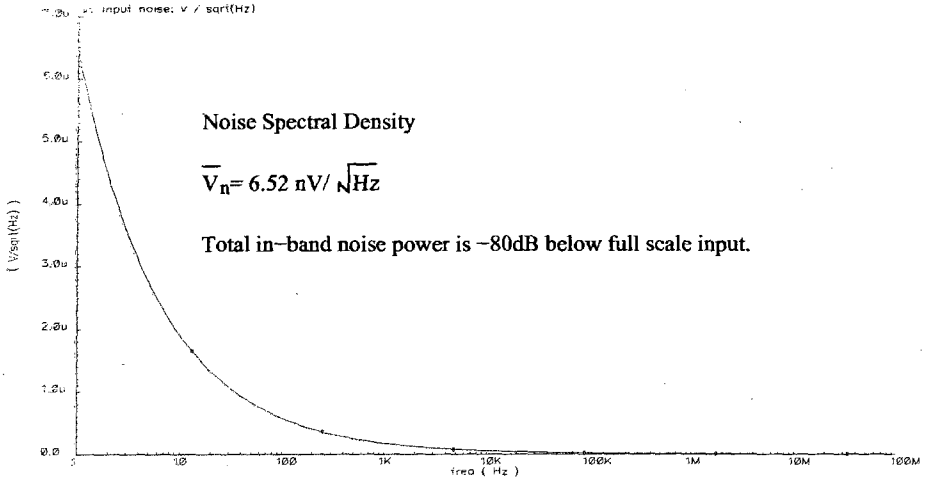


Figure 4.10: Simulated noise spectral density of the first-stage integrator.

noise sources at this stage including input resistors R_1 and the operational amplifier. The in-band noise generated by the two input resistors R_1 is:

$$\overline{v_{R_1}^2} = 8kTR_1 \quad (V^2/Hz) \tag{4.7}$$

where k is Boltzmann's constant with a value of $1.38 \times 10^{-23} J/K$, T is the absolute temperature. In this design we chose $R_1 = 480\Omega$.

In the amplifier shown in Figure 4.5, the differential input-referred thermal noise is given by

$$\overline{v_{n,thermal}^2} \approx 8kT \cdot \gamma \cdot \frac{1}{g_{m1}}(1 + \frac{g_{m3} + g_{m9} + g_{m11}}{g_{m1}}) \quad (V^2/Hz) \tag{4.8}$$

where γ is thermal noise coefficient, and g_{m1}, g_{m3}, g_{m9}, g_{m11} are the transconductances of transistors M1, M3, M9, and M11, respectively.

The input-referred flicker noise of the amplifier can be expressed as

$$\begin{aligned} \overline{v_{n,flicker}^2} \approx & \left(\frac{K_N}{C_{ox}(WL)_{M1}} + \frac{g_{m3}^2}{g_{m1}^2}\frac{K_N}{C_{ox}(WL)_{M3}} + \frac{g_{m9}^2}{g_{m1}^2}\frac{K_P}{C_{ox}(WL)_{M9}}\right. \\ & \left. + \frac{g_{m11}^2}{g_{m1}^2}\frac{K_P}{C_{ox}(WL)_{M11}}\right) \cdot \frac{1}{f} \quad (V^2/Hz) \end{aligned} \tag{4.9}$$

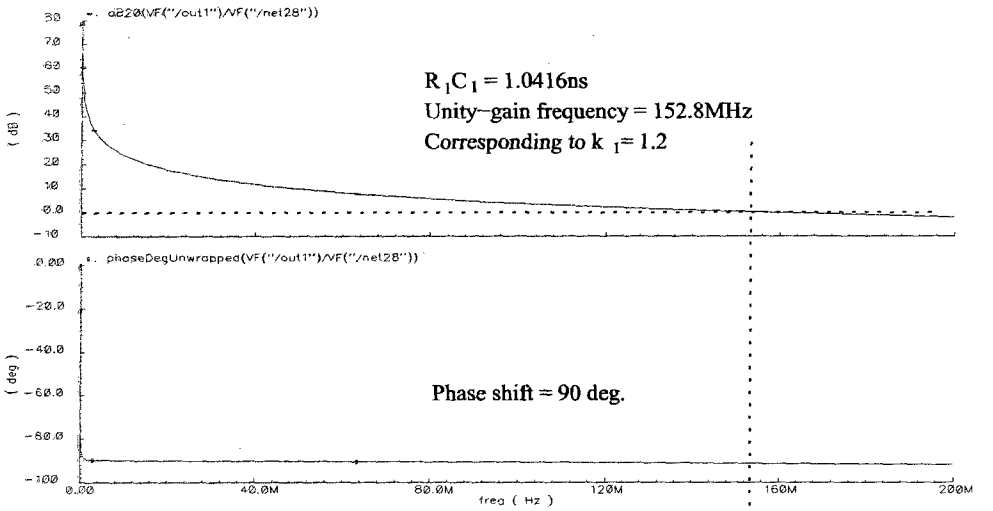
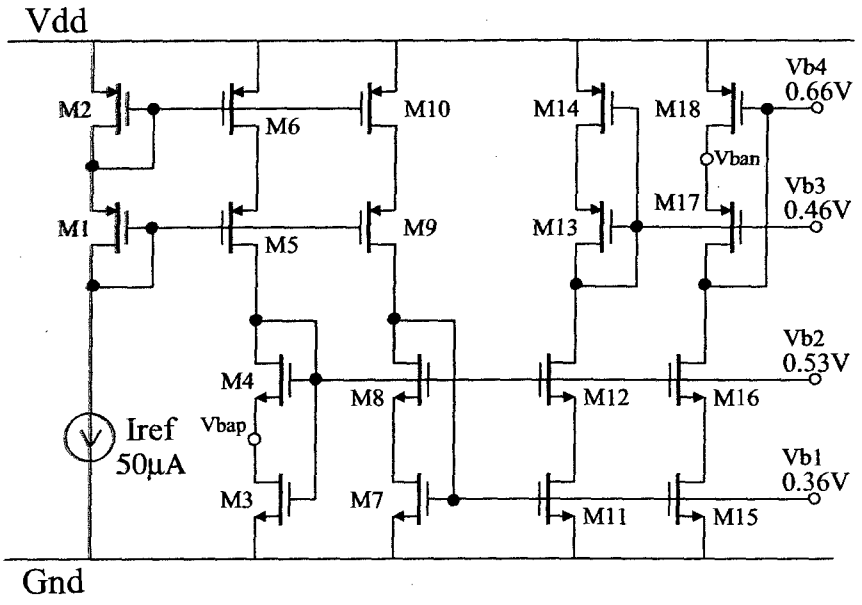


Figure 4.11: Simulated frequency response of the first-stage integrator.

where K_N and K_P are the flicker noise coefficient of NMOS and PMOS transistors. It is clear that g_{m1} should be maximized and g_{m3}, g_{m9}, g_{m11} minimized to reduce the noise contribution from input transistor M1 and current source transistors M3, M9, and M11. Based on simulations, the input-referred noise (thermal and flicker) spectral density of the first integrator is $6.52nV/\sqrt{Hz}$, $-80dB$ lower than the full scale input signal power. Simulated noise spectral density of the first-stage integrator is shown in Figure 4.10. The simulated frequency response of the first-stage integrator is shown in Figure 4.11.

Bias Circuit

The bias circuit for the main and auxiliary amplifiers is shown in Fig.4.12. The transistors in the amplifiers are biased so that their drain-source voltage is greater than their gate-source overdrive voltage to insure that the transistors operate in the saturation region and thus maintaining a high output resistance. Low-voltage cascode current mirrors are used to bias the gates of the NMOS and PMOS current source M3-M4 and M9-M10 to 0.36V and 0.66V respectively. The cascode transistor M5-M6 and M7-M8 are biased to 0.53V and



Transistor	W/L(μm)	Transistor	W/L(μm)
M1,M5,M9	26/0.2	M7,M11,M15	8/0.4
M2,M6,M10	40/0.4	M13,M17	12/0.2
M3	2/0.4	M14	4.6/0.4
M4,M8,M12,M16	4/0.2	M18	26/0.4

Figure 4.12: Bias circuit for integrators.

0.46V. This is a compromise that ensures the transistors remaining in saturation region during normal operation while allowing for a relatively large output signal swing. In order to reduce layout complexity, but at the expense of increased power dissipation, this loop filter contains five independent biasing circuits, one for each integrator.

4.1.2 The Second- to Fifth-Stage Integrators

The following four stages are implemented using G_m-C integrators for fast operation and power saving. The overall circuit structure of the G_m-C integrators is shown in Figure 4.13.

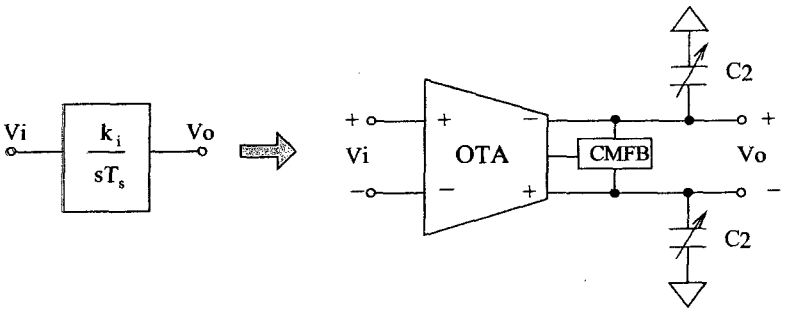


Figure 4.13: Circuit structure of a G_m-C integrator.

The transfer function of the integrator is

$$\frac{V_o}{V_i} = -\frac{k_i}{sT_s} = -\frac{G_m}{sC_2} \tag{4.10}$$

where k_i is the desired gain of the integrator, T_s is the modulator sampling clock rate, G_m is the transconductance of the operational transconductance amplifier (OTA), and C_2 is the integration capacitor. The required G_m is calculated using

$$G_m = \frac{k_i}{T_s} \cdot C_2 \tag{4.11}$$

The linearity and noise requirements on these integrators are progressively relaxed along the integrator chain. The noise transfer functions of the internal nodes are redrawn here in Figure 4.14. Any noise added at second integrator is suppressed by the noise transfer function NTF2, and noise added at the third stage is suppressed by NTF3, and so on. As can be seen in Figure 4.14, noise and nonlinearity of the second stage are only suppressed with the first-stage gain by around 16dB at 25MHz. Care should be taken to ensure that the second-stage integrator does not degrade the performance of the overall modulator.

Due to the open-loop operation, harmonic distortion becomes the dominant noise source in G_m-C integrators. Therefore, the main design concern is to improve the linearity of the integrators. The schematic of the second-stage G_m-C integrator is shown in Figure 4.15. For good linearity, a gain boosted folded-cascode OTA with resistive source degeneration is adopted. PMOS transistors are used at input for less body modulation effect.

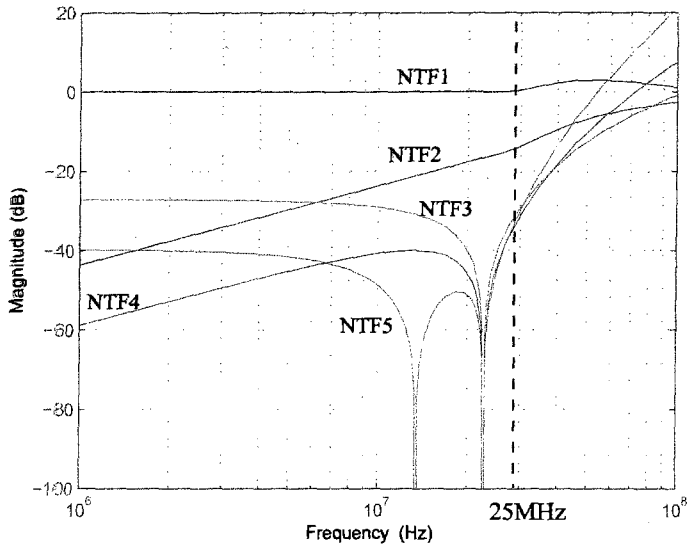


Figure 4.14: Internal noise transfer functions of the proposed ΣΔ modulator.

To further improve the linearity, two input driving amplifiers A_{01} and A_{02} are connected at the inputs. The transconductance of the OTA can be expressed as [63]

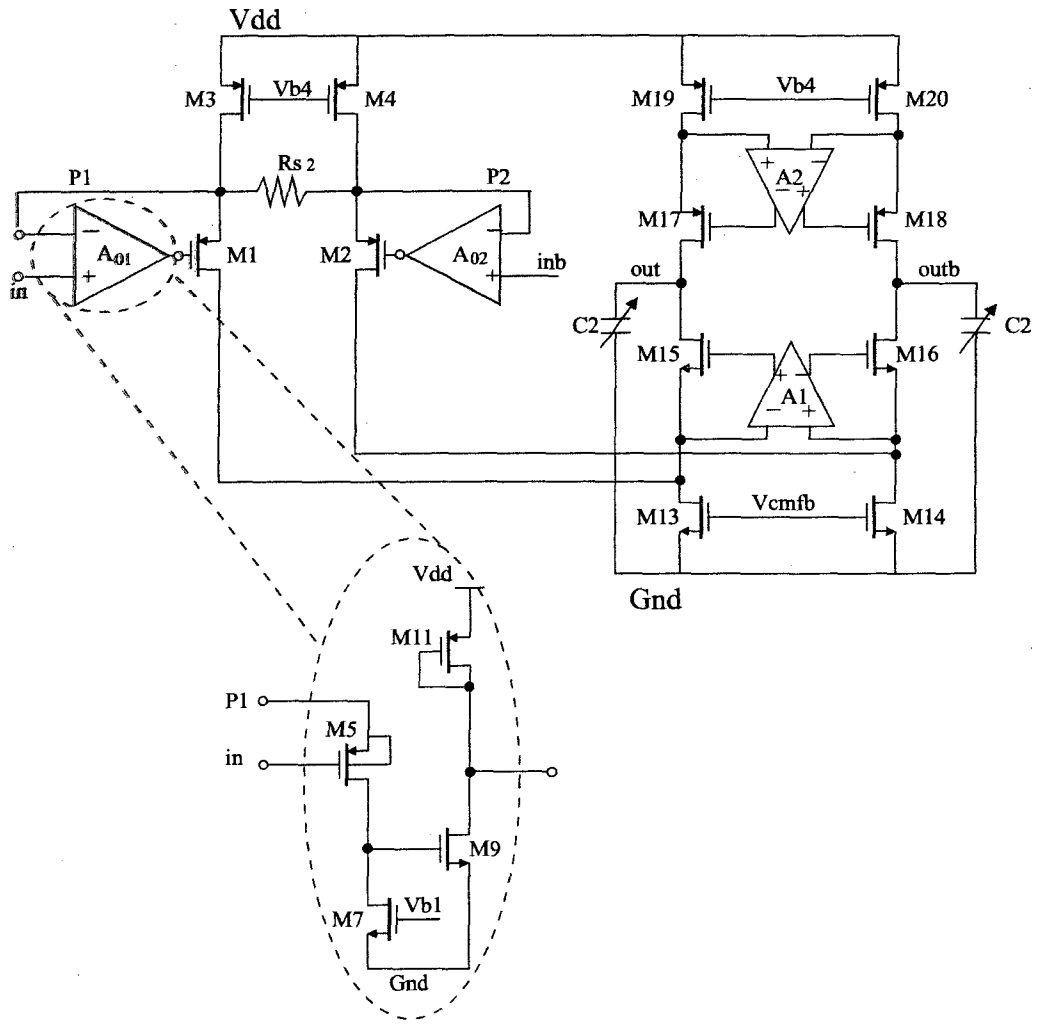
$$G_m \approx \frac{A \cdot g_{m1}}{1 + A \cdot g_{m1} \cdot R_s} \tag{4.12}$$

where A is the gain of the input driving amplifiers A_{01} and A_{02}, g_{m1} is the transconductance of the input transistors M1 and M2, R_s is the source degeneration resistor. And the third-order harmonic distortion HD_3 of the circuit can be expressed as [64]:

$$HD_3 = \frac{1}{32}\left(\frac{1}{1 + A \cdot g_{m1} R_s}\right)^2 \left(\frac{v_i}{V_{GS} - V_{th}}\right)^2 \tag{4.13}$$

where $(V_{GS} - V_{th})$ is the overdrive voltage of M1 and M2, v_i is the differential input voltage as shown in Fig. 4.15. In this work, the gain of A_{01} and A_{02} is made large enough to significantly suppress distortion. The simulated frequency response of the second integrator is shown in Figure 4.16.

The third- to fifth- integrators have the same circuit structure as the second one. Due to the different transconductance requirements, lower bias currents and larger source de-



Transistor	W/L(μm)	Transistor	W/L(μm)
M1-M2	95/0.2	M11	1.37/0.4
M3-M4	180/0.4	M13-M14	80/0.4
M5	2/0.2	M15-M16	20/0.2
M7	0.5/0.4	M17-M18	70/0.2
M9	1/0.2	M19-M20	180/0.4

Figure 4.15: Schematic of the second-stage G_m-C integrator.

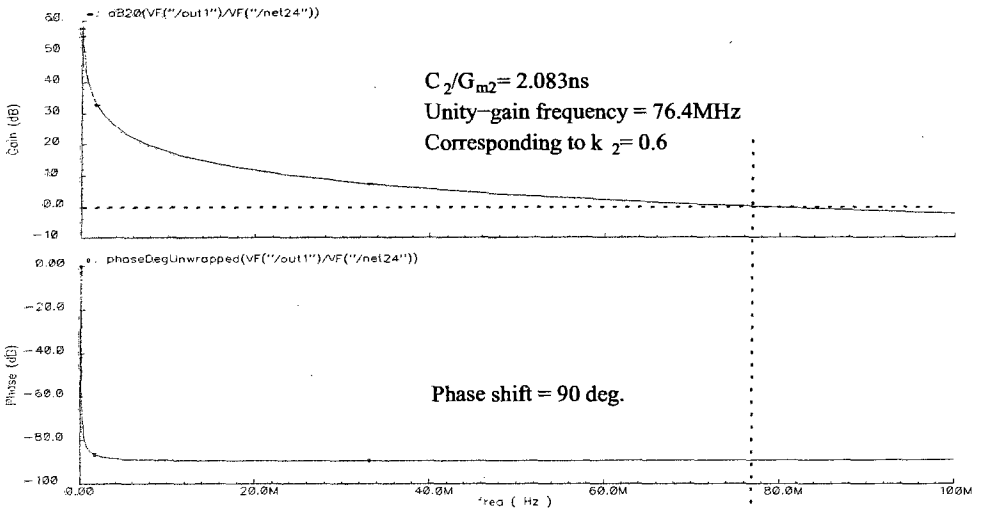


Figure 4.16: Simulated frequency response of the second-stage integrator.

generation resistors are used in these integrators. Circuit parameters of the five integrators of Figure ?? are listed in the following table.

Table 4.2: Summary of Circuit Parameters of Integrators

	R	G_m	C	I_{bias} per branch
1^{st} Integ.	$R_1 = 480\Omega$	N/A	C_1=2.17pF	$1mA$
2^{nd} Integ.	$R_{s1} = 4.3k\Omega$	$G_{m2} = 480\mu S$	C_2=1pF	$350\mu A$
3^{rd} Integ.	$R_{s2} = 9.2k\Omega$	$G_{m3} = 240\mu S$	C_2=1pF	$150\mu A$
4^{th} Integ.	$R_{s2} = 19.4k\Omega$	$G_{m4} = 128\mu S$	C_2=1pF	$150\mu A$
5^{th} Integ.	$R_{s2} = 52.5k\Omega$	$G_{m5} = 64\mu S$	C_2=1pF	$75\mu A$

4.1.3 Local Feedback Paths

Local g_m feedback paths (g_1 and g_2 in Fig. 3.16) shift the poles of the loop filter to the optimal position. The circuit structure used to implement g_1 and g_2 is similar to the OTA

of the second-stage integrator. The transconductance of the two OTAs including G_{m_g1} and G_{m_g2} (shown in Figure 4.1) are calculated as follows:

$$G_{m\_g1} = \frac{k_2}{T_s} \cdot C_2 \cdot g_1 \tag{4.14}$$

$$G_{m\_g2} = \frac{k_4}{T_s} \cdot C_2 \cdot g_2 \tag{4.15}$$

where k_2 and k_4 are the gain of the second- and fourth-stage integrator, C_2 is the integrator capacitor. g_1 and g_2 are the desired local feedback gain. The first local feedback path forming a loop filter pole and its implementation is shown in Figure 4.17.

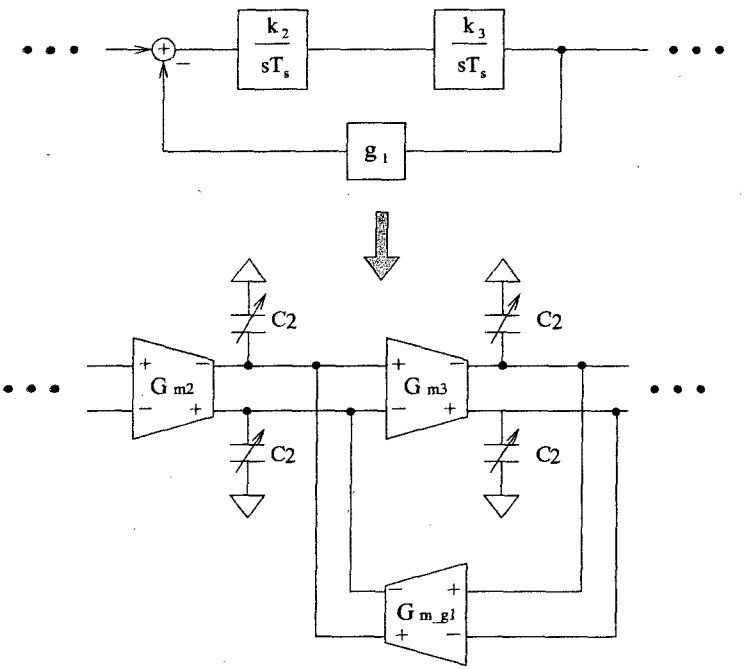


Figure 4.17: Local feedback path g_1 and its g_m implementation.

4.1.4 Feed-forward Paths and Current Summation

The current summation schematic is shown in Figure 4.18. The six transconductor gain stages convert the modulator input and five integrator outputs from voltage to current.

Again, input driving amplifiers A_{01} and A_{02} are used to improve the linearity of the gain stages. Currents from different branches together with the current generated by DAC_B are summed at nodes **A** and **B** and then converted back to voltage through two pull-up resistors R_L, which drive the 4-bit internal flash quantizer. In this design R_L is chosen to be $3k\Omega$. A gain-boosting amplifier (A1 in Figure 4.18) is used to increase the output impedance of the summation circuit.

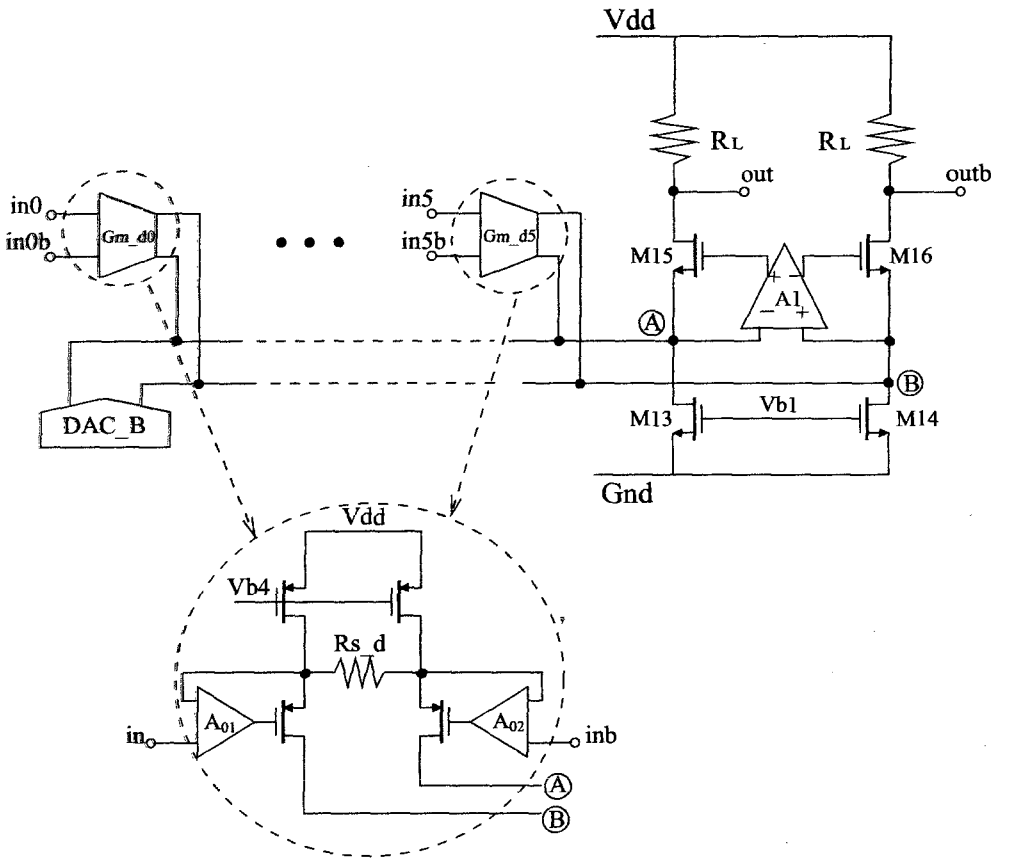


Figure 4.18: Transconductor current summation schematic.

The required transconductance for each feed-forward path is calculated using the following equation:

$$G_{m\_di} = \frac{d_i}{R_L} \tag{4.16}$$

where $i = 0, 1.., 5$, d_i is the required gain in i^{th} feed-forward path, and R_L is the pull-up resistor.

4.1.5 RC Time Constant Automatic Tuning

Large process variations in CMOS technology can result in large RC time constant uncertainty, which seriously degrades the system performance [32]. In this 90nm CMOS technology, measured data of p+ poly non-silicided resistance varies $\pm 13.6\%$ of its nominal value and metal-diaelectric-metal (MIM) capacitance varies $\pm 15\%$ of its nominal value, which result in RC product variation -26.6% to $+30.7\%$ of its nominal value [65]. However, simulation results reveal that the proposed modulator can only tolerate $\pm 5\%$ time constant variation to have less than 1.5dB SNDR variation. On-chip automatic RC tuning circuit is necessary.

In this design, a master-slave capacitor array tuning scheme is used to adjust the time constants [66]. Each integration capacitor in the loop filter is realized as a tunable capacitor with a 4-bit binary-weighted capacitor array as shown in Figure 4.19. The capacitor array is digitally controlled by a master RC tuning block. The maximum available capacitance in the array is

$$C_{max} = C_{Base} + 15C_{LSB} \tag{4.17}$$

The minimum available capacitance is

$$C_{min} = C_{Base} \tag{4.18}$$

Tuning accuracy is

$$p = \frac{C_{LSB}}{C_{Base} + 7C_{LSB}} \tag{4.19}$$

C_{Base} and C_{LSB} are chosen so that $C_{Base}+7C_{LSB}$ equals the nominal value of the integration capacitor with tuning accuracy of $\pm 5\%$. The achieved tuning range of the array is -35% to $+40\%$ which is sufficient for our design.

The digital switching code is provided by a master tuning block as shown in Figure 4.20. It has replicas of R and C used in the to-be-tuned-integrators. V_{ref1} is external reference

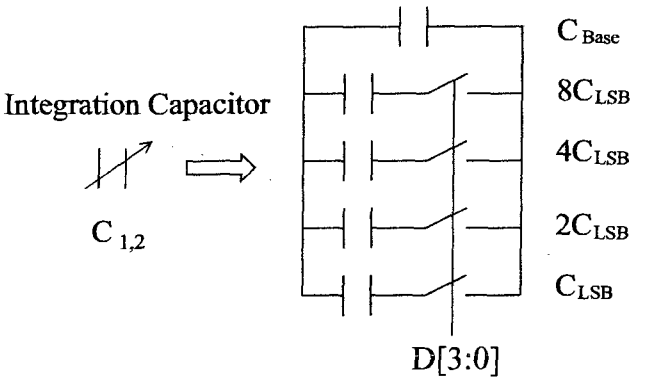


Figure 4.19: Tunable capacitor with a 4-bit binary-weighted capacitor array.

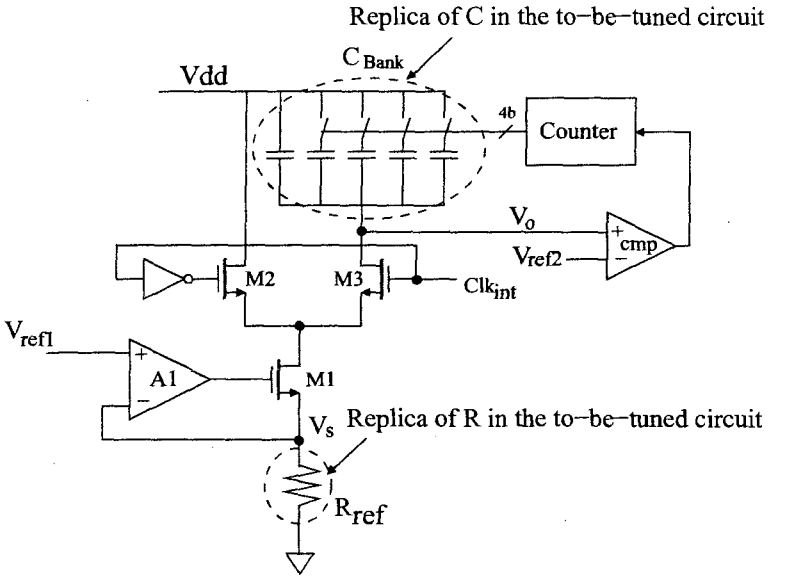


Figure 4.20: Simplified schematic of master RC tuning block.

voltage. High gain amplifier $A1$ keeps V_s equal to V_{ref1}. The output voltage V_o can be calculated using equation:

$$V_o = V_{dd} - \frac{V_{ref1} \cdot \Delta t}{R_{ref} \cdot C_{Bank}} \tag{4.20}$$

where Δt is the integration period controlled by clock signal Clk_{int}. V_{ref2} is set to be the value when the product of $R_{ref} \cdot C_{Bank}$ equals the desired value. V_o is compared to V_{ref2}. If V_o is smaller than V_{ref2}, switching code increments until V_o drops below V_{ref2}. If V_o is bigger than V_{ref2}, switching code decrements until V_o rises above V_{ref2}. After tuning procedure is done, the tuning circuitry is disabled to save power.

4.2 Internal 4-bit Quantizer with DAC Trimming

The block diagram of the 4-bit internal flash quantizer is shown in Figure 4.21. Signal *in* and *inb* is the differential input to the quantizer, which has 15 digital outputs $Q_0, Q_1, ...Q_{14}$. The quantizer consists of a resistor-based voltage reference ladder and fifteen identical clocked comparators. The resistor-based reference ladder has DC current of $200\mu A$. V_{ref+} is set 0.26V and V_{ref-} is 0.74V with total 480mV voltage swing. The resistor r is chosen as 150Ω so that the reference ladder has 30mV voltage increment.

As can be seen in Figure 4.21, each clocked comparator is composed of a preamplifier, a regenerative latch and a SR flip-flop. The block diagram, schematic, and transistor sizes of the preamplifier are shown in Figure 4.22. Preamplifier samples and amplifies the difference between the differential input signal and the differential reference voltage. A correct differential output is then generated and fed to the following regenerative latch. The input transistor pairs M2, M3, M4, and M5 of the preamplifier have the smallest sizes allowed by the technology to minimize the delay of the comparator. A cross-coupled load is used to form a strong positive feedback for fast operation. A *reset* signal is utilized to short the differential outputs after comparison phase for fast overdrive voltage recovery.

The schematic and transistor sizes of the regenerative latch and SR flip-flop are shown in Figure 4.23. The timing diagram of the clocked comparator is shown in Figure 4.24. When *reset* signal goes low, preamplifier samples and amplifies the voltage difference between the

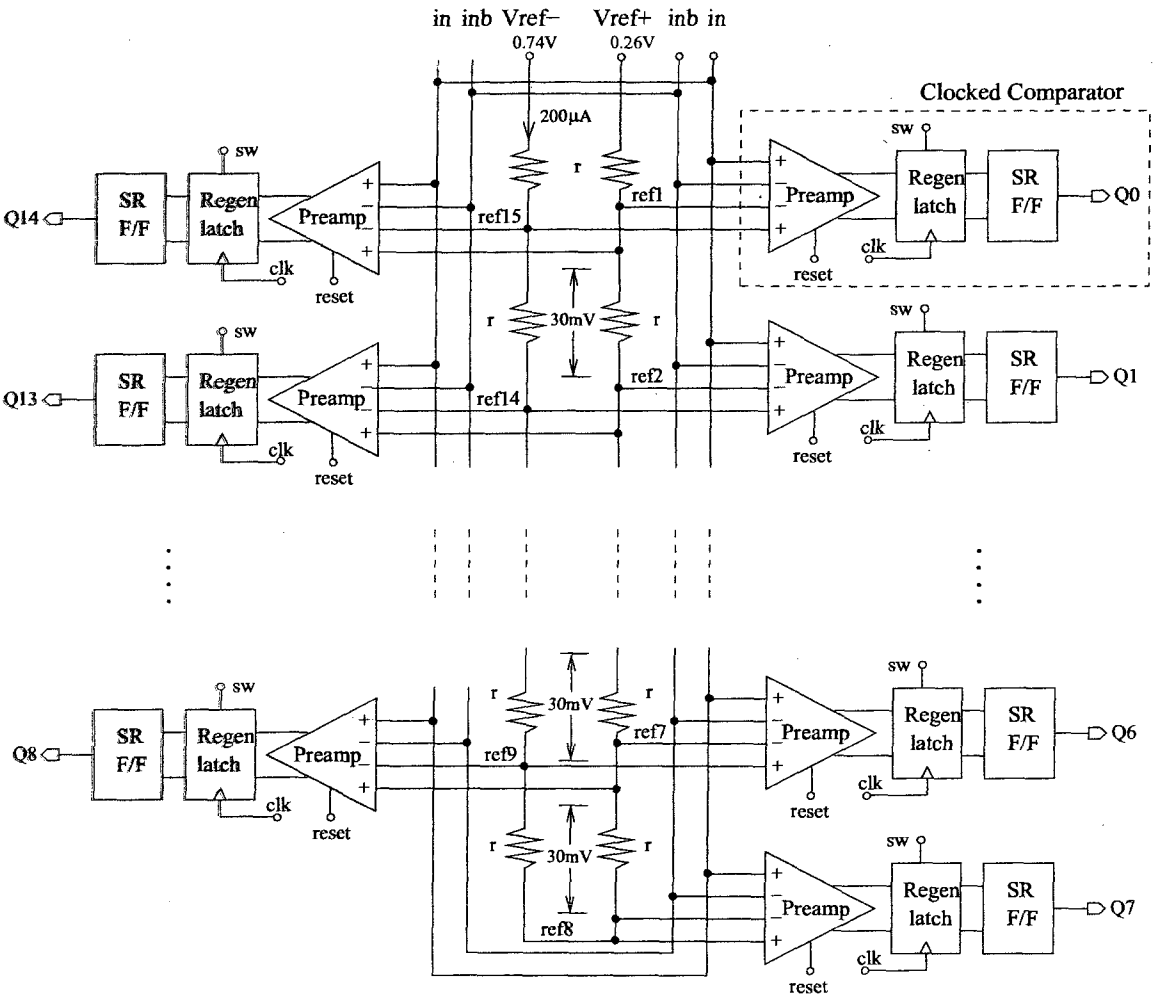
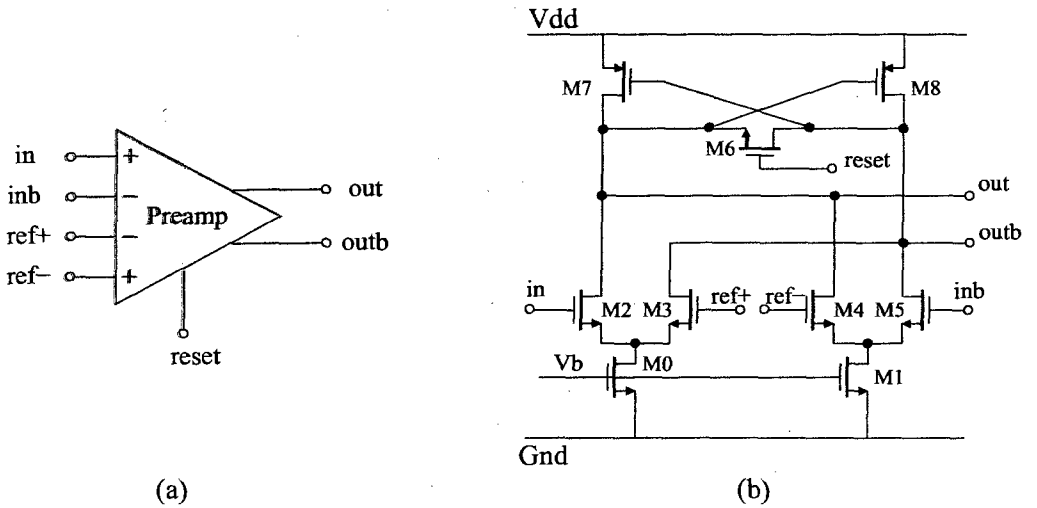


Figure 4.21: Block diagram of the internal 4-bit flash quantizer.

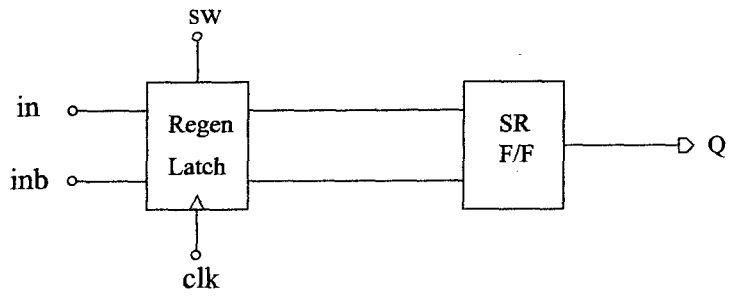


Transistor	W/L(μm)	Transistor	W/L(μm)
M0,M1	2/0.2	M7,M8	1.5/0.1
M2,M3,M4,M5	0.12/0.1	M6	3/0.1

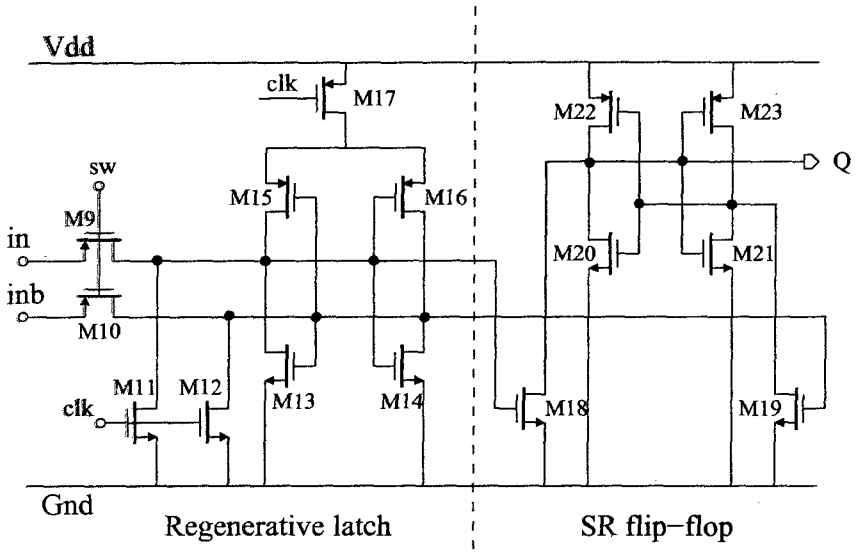
Figure 4.22: (a) Block digram and (b) schematic of the preamplifier.

input and the reference voltage. Shortly after it, Signal *clk* and signal *sw* are going low, output of the preamplifier is connected to the latch for regeneration. Signal *sw* goes high to disconnect the preamplifier before the output of the latch reaches full rail voltage to reduce kickback noise. When *reset* signal goes high, the preamplifier is shorted together at its output. Since the output of the latch maintains the final voltage less than half a clock period, the SR flip-flop is used to convert it to rail-to-rail value and sustain it for a full clock period.

Since minimum-sized input transistors are used in the preamplifiers for low latency, calibration is necessary to compensate the input device offsets. In this design a DAC trimming technique is used to correct offset error [67]. Monte Carlo simulation results show that the input-referred offset of the comparator has a standard deviation of 0.87LSB before calibration. A 8-level differential *DAC_trim* cell is designed with trimming accuracy of



(a)



(b)

Transistor	W/L(μm)	Transistor	W/L(μm)
M9,M10,M15,M16	0.36/0.1	M11,M12	0.3/0.1
M13,M14,M18,M19,M20,M21	0.12/0.1	M17	0.5/0.1
M22,M23	0.24/0.1		

Figure 4.23: (a) Block diagram and (b) schematic of regenerative latch and SR flip-flop.

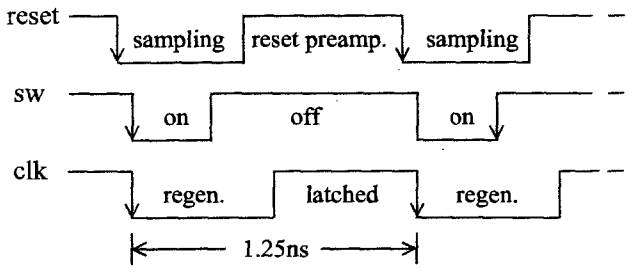


Figure 4.24: Timing diagram of the clocked comparator.

0.25LSB and trimming clock of 25MHz. The simplified circuit diagram of the cell is shown in Figure 4.25.

Timing diagram for the trimming process is shown in Figure 4.26. When *Trim* signal goes high, system enters trimming mode. Loop filter is disconnected from the quantizer. Both input and reference voltages to the preamplifier are connected to common mode voltage so that the digital output of the comparator is determined only by its offset. The trimming current *I_trim* generated by the *DAC_trim* cell is initially completely steered in one direction to generate an initial offset, The current is then incremented in 1-LSB *DAC_trim* steps in the other direction until the comparator output toggles. Since *I_trim* search is based on the comparator's digital output, this corrects the combined offsets of both preamplifier and regenerative latch. The process takes less than $1\mu s$ to complete and is simultaneously conducted on all 15 comparators at start-up.

The output of the quantizer is a 15-bit thermometer code. A fast encoder is needed to convert it to 4-bit binary code. In this work a fat tree TC-to-BC encoder is used because it can operate at very high speed [68]. The block diagram of the encoder is shown in Figure 4.27. The logic implementation of the encoder is shown in Figure 4.28.

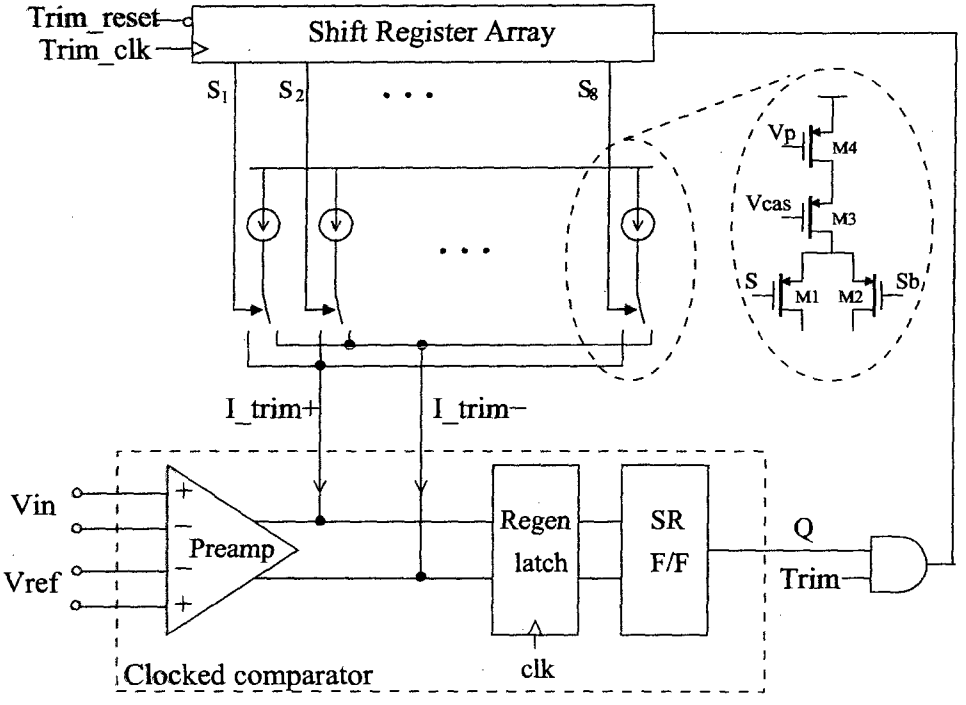


Figure 4.25: Schematic of DAC_trim cell for each comparator.

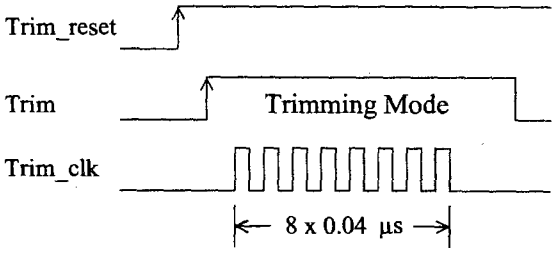


Figure 4.26: Timing digram for DAC trimming process.

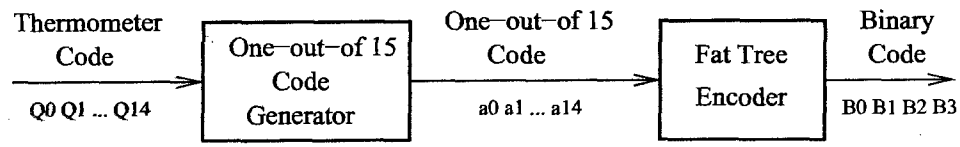


Figure 4.27: Block digram of the two-stage fat tree TC-to-BC encoder.

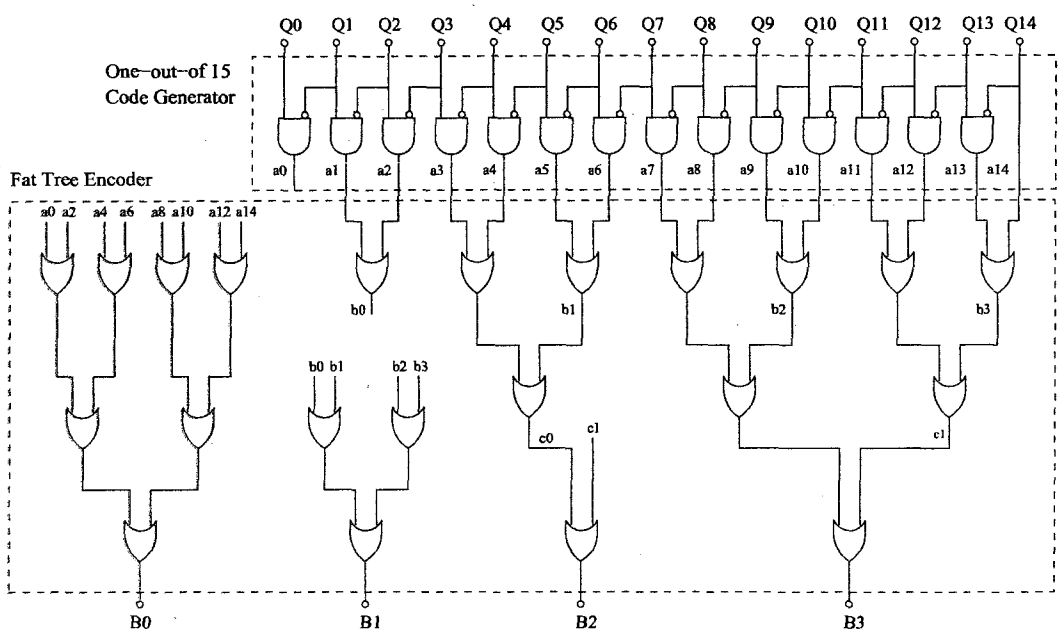


Figure 4.28: Logic implementation of the TC-to-BC encoder.

4.3 Feedback Current-Steering DACs

Two current-steering NRZ DACs are used in the system. DAC_A converts the digital output of the quantizer to analog signal and feeds it back to the input of the loop filter, as depicted in Figure 4.29. Transistors M_{61} and M_{62} are employed to generate a differential current output. Noise and linearity requirements on DAC_A have to exceed the overall performance of the modulator. DAC_A is designed to achieve 12-bit linearity. For a sufficient yield, the required current matching accuracy can be calculated using the formula given by Bosch *et*

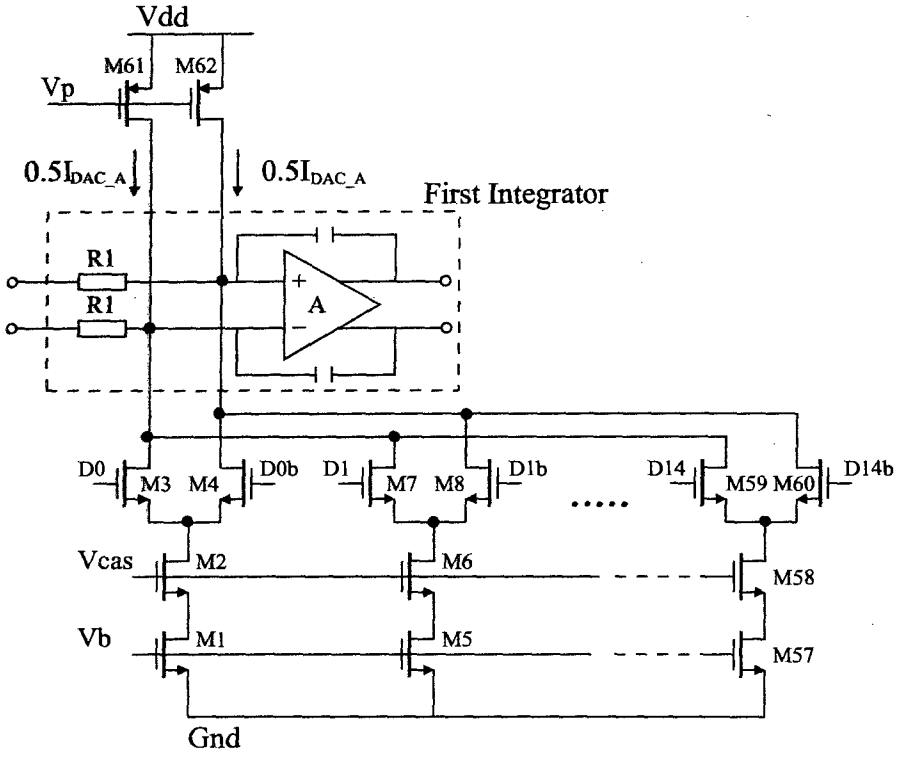


Figure 4.29: Schematic of DAC_A current cells and their interface to the loop filter.

al. in [69]:

$$\sigma(\frac{\Delta I}{I}) \leq \frac{1}{\sqrt{2^{12+2}} \times 1.3} = 0.6\% \tag{4.21}$$

Current source transistors ($M_{1,5,..,57}$) of DAC_A can accordingly be designed using Pelgrom model [70]:

$$0.6\% = \sqrt{\frac{A_\beta^2}{W \cdot L} + \frac{4A_{Vt}^2}{W \cdot L(V_{GS} - V_{th})}} \tag{4.22}$$

where A_β and A_{Vt} are the technology constants, W, L, and $(V_{GS} - V_{th})$ are the width, length, and overdrive voltage of $M_{1,5,..,57}$. In this design, the current source transistors have large overdrive voltages to guarantee the required current matching accuracy.

All the current source transistors are cascoded to increase the output impedance. Current switch transistors $M_{3,4}$, $M_{7,8}$ ... $M_{59,60}$ are always operate in saturation region to provide an additional level of cascoding to further improve output impedance. The lower

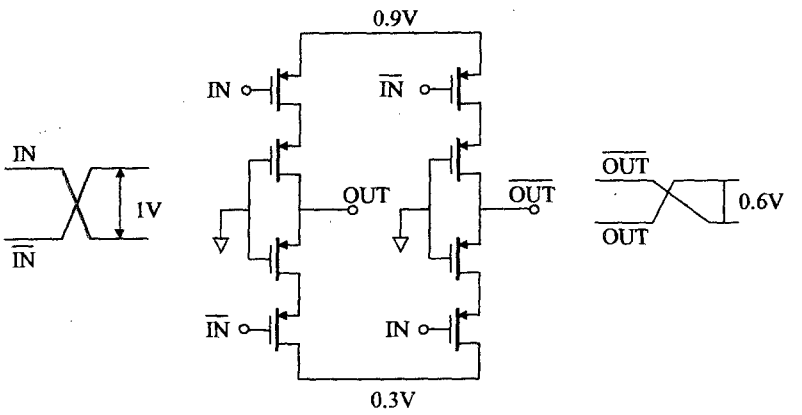


Figure 4.30: High-crossing low-swing switch driver.

bound of DAC_A current I_{DAC_A} for sufficient low noise can be estimated using the equation described in [32].

$$I_{DAC} = \frac{32kT\gamma \cdot SNR_{DAC} \cdot \Delta f}{(V_{GS} - V_{th})} \tag{4.23}$$

where $(V_{GS} - V_{th})$ is the overdrive voltage of the NMOS current source transistor, Δf is the signal bandwidth, and SNR_{DAC} is the required SNR for DAC_A. In this design $I_{DAC\_A} = 1mA$ is used. To prevent clock feed-through and charge injection through switch transistors, high-crossing low-swing switch drivers [32, 71], shown in Figure 4.30, are used to drive the current switches $M_{3,4}$, $M_{7,8}$ ... $M_{59,60}$.

The DAC_B is used to compensate the quantizer delay. Requirements on noise and linearity are much relaxed due to the large noise suppression by the gain of the integrators. For easy interface with current summation circuit, PMOS current cells are used instead of NMOS cells. The schematic of DAC_B is shown in Figure 4.31. Its interface to the current summation circuit is also shown. To reduce the clock feed-through and prevent two current switches from turning off at the same time, low-crossing low-swing switch drivers are used to drive its current switches as shown in Figure 4.32.

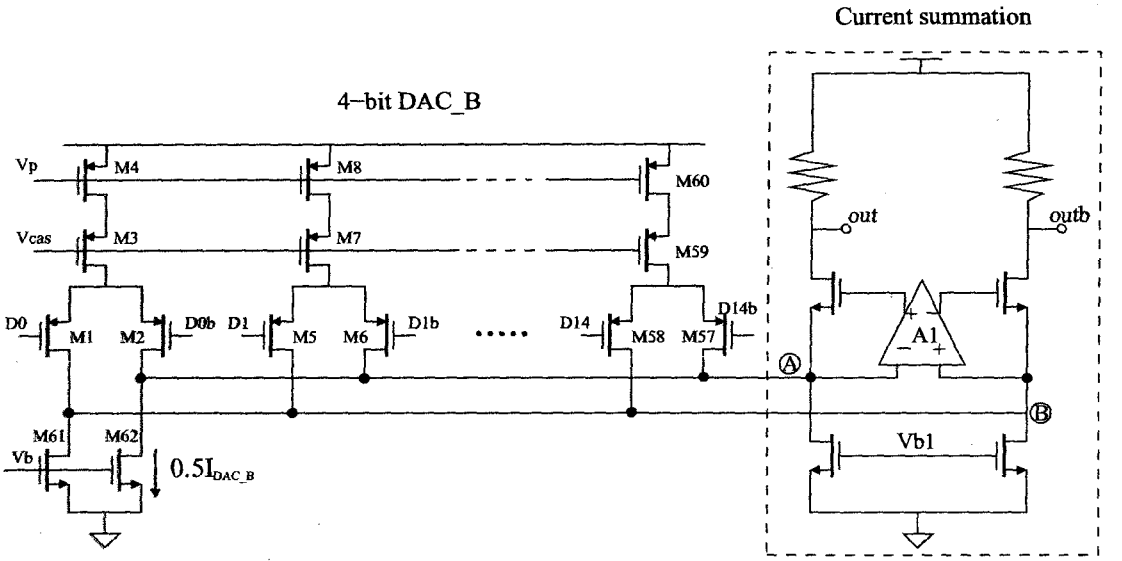


Figure 4.31: Schematic of DAC_B and its interface to the current summation.

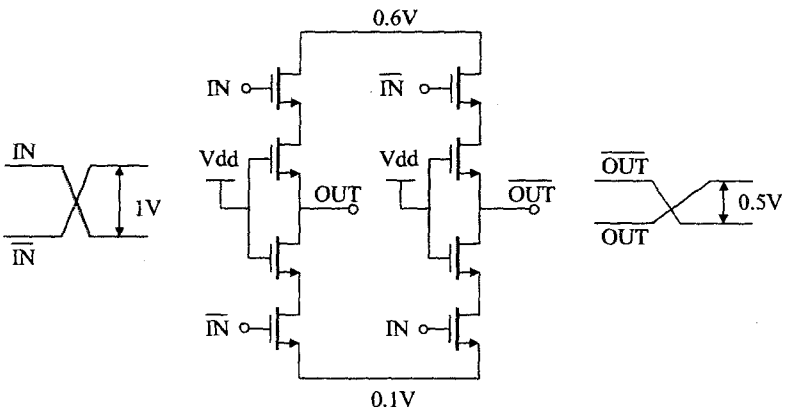


Figure 4.32: Low-crossing low-swing switch driver.

4.4 Summary

The implementation of the proposed wideband low-power continuous-time $\Sigma\Delta$ modulator was described in this chapter. A fully differential fifth-order loop filter that implements the desired transfer function has been designed. It is known that the first integrator in the loop filter has the most stringent performance requirements and care has been taken to ensure it will not degrade the overall performance. The following four integrators chosen as G_m-C type to save power. Due to its open loop operation, harmonic distortion becomes the dominant noise source. Several design techniques are adopted to increase its linearity including using resistive source degeneration, gain boosting auxiliary amplifiers, and two input driving amplifiers. An automatic on-chip RC tuning is design to compensate large process variation.

Additional circuits in the prototype described in this chapter include a 4-bit internal quantizer, two current-steering DACs. The design focus on the quantizer is to reduce its latency so that the excess loop delay is minimized for better performance and stability. DAC trimming technique is used to compensate the process variation in the quantizer. For feedback current-steering DACs, design emphasis is the current cell matching on the DAC_A. Large overdrive voltage of current source transistors are used to ensure the required matching.

Chapter 5

Experimental Results

A prototype of the continuous-time $\Sigma\Delta$ modulator proposed in the previous chapters has been realized in a 90nm one-poly seven-metal CMOS technology process through CMC Microsystems (http://www.cmc.ca). This chapter describes the layout design, test setup , and the performance of the modulator in the context of some state-of-the-art wideband (10MHz+) modulators.

5.1 Layout Design

The chip die photo is shown in Figure 5.1 with a die area of $0.5 \times 0.5mm^2$, excluding the pads. 44-pin CQFP package is used with total chip area of $1 \times 1mm^2$.

The continuous-time $\Sigma\Delta$ modulator is essentially a mixed-signal system. It contains pure analog blocks such as the fifth-order loop filter. It includes mixed-signal blocks such as the 4-bit internal quantizer and two current-steering DACs. It also has purely digital block such as TC-to-BC encoder. To achieve high resolution and linearity, care must be taken in the layout design to reduce the effects of mismatch, parasitics, and digital noise coupling to analog blocks [72, 73].

The main consideration in the chip floor plan is to minimize the noise coupling from

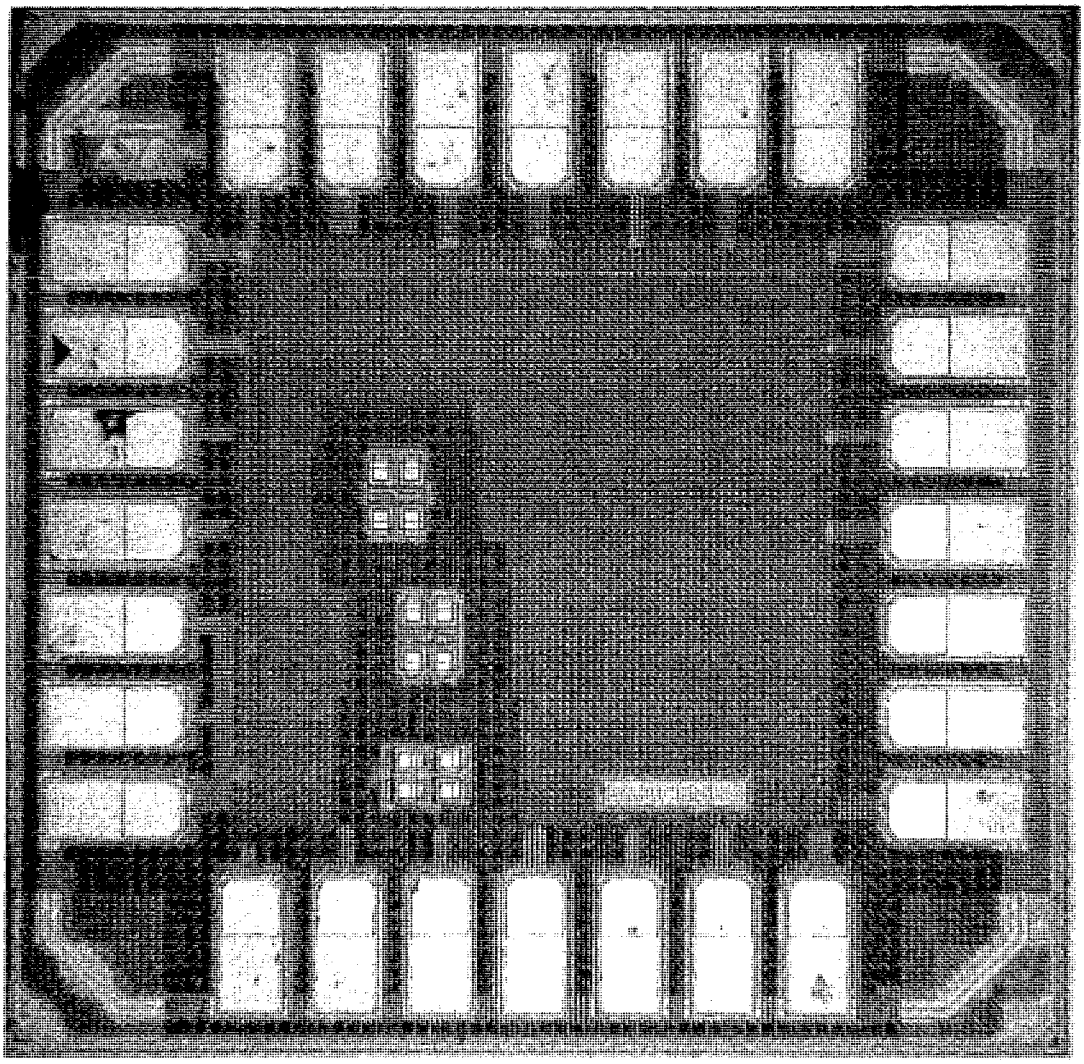


Figure 5.1: Chip die photo.

digital blocks to analog blocks. The most sensitive analog blocks, such as the first-stage integrator, are placed far away from the internal quantizer and the TC-to-BC encoder. Input analog signals enter the chip at the left bottom corner of the die, whereas digital outputs and clock signal are at the far right top corner. To further isolate the noise from the digital blocks, several approaches are considered.

- The analog circuits and digital circuits are powered by separate supplies named as AVDD and DVDD, respectively. The use of of separate supplies decouples the analog circuitry from the switching noise caused by large dynamic currents drawn from the digital supply.
- Guard rings are placed around the analog circuits to shield noise generated by digital circuits.
- Clock signals are drawn using a top metal layer to prevent interference from clock signal to analog circuitry.
- Coaxial type of wire is used to sensitive line and high frequency line such as input signals and clock signals.

Several other commonly used layout techniques have been employed to reduce mismatch and parasitics. Common-centroid technique is applied to all the input differential transistor pairs to reduce the effect of thermal and process linear gradients. Inter-digitation for all the transistors is used to minimize parasitics. Mirror symmetry is followed in the layout to reject common-mode interferences such as those from the power supplies and the substrate. In DAC_A as shown in Figure 5.2, current cells are encased within a ring of dummy cells to protect them from over-etching on all four sides. These dummy cells are the current cells with the same dimension as the non-dummy current cells.

5.2 Test Setup

Figure 5.3 illustrates the configuration of the test equipments used to evaluate the performance of the prototype chip. The differential sinusoidal input signals are produced by the

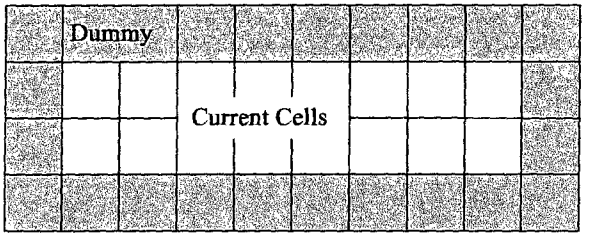


Figure 5.2: Dummy cells are used in DAC_A.

function arbitrary generator (Agilent 81150A). Keithley 6220 precision current sources provide external reference current to the bias circuits. Voltage supply and regulated reference voltages to the chip are provided by Keithley 2602 system source meter. The pulse pattern generator Agilent 81134A is used to provide low jitter clock signal for the modulator. The modulator digital outputs are captured by the digital oscilloscope (Agilent infiniium 54832D) and exported to a workstation. The FFT analysis of the output data is then performed in MATLAB.

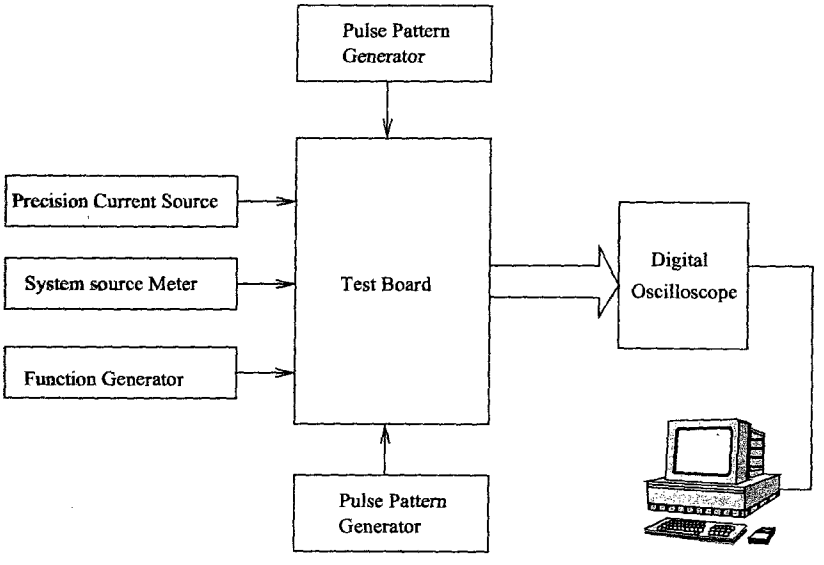


Figure 5.3: Experimental test setup.

5.3 Performance Evaluation and Comparison

The chip has been tested with a clock frequency of 800MHz. The output spectrum plots for -4.1dBFS ($0.6V_{pp}$) 5MHz and 21MHz input signals are shown in Figure 5.4 and Figure 5.5, respectively. The full scale input amplitude (0dBFS) is $0.96V_{pp}$. SNDR for both inputs is 70dB. No performance degradation has been observed with the increase in input signal frequency.

The modulator is also tested with a 5MHz input signal of varying amplitude. Since the signal bandwidth is 25MHz, up to 5^{th} order harmonics can be observed in the output spectrum. The SNDR versus input signal power level is plotted in Figure 5.6. The achieved DR is 75dB (12.2bits), where DR is defined as the difference between the two input levels for which SNDR $\geq$ 0dB.

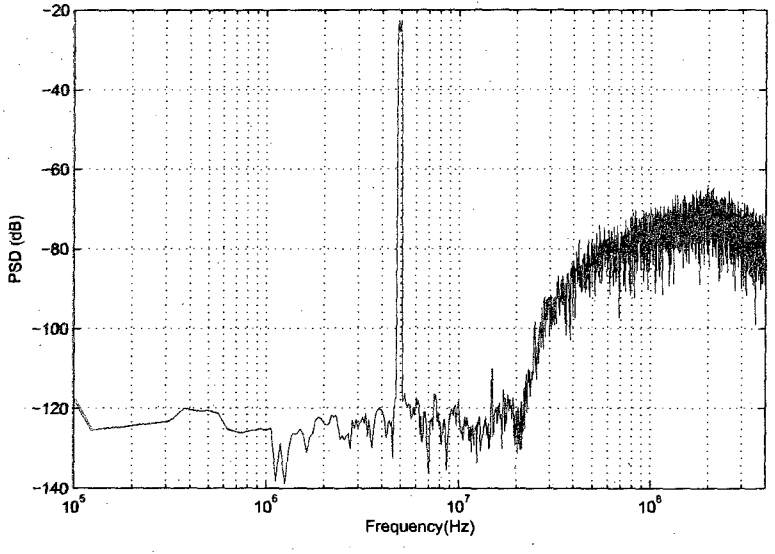


Figure 5.4: Power spectrum density (12800-point FFT) for a 5MHz -4.1dBFS input signal.

The overall performance of the modulator is summarized in Table 5.1. It achieves 75dB DR, 70dB SNDR over 25MHz signal bandwidth with oversampling ratio of 16. It dissipates 16.4mW from a 1.0-V supply.

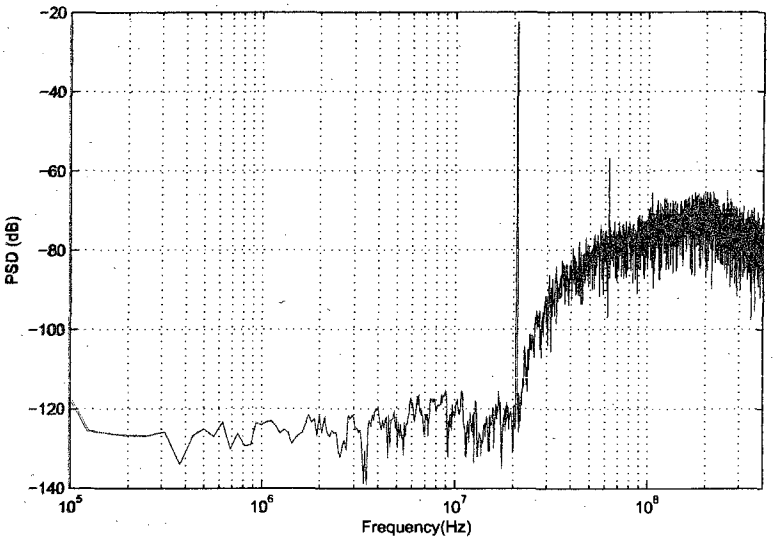


Figure 5.5: Power spectrum density (12800-point FFT) for a 21MHz -4.1dBFS input signal.

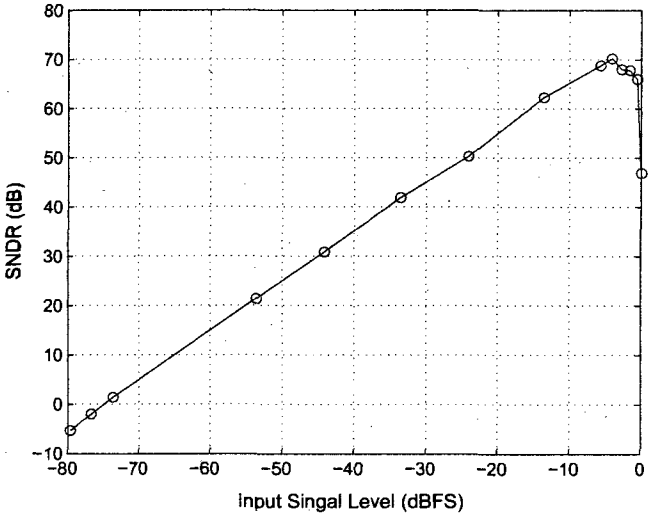


Figure 5.6: SNDR versus input signal power level for a 5MHz signal. Peak SNDR is 70dB. Dynamic range is 75dB.

Table 5.1: Performance Summary

Signal bandwidth	25MHz
Sampling frequency	800MHz
Oversampling ratio	16
Dynamic range	75dB
SNDR	70dB
Input range	0.96 V_{pp}
Power supply	1.0V
Power consumption	16.4mW
Technology	90nm 1P7M CMOS

Table 5.2: Performance summary of state-of-the-art wideband (10MHz+) low-pass CT $\Sigma\Delta$ ADCs

Work	CMOS(μm)/ Supply(V)	BW (MHz)	Power(mW)/ DR(dB)	SNDR (dB)	Architecture order(bits)	F_s (MHz)	FOM (pJ)
Bre04/[2]	0.18/1.8	10	122/67	57	2-2(4b)cas.	160	3.42
Sch07/[3]	0.18/1.8	10	7.5/72	66	3(1b)	640	0.11
Pat04/[4]	0.13/1.5	15	70/67	63.7	4(4b)	300	1.31
Cal06/[5]	0.18/1.8	20	103/55.2	48.8	3(4b) inter.	200	5.39
Mit06/[6]	0.13/1.2	20	20/80	74	3(4b)	640	0.061
This Work	90nm/1.0	25	16.4/75	70	5(4b)	800	0.069

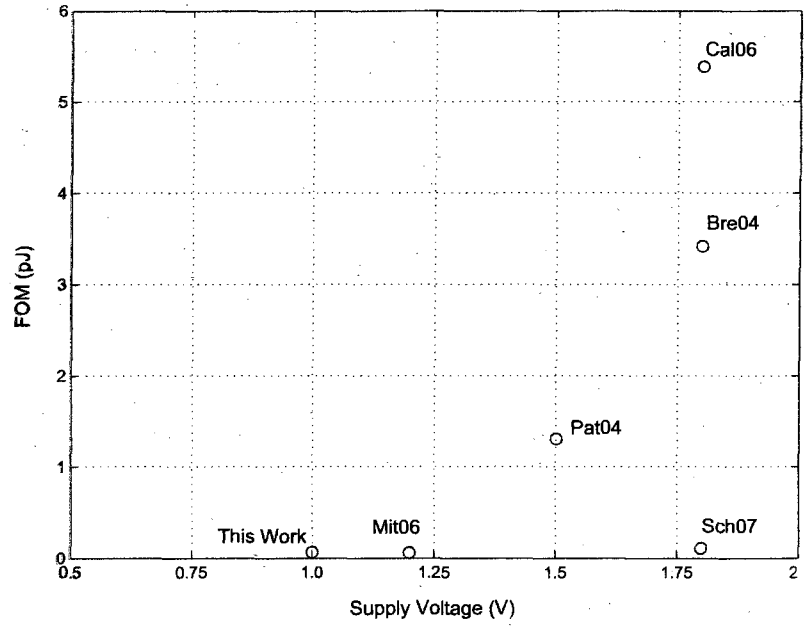


Figure 5.7: Performance comparison of state-of-the-art wideband (10MHz+) CT ΣΔ ADCs

To evaluate the performance of the modulator in the context of some state-of-the-art wideband (10MHz+) modulators, figure of merit (FOM) [14] is used with definition of

$$FOM = \frac{P}{2^b \cdot 2f_B} \tag{5.1}$$

where P is overall power consumption, b is overall modulator resolution, and f_B is the input signal bandwidth. The smaller the FOM value is, the better the overall performance is. Table 5.2 lists the performance of recent published wideband (10MHz+) continuous-time ΣΔ modulators. The entries in the table are sorted in order of signal bandwidth. A plot of FOM vs supply voltage is shown in Figure 5.7. As can be seen in Table 5.2 and Figure 5.7, this work is among the most improved published to date. It uses the lowest supply voltage. It has the highest input signal bandwidth while dissipating the lowest power among the bandwidths exceeding 15MHz.

5.4 Summary

The physical implementation of the proposed fifth-order continuous-time $\Sigma\Delta$ modulator was described in this chapter. The floor plan of the prototype chip was carefully chosen to minimize the noise coupling from the digital blocks to the sensitive analog blocks. Some commonly-used layout techniques were adopted to reduce mismatch and parasitics. Experimental results showed that the proposed system achieved a DR of 75dB and SNDR of 70dB over 25MHz input signal bandwidth with 16.4mW power dissipation. The performance is among the most improved continuous-time $\Sigma\Delta$ ADCs published to date.

Chapter 6

Conclusion

In this chapter, we summarize some key research contributions and results, and provide some recommendations for future work. There were two general thrusts of this research: 1) Design issues of wideband $\Sigma\Delta$ modulators at system, architecture, and circuit level were explored with particular emphasis on minimizing the power dissipation. 2) Techniques for implementing the proposed system in nanometer technology such as 90nm CMOS with very low supply voltage were investigated. Large process variations in nanometer CMOS technology affect the modulator performance dramatically. Measures including on-chip RC automatic tuning and DAC trimming were taken to minimizing the performance degradation caused by the process variations.

6.1 Key Research Contributions and Results

This research focuses on the design of a wideband low-power continuous-time $\Sigma\Delta$ modulator implemented in 90nm CMOS technology with very low power consumption, which has many applications including medical imaging and wireless receivers. The key research contributions and results are summarized below:

- An improved design method has been developed to speed up the design process for

CT ΣΔ ADCs by eliminating the transformation between DT and CT. The algorithm for generating time-delay root locus can be easily adapted for any system with delay elements.

- The comprehensive study on wideband low-power low-voltage CT ΣΔ ADCs at system and architecture level can serve as the starting point for future research to further push performance limits.
- The research results at circuit level are especially useful for any high-speed low-power analog/mixed signal circuit design using nanometer CMOS technology.
- The prototype chip is the implementation of the proposed CT ΣΔ ADC. It uses the lowest supply voltage. It has the highest signal bandwidth while dissipating the lowest power among the bandwidths exceeding 15MHz.
- The proposed system is the first wideband CT ΣΔ ADC that has been implemented in nanometer CMOS. It has demonstrated the feasibility of realizing a ΣΔ ADC in nanometer CMOS with low power consumption.

6.2 Recommended Future Work

6.2.1 Designing CT ΣΔ ADC Less Sensitive to Clock Jitter

To design CT ΣΔ ADC modulators for even wider bandwidths with high resolution requires even higher clock sampling rate. Clock frequencies will reach GHz range and hence the clock jitter issue becomes more critical. Some non-rectangular DAC shapes such as an sine-shaped DAC might be worth exploring to reduce clock jitter sensitivity.

6.2.2 Further Reducing Power Consumption

Various design strategies can be adopted to further lower the power consumption. For example, more aggressive power scaling can be done based on circuit level simulation to further reduce the power consumption along the integrator chain; The multi-bit quantizer

does not have to be flash ADC; Implementing the system in an even smaller technology with lower power supply and shorter channel length will also help to reduce the power consumption in digital blocks.

6.2.3 Reconfigurable CT ΣΔ ADC for Multi-Standard Wireless Applications

The diversity in wireless communication standards requires receivers to have multi-mode operation capability. Reconfigurable continuous-time ΣΔ modulators for A/D converters for multi-mode wireless communication applications is a interesting research topic.

References

[1] S. Yan and E. Sánchez-Sinencio, "A continuous-time ΣΔ modulator with 88-dB dynamic range and 1.1-MHz signal bandwidth," *IEEE Journal of Solid-State Circuits*, vol. 39, no. 1, pp. 75–86, 2004.

[2] L. J. Breems, R. Rutten, and G. Wetzker, "A cascaded continuous-time ΣΔ modulator with 67-dB dynamic range in 10-MHz bandwidth," *IEEE Journal of Solid-State Circuits*, vol. 39, no. 12, pp. 2152–2160, 2004.

[3] R. Schoofs, M. S.J.Steyaert, and W. M.C.Sansen, "A design-optimized continuous-time delta-sigma ADC for WLAN applications," *IEEE Transactions on Circuits and Systems*, vol. 54, no. 1, pp. 209–217, 2007.

[4] S. Patón, A. D. Giandomenico, L. Hernández, A. W. T. Pötscher, and M. Clara, "70-mW 300-MHz CMOS continuous-time ΣΔ ADC with 15-MHz bandwidth and 11 bits of resolution," *IEEE Journal of Solid-State Circuits*, vol. 39, no. 7, pp. 1056–1063, 2004.

[5] T.C.Caldwell and D.A.Johns, "A time-interleaved continuous-time ΔΣ modulator with 20-MHz signal bandwidth," *IEEE Journal of Solid-State Circuits*, vol. 41, no. 7, pp. 1578–1588, 2006.

[6] G. Mitteregger, C. Ebner, S. Mechnig, T. Blon, C. Holuigue, and E. Romani, "A 20-mW 640-MHz cmos continuous-time ΣΔ ADC with 20-MHzsignal bandwidth, 80-dB dynamic range and 12-bit ENOB," *IEEE Journal of Solid-State Circuits*, vol. 41, no. 12, pp. 2641–2649, 2006.

[7] A. V. Oppenheim and R. W. Schafer, *Discrete-Time Singal Processing.* New Jersey: Prentice Hall, 1989.

[8] W. R. Bennett, "Spectra of quantized signals," *Bell Syst. Tech. J.*, vol. 27, pp. 446–472, 1948.

[9] B. Widrow, "A study of rough amplitude quantization by means of nyquist sampling theory," *IRE Trans. Circuit Theory*, vol. Ct-3, pp. 266–276, 1956.

[10] R. van de Plassche, *Integrated Analog-to-Digital and Digital-to-Analog Converters.* Kluwer Academic Publishers, 1994.

[11] R. M. Gray, "Quantization noise spectra," *IEEE Trans. Inform. Theory*, vol. 36, no. 6, pp. 1220–1244, 1990.

[12] F. Medeiro and B. Perez-Verdu, *Top-Down Design of High-Performance Sigma-Delta Modulators.* Dordrecht: Kluwer Academic Publisher, 1999.

[13] F. Gerfers, K. M. Sho, M. Ortmanns, and Y. Manoli, "Figure of merit based design strategy for low-power cotninuous-time $\Sigma\Delta$ modulators," in *Proc. IEEE Int. Symp. Circuits Systm.*, 2002, pp. 233–236.

[14] M. Ortmanns and F.Gerfers, *Continuous-Time Sigma-Delta A/D Conversion.* Springer, 2006.

[15] J. C. Candy, "A use of double integration in sigma-delta modulation," *IEEE Trans. Communications*, vol. 33, pp. 249–258, 1985.

[16] L. E. Larson, T. Cataltepe, and G. C. Temes, "Multibit oversampled $\Sigma\Delta$ A/D converter with ditial error corrention," *Electronics Letters*, no. 8, pp. 1051–1052, 1988.

[17] W. Zhang, "High-speed high-resolution low-power self-calibrated digital-to-analog converters." Ph.D. dissertation, Iowa State University, Iowa U.S.A, 2001.

[18] S. R. Norsworthy, R. Schreier, and G. C. Temes, *Delta-Sigma Data converters- Theory, Design and Simulation.* IEEE Press, 1996.

[19] T. Hayashi, Y. Inabe, K. Uchimura, and T. Kimura, "A multi-stage delta-sigma modulator without double integration loop," *Int. Solid-State Cir. Conf. Technical Digest*, pp. 182–183, 1986.

[20] R. T. Baird and T. S. Fiez, "a low oversampling ratio 14-b 500-kHz $\Sigma\Delta$ ADC with a self-calibrated multibit DAC," *IEEE J. Solid-State Circ.*, no. 3, pp. 312–320, 1996.

[21] J. Nedved, J. Vanneuville, D. Gevaert, and J. Sevenhans, "A transistor-only switched current sigma-delta A/D converter for a CMOS speech code," *IEEE J. Solid-State Circ.*, no. 7, pp. 819–822, 1995.

[22] J. Jensen, G. Raghavan, A. E. cosand, and R. H. Walden, "A 3.2-GHz second-order delta-sigma modulator implemented in Inp HBT technology," *IEEE J. Solid-State Circ.*, no. 10, pp. 1119–1127, 1995.

[23] J. A. Cherry and W. M. Snelgrove, "clock jitter and quantizer metastability in continuous-time delta-sigma modulators," *IEEE Trans. circuits and Systems-II*, vol. 46, no. 6, pp. 661–676, 1999.

[24] ——, "Excess loop delay in continuous-time delta-sigma modulators," *IEEE Trans. circuits and Systems-II*, vol. 46, no. 4, pp. 367–389, 1999.

[25] I. Fujimori, L. Longo, A. Hairapetian, K. Seiyama, S. Kosic, J. Cao, and S. L. Chan, "A 90-dB SNR 2.5-MHz output rate ADC using cascaded multibit sigma-delta modulator at 8x oversampling ratio," *IEEE J. Solid-State Circuits*, vol. 35, no. 12, pp. 1820–1828, 2000.

[26] T. L. Brooks, D. H. Robertson, D. F. Kelly, A. D. Muro, and S. W. Harston, "A cascaded sigma-delta pipeline A/D converter with 1.25MHz signal bandwidth and 89dB SNR," *IEEE J. Solid-State Circuits*, vol. 32, no. 12, pp. 1896–1906, 1997.

[27] L. A. Williams and B. A. Wooley, "A third-order sigma-delta modulator with extended dynamic range," *IEEE J. Solid-Stage Circuits*, vol. 29, no. 3, pp. 193–202, 1994.

[28] J. A. Cherry, W. M. Snelgrove, and W. Gao, "On the design of a fourth-order continuous-time LC delta-sigma modulator for UHF A/D conversion," *IEEE Trans. Circuits and Systems-II*, vol. 47, no. 6, pp. 518–530, 2000.

[29] E. H. Dagher, P. A. Stubberud, W. K. Masenten, M. Conta, and T. v. Dinh, "A 2-GHz analog-to-digital delta-sigma modulator for CDMA receiver with 79-dB signal-to-noise-ratio in 1.23-MHz bandwidth," *IEEE Trans. Circuits and Systems-II*, vol. 39, no. 11, pp. 1819–1828, 2004.

[30] T. Burger and Q. Huang, "A 13.5-mW 185-Msample/s $\Sigma\Delta$ modulator for UMTS/GSM dual-standard IF reception," *IEEE J. Solid-Stage Circuits*, vol. 36, no. 12, pp. 1868–1878, 2001.

[31] P. Balmelli and Q. Huang, "A 25-MS/s 14-b 200-mW $\Sigma\Delta$ modulator in 0.18-μm CMOS," *IEEE Journal of Solid-State Circuits*, vol. 39, no. 12, pp. 2161–2169, 2004.

[32] S. Yan, "Baseband continuous-time sigma-delta analog-to-digital conversion for ADSL applications," Ph.D. dissertation, Texas A&M University, Texas U.S.A, 2002.

[33] R. Schreier and B. Zhang, "Delta-sigma modulators employing continuous-time circuitry," *IEEE Transactions on Circuits and Systems I*, vol. 43, no. 4, pp. 324–332, 1996.

[34] B. E. Boser and B. A. Wooley, "The design of sigma-delta modulation analog-to-digital converters," *IEEE J. Solid-State Circuits*, vol. 23, no. 12, pp. 1298–1308, 1988.

[35] E. J. van der Zwan and E. C. Dijkmans, "A 0.2-mW CMOS $\Sigma\Delta$ modulator for speech coding with 80 dB dynamic range," *IEEE J. Solid-State Circuits*, vol. 31, no. 12, pp. 1873–1880, 1996.

[36] L. Hernandez, A. W. adn S. Paton, and A. D. Giandomenico, "Modelling and optimization of low pass continuous-time sigma-delta modulators for clock jitter noise reduction," in *Proc. IEEE International Symposium on Circuits and Systems*, May 2004, pp. I 1072–1075.

[37] H. Tao, L. Tóth, and J. M. Khoury, "Analysis of timing jitter in bandpass sigma-delta modulators," *IEEE Transactions on Circuits and Systems II*, vol. 46, no. 8, pp. 991–1001, 1999.

[38] F. Gerfers, M. Ortmanns, and Y. Manoli, "Design issues and performance limitations of a clock jitter insensitive multibit DAC architecture for high-performance low-power ct $\Sigma\Delta$ modulators," in *Proc. IEEE International Symposium on Circuits and Systems*, May 2004, pp. I 1076–1079.

[39] S. Luschas and H. S. Lee, "High-speed $\Sigma\Delta$ modulators with reduced timing jitter sensitivity," *IEEE Transactions on Circuits and Systems II*, vol. 49, no. 11, pp. 712–720, 2002.

[40] J. A. Cherry and W. M. Snelgrove, *Continuous-Time Delta-Sigma Modulators for High-Speed A/D Conversion.* Kluwer Academic Publishers, 2000.

[41] R. Khoini-Poorfard, L. B. Lim, and D. A. Johns, "Time-interleaved oversampling A/D converters: theory and practice," *IEEE Transactions on Circuits and Systems II*, vol. 44, no. 8, pp. 634–645, 1997.

[42] P. P. Vaidyanathan, *Multirate Systems and Filter Banks.* Englewood Cliffs, NJ: Prentice-Hall, 1993.

[43] M. Kozak, M. Karaman, and I. Kale, "Efficient architectures for time-interleaved oversampling delta-sigma converters," *IEEE Transactions on Circuits and Systems II*, vol. 47, no. 8, pp. 802–810, 2000.

[44] M. Kozak and I. Kale, "Novel topologies for time-interleaved delta-sigma modulators," *IEEE Transactions on Circuits and Systems II*, vol. 47, no. 7, pp. 639–654, 2000.

[45] R. H. M. van Veldhoven, "A triple-mode continuous-time $\Sigma\Delta$ modulator with switched-capacitor feedback DAC for a GSM-EDGE/CDMA2000/UMTS receiver," *IEEE Journal of Solid-State Circuits*, vol. 38, no. 12, pp. 2069–2076, 2002.

[46] L. Dorrer, F. Kuttner, P. Greco, P. Torta, and T. Hartig, "A 3-mW 74-dB snr 2-MHz continuous-time delta-sigma ADC with a tracking ADC quantizer in 0.13-μm CMOS," *IEEE Journal of Solid-State Circuits*, vol. 40, no. 12, pp. 2416–2427, 2005.

[47] A. Marques, V. Peluso, M. S. Steyaert, and W. M. Sansen, "Optimal parameters for $\Sigma\Delta$ modulator topologies," *IEEE Transactions on Circuits and Systems II*, vol. 45, no. 9, pp. 1232–1241, 1998.

[48] B. P. Agrawal and K. Shenoi, "Design methodology for $\Sigma\Delta M$," *IEEE Trans. on Communications*, vol. COM31, no. 3, pp. 360–370, 1983.

[49] O. Shoaei and W. M. Snelgrove, "Design and implementation of a tunable 40MHz-70MHz Gm-C bandpass $\Delta\Sigma$ modulator," *IEEE Trans. on Circuits and Systems II*, vol. 44, no. 7, pp. 521–530, 1997.

[50] P. Benabes, M. Keramat, and R. Kielbasa, "Sigma-delta modulators employing continuous-time filters," *Analog Integrated Circuits and Signal Processing*, vol. 23, no. 2, pp. 141–152, 2000.

[51] R. Schreier, "An empirical study of high-order single-bit delta-sigma modulators," *IEEE Transactions on Circuits and Systems II*, vol. 40, no. 8, pp. 461–466, 1993.

[52] F. Chen, T. Kuendiger, and S. Erfani, "Improved direct stability analysis of high-order continuous-time sigma-delta modulators," in *Proc. IEEE North-East Workshop on Circuits and Systems*, Ottawa, Canada, June 2006, pp. 73–76.

[53] R. T. Baird and T. S. Fiez, "Stability analysis of high-order delta-sigma modulator for ADCs," *IEEE Trans. on Circuits and Systems II*, vol. 41, no. 1, pp. 59–62, 1994.

[54] J. Engelen, "Stability analysis and design of bandpass sigma delta modulators," Ph.D. dissertation, Eindhoven University of Technology, The Netherlands, 1999.

[55] A. Krall, "Stability criteria for feedback systems with a time lag," *J.SIAM ser. A, Contro*, vol. 2.2, pp. 160–170, 1965.

[56] ——, "An algorithm for generating root locus diagrams," *Communications of the ACM*, vol. 10, no. 3, pp. 186–188, 1967.

[57] W. H. Press, S. A. Teukolsky, W. T. Vetterling, and B. P. Flannery, *Numerical Recipes in C++: The Art of Scientific Computing.* Cambridge University Press, 2002.

[58] L. Breems and J. H. Huijsing, *Continuous-Time Sigma-Delta Modulation for A/D Conversion in Radio Receivers.* Kluwer Academic Publishers, 2001.

[59] R. Schaumann and M. E. van Valkenburg, *Design of Analog Filters.* Oxfor University Press, 2001.

[60] F. Chen, T. Kuendiger, and S. Erfani, "Compensation of finite gbw induced performance loss on a fourth-order continuous-time sigma-delta modulator," in *Proc. IEEE Canadian Conference on Electrical and Computer Engineering*, Ottawa, Canada, May 2006, pp. 73–76.

[61] B. Razavi, *Design of Analog CMOS Integrated Circuits.* McGraw-Hill, 2000.

[62] C.-H. Cho, "A power optimized pipeline analog-to-digital converter design in deep sub-micron CMOS technology." Ph.D. dissertation, Georgia Institute of Technology, Atlanta U.S.A, 2005.

[63] Y. Zhang, "High-speed low-power continuous-time delta-sigma modulators," Ph.D. dissertation, Stony Brook University, Stony Brook, NY U.S.A, 2005.

[64] E. Sánchez-Sinencio and J. Silva-Martinez, "CMOS transconductance amplifiers, architectures and active filters: a tutorial," in *IEEE Proceedings on Circuits, Devices and Systems.*, vol. 147, no. 1, 2000, pp. 3–12.

[65] *CMOS090GP Design Rule Manual 90nm General Purpose.* STM Microelectronics, France, 2004.

[66] B. Xia, S. Yan, and E. Sánchez-Sinencio, "An RC time constant auto-tuning structure for high linearity continuous-time $\Sigma\Delta$ modulators and active filters," *IEEE Transactions on Circuits and Systems I*, vol. 51, no. 11, pp. 2179–2188, 2004.

[67] S. Park, "Design techniques for high performance CMOS flash analog-to-digital converters," Ph.D. dissertation, University of Michigan, Ann Arbor, MI U.S.A, 2006.

[68] D. Lee, J. Yoo, K. Choi, and J. Ghaznavi, "Fat tree encoder design for ultro-high speed flash A/D converters," in *IEEE Proceedings on Circuits, Devices and Systems.*, vol. 147, no. 1, 2002, pp. 87–90.

[69] A. V. den Bosch, M. Steyaert, and W. Sansen, "An accurate statistical yield model for CMOS current-steering D/A converters," in *Proc. IEEE International Symposium on Circuits and Systems*, Geneva, Switzeland, May 2000, pp. IV 105–108.

[70] M. Pelgrom, A. Duinmaijer, and A. Welbers, "Matching properties of MOS transistors," *IEEE Transactions on Circuits and Systems II*, vol. SC, no. 24, pp. 1433–1439, 1989.

[71] Z. Li, "Design of a 14-bit Continuous-Time Delta-Sigma A/D Modulator with 2.5MHz Signal Bandwidth." Ph.D. dissertation, Oregon State University, Eugene, OR U.S.A, 2006.

[72] C. Saint and J. Saint, *IC Mask Design: Essential Layout Techniques.* McGraw-Hill, 2002.

[73] A. Hastings, *Art of Analog Layout.* Prentice Hall, 2005.

[74] E. Hogenauer, "An economical class of digital filters for decimation and interpolation," *IEEE Transactions on Acoustics, Speech, and Signal Processing*, vol. 29, no. 2, pp. 155 – 162, 1981.

[75] R. E. Crochiere and L. R. Rabiner, *Multirate Digital Signal Processing.* Prentice Hall, 1983.

Appendix A

Decimation Filter Design

The output of a $\Sigma\Delta$ modulator contains the input signal together with its out-of-band components, modulation noise, circuit noise an interference. A decimation digital filter is required to attenuate all of the out-of-band components of the signal and re-sample it at the Nyquist rate without insert significant noise penalty because of aliasing. A example of a decimation filter is given in this appendix. It consists of two stages. The filter in the first stage of decimation process is designed primarily to remove modulation noise, because that noise dominates at high frequency. Out-of-band components of the signal that dominate at lower frequency are attenuated by the abrupt low-pass filter in the second stage of the decimation process as shown in Figure A.1. Our example of the decimation filter has the architecture shown in Figure A.2.

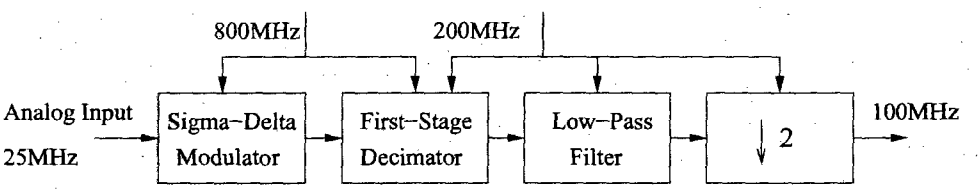


Figure A.1: Decimating the output of a $\Sigma\Delta$ modulator in two stages, from 800MHz to 200MHz and then to 100MHz.

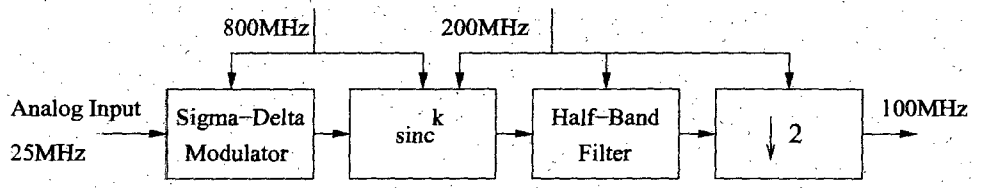


Figure A.2: Filter architecture for decimation.

As can be seen in Figure A.2, a $sinc^k$ filter is chosen as the first stage decimator because it does not require the use of digital multipliers [74]. The transfer function of the $sinc^k$ decimation filter has the general form of

$$H(z) = \left(\frac{1}{M} \cdot \frac{1 - z^{-M}}{1 - z^{-1}}\right)^k \tag{A.1}$$

and its frequency response is

$$|H(e^{j\omega})| = \left(\frac{1}{M} \cdot \frac{sin(\omega M/2)}{sin(\omega/2)}\right)^k = \left(\frac{sinc(\omega M/2)}{sinc(\omega/2)}\right)^k \tag{A.2}$$

where M is the decimation ratio and $\omega = 2\pi f/f_s$. For optimum decimating result, k is chosen as L+1 with $\Sigma\Delta$ modulator loop filter order of L [18].

In our example, we have intermediate sampling frequency of $f_s/4 = 200MHz$ with decimation ratio of M=4. The decimator has the transfer function of

$$H(z) = \left(\frac{1}{4} \cdot \frac{1 - z^{-4}}{1 - z^{-1}}\right)^6 \tag{A.3}$$

The implementation of the above filter is shown in Figure A.3. And the corresponding frequency response is shown in Figure A.4.

For second stage decimation, a half-band filter is used, which is characterized by the constraints that its passband and stopband ripples are the same ($\delta_p = \delta_s$) and the cutoff frequencies are symmetrical around $\pi/2$. It uses one-fourth of multiplications needed for arbitrary FIR filter. The filter transfer function is:

$$H(z) = z^{-K} \cdot \left[h(0) + \sum_{n=1}^{K} h(n)(z^n + z^{-n})\right] \tag{A.4}$$

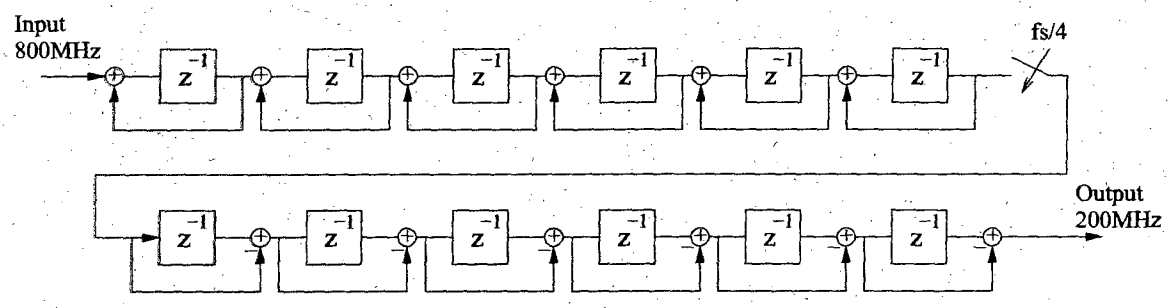


Figure A.3: Cascaded integrator comb (CIC) implementation of the first stage $sinc^k$ decimator.

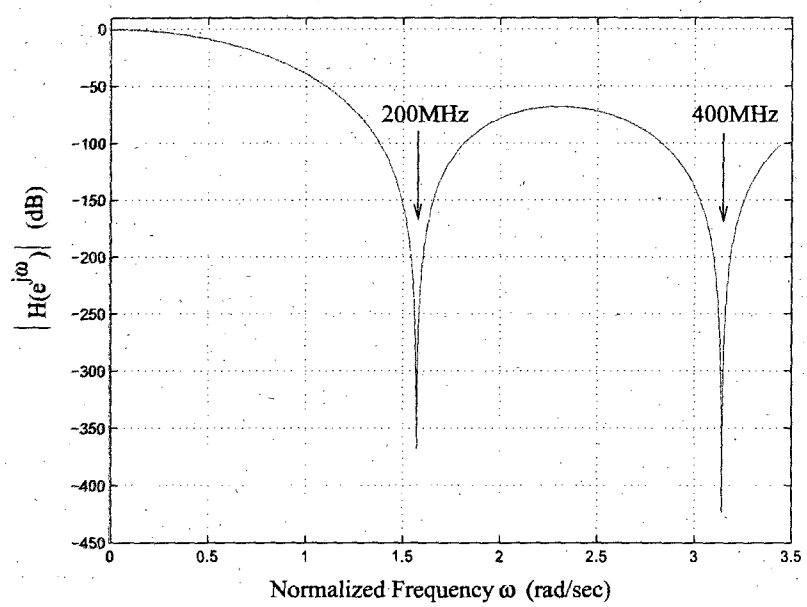


Figure A.4: Frequency response of the first stage $sinc^k$ decimator.

where $K = \frac{N-1}{2}$. N is the required filter order, which can be calculated using kaiser window method. The coefficients $h(n)$ can be obtained using:

$$h(n) = \frac{sin(\pi n/2)}{\pi n/2} \tag{A.5}$$

where $n = 0, 1, ..., \frac{N-1}{2}$. The required frequency response of the our half-band filter is shown in the Figure A.5.

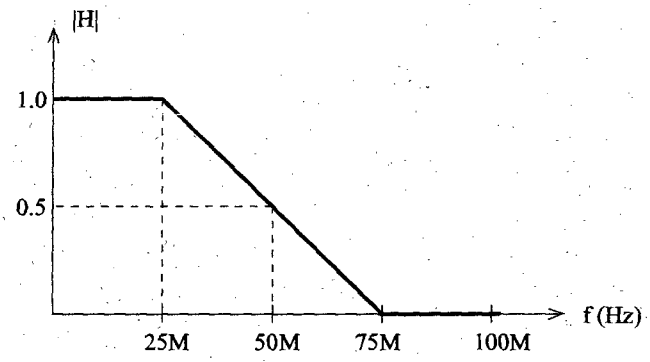


Figure A.5: Required frequency response of the half-band low-pass filter.

The example of a half-band filter with the order of 15 has the following transfer function:

$$\begin{aligned} H(z) &= z^{-7}[h(0) + \sum_{n=1}^{7} h(n)(z^{-n} + z^{n})] \\ &= h(7)(1 + z^{-14}) + h(5)(z^{-2} + z^{-12}) \\ &\quad + h(3)(z^{-4} + z^{-10}) + h(1)(z^{-6} + z^{-8}) + h(0)z^{-7} \end{aligned} \tag{A.6}$$

Half-band filter can be efficiently implemented with a poly-phase direct-form filter [75]. The realization of the above half-band filter with decimation ratio of M=2 is shown in Figure A.6. The pseudo code of the implementation is shown below:

```
%%% beginning of the code %%%
% nft is the data length of input x(n)
for n=0:(nft/2-1)
    x0(n)=x(2*n)
```

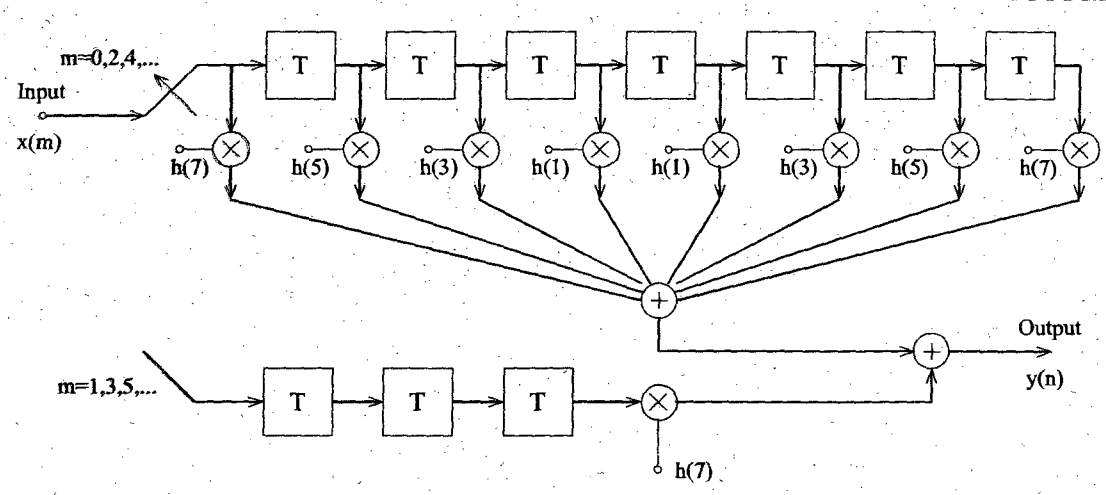


Figure A.6: Poly-phase direct-form implementation of a N=15 M=2 half-band filter.

```
end
for n=1:nft/2
    x1(n)=x(2*n-1)
end
for k=0:(nft/2-1)
    y(k)=h(7)[x0(k)+x0(k-1)]+h(5)[x0(k-1)+x0(k-6)]
         +h(3)[x0(k-2)+x0(k-5)]+h(1)[x0(k-3)+x0(k-4)]+h(0)x1(k-3)
end
%%%% end of the code %%%
```

Appendix B

Power Spectrum Estimation

This appendix shows the steps that are used to estimate SNDR of the output of the proposed $\Sigma\Delta$ modulator.

- N - Length of data and length of FFT.
- K - Number of sets for averaging periodograms.

1. Step One: Apply Hann window to the output signal.

$$\begin{aligned} y_w(n) &= y(n)w(n) \\ &= y(n) \cdot \frac{1}{2}\left[1 - cos\left(\frac{2\pi n}{N}\right)\right] \end{aligned} \tag{B.1}$$

   where $n = 0, 1, 2, ...N-1$, $y(n)$ is the modulator output signal, and $w(n)$ is the Hann window function.

2. Step Two: FFT the stream $y_w(n)$.

$$Y_w(k) = \sum_{n=0}^{N-1} y_w(n) e^{-j2\pi kn/N} \tag{B.2}$$

   where $k = 0, 1, 2, ..., N-1$.

3. Step Three: Calculate periodogram of $Y_w(k)$ for $k = 0, 1, 2, ...N/2$.

$$P(0) = \frac{1}{N^2}|Y_w(0)|^2 \tag{B.3}$$

$$P(k) = \frac{1}{N^2}\left[|Y_w(k)|^2 + |Y(N-k)|^2\right] \qquad k = 1, ...(\frac{N}{2} - 1) \tag{B.4}$$

$$P(\frac{N}{2}) = \frac{1}{N^2}|Y_w(\frac{N}{2})|^2 \tag{B.5}$$

4. Step Four: Take another K-1 sets of data, each is N long, repeat Step One to Step Three. Average P(k) to reduce the variance.

$$P(0) = \frac{1}{K}\sum_{i=1}^{K} P_i(0) \tag{B.6}$$

$$P(k) = \frac{1}{K}\sum_{i=1}^{K} P_i(k) \tag{B.7}$$

$$P(\frac{N}{2}) = \frac{1}{K}\sum_{i=1}^{K} P_i(\frac{N}{2}) \tag{B.8}$$

5. Step Five: Calculate the SNDR in certain frequency range.

The following is the Matlab code used in this work to estimate SNDR of the output of the proposed $\Sigma\Delta$ modulator.

```
%Matlab code to estimate SNDR
%using periodogram to estimate power spectrum and SNR of the signal y(n)
%input: signal y, data length nfft(choose the one that is to the power of 2)
%sampling frequency fs; output: plot PSD
%and output SNDR of the y(n).
load matlab_DAC_C.mat
fs=4000e6;
nfft=20000; % for 5u second
K=1; %K successive sets of data (each set is nfft long)
y0=[]; %take value form imported data file
y1=[];
y0=data';
```

```
y1=y0(2:nfft+1)*480;
%---------------- Begin ------------------------------------------
for i=1:nfft
    fk(i)=(i-1)*fs/nfft;
end
%STEP 1: apply Hann window to the output bit stream to reduce spectrum leakage.
n=1:nfft; %index
hw=0.5*(1-cos(2*pi*n/nfft)); %Hann window
yw1=y1.*hw;
%STEP 2: FFT the yw.
Yw1=fft(yw1,nfft);
%STEP 3: Calculate periodogram P of Yw for k=0,1,...N/2
P1=[];
%------------ Data set 1 --------------------------
P1(1)=1/nfft^2*(Yw1(1).*conj(Yw1(1))); %index is 1, frequency is 0
for k=2:(nfft/2)
    P1(k)=1/nfft^2*((Yw1(k).*conj(Yw1(k)))+(Yw1(nfft-k).*conj(Yw1(nfft-k))));
end
P1(nfft/2+1)=1/nfft^2*(Yw1(nfft/2+1).*conj(Yw1(nfft/2+1)));
%-----------------------------------------------------------------
%STEP 4: plot power spectrum over frequency range[0 fs/2]
figure;
plot(fk(1:200),10*log10(P1(1:200)));
xlabel('frequency(Hz)');
ylabel('Amplitude');
grid on;
%STEP 5: calculate the SNDR in frequency range k=[0 64] fk=k*fs/nfft
%know the signal bandwidth(number of bins); know the signal power bin numbers
Ptotal=0; %total in-band power
```

```
Psignal=0; %total in-band signal power
for i=1:125
    Ptotal=P1(i)+Ptotal;
end
%take a look at P vector to determine the number of bins
%the signal power pas spread to
for j=23:27
  Psignal=Psignal+P1(j);
end
Pnd=Ptotal-Psignal; %total in-band noise and distortion
SignalPower=10*log10(Psignal)
TotalNoiseandDistortion=10*log10(Pnd)
SNDR=10*log10(Psignal/Pnd)
%---------------------- END -----------------------------------
```

Appendix C

C/C++ Code for Time Delay Root Locus

This appendix shows the C/C++ code written to calculate time delay root locus.

```
%---------- Make file--------------------
#CCC = /usr/local/opt/SUNWspro/bin/CC
#CC = /usr/local/opt/SUNWspro/bin/cc
#LD = /usr/local/opt/SUNWspro/bin/ld
CCC = /usr/local/bin/g++
CC = /usr/local/bin/gcc
LD = /usr/ccs/bin/ld
#CFLAGS = -mt -c -I/usr/include -I/usr/local/opt/SUNWspro/include
#CFLAGS = -g -I/usr/include -I/usr/local/include
              -mhard-float -mcpu=ultrasparc -mtune=ultrasparc
CFLAGS = -g -I/usr/include -I/usr/local/include
#LDFLAGS = -mt -L/usr/lib -L/usr/local/opt/SUNWspro/lib -lm -lpthread -lc
LDFLAGS = -L/usr/lib -L/usr/local/lib -lm -lc -lstdc++
OBJS = complex.o points.o
stable: $(OBJS) stability.cc
```

```
$(CCC) $(CFLAGS) stability.cc $(LDFLAGS) -o stable $(OBJS)
complex.o: complex.cc complex.hh
$(CCC) -c $(CFLAGS) -o complex.o complex.cc
points.o: points.cc points.hh complex.cc complex.hh
$(CCC) -c $(CFLAGS) -o points.o points.cc
clean:
rm -f *.o stable
%--------------stable.cc-------------------
#include<stdio.h>
#include<math.h>
#include "complex.hh"
#define ERROR 1e-8
/* Function prototypes */
double characteristic(double, double);
double calcK(double, double);
int findVal(double,double,double,double,double,double);
double bisection(double, double , double);
int main(int nargs, char *arg[])
{ double xmin, xmax, ymin, ymax;
double dx,dy;
/*range of s=x+jy for root locus plot*/
 xmin = -1.5;
 xmax = 1.5;
 ymin = 0.0;
 ymax = M_PI;
/*incremental value of x and y */
dx = 0.0001;
dy = 0.01;
findVal(xmin, xmax, ymin, ymax, dx,dy);
```

```
return 0;
}
int findVal(double x1, double x2, double y1, double y2, double dx, double dy)
{ double x, y;
double pa,py;
double a, k;
double root_y;
for(x = x1; x <= x2; x += dx)
{ a = 0.0;
py = y1;
for(y = y1; y <= y2; y += dy)
{ pa = a;
a = characteristic(x,y);
if(fabs(a) == 0.0)
{ k = calcK(x,y);
if( k >=0.0)
printf("%2.10lf %2.10lf %2.10lf\n" ,x,y,k);
}
else if((a < 0.0 && pa > 0.0) || (a > 0.0 && pa < 0.0))
{ root_y = bisection (x, py, y);
k = calcK(x,root_y);
if( k >=0.0)
printf("%2.10lf %2.10lf %2.10lf\n" ,x,root_y,k);
}
py = y;
}
}return 0;
}
double bisection(double x, double py, double y)
```

```
{ double abstol;
double f_lower, f_higher, f_bisect, y_lower, y_higher, y_bisect, root;
int SUCCESS;
y_lower = py;
y_higher = y;
f_lower = characteristic (x, y_lower);
f_higher = characteristic (x, y_higher);
SUCCESS = 0;
do
{ y_bisect = (y_lower+y_higher)/2.0;
f_bisect = characteristic(x,y_bisect);
if(f_bisect == 0.0)
{SUCCESS = 1;
root = y_bisect;
}
else if ((f_lower > 0.0 && f_bisect < 0.0)
          || (f_lower < 0.0 && f_bisect > 0.0))
     {root = 0.5*(y_lower+y_bisect);
     y_higher = y_bisect;
      f_higher = f_bisect;
     }
  else if ((f_higher > 0.0 && f_bisect < 0.0)
          || (f_higher < 0.0 && f_bisect > 0.0))
     { root = 0.5*(y_higher+y_bisect);
      y_lower = y_bisect;
      f_lower = f_bisect;
     }
abstol = y_higher - y_lower;
   }while(!SUCCESS && abstol> ERROR);
```

```
return root;
}
double characteristic(double x, double y)
{ Complex s;
Complex H_G;
double ans, tau_m,tau;
double Real, Img;
s.setImaginary(y);
s.setReal(x);
/* Calculate tau_m and tau */
if(0 <= y && y <= M_PI_2 )
tau_m = 0.5;
else if((M_PI_2) < y  && y < M_PI)
tau_m = (M_PI_2/y - 0.5);
tau =tau_m+1.65;
H_G = (s.power(2.0)+s*0.3684+0.1225)/(s.power(2.0)*(s.power(2.0)+0.03));
/* H_G = (s*2.0+1.0)/s.power(3.0);*/
Real = H_G.getReal();
Img = H_G.getImaginary();
ans = cos(y*tau) * (Img - exp(x)*(Real*sin(y) + Img *cos(y)))- sin(y*tau)
      * (Real-exp(x)*(Real*cos(y)-Img *sin(y)));
return ans;
}
double calcK(double x,double y)
{ Complex H_G,s;
double tau, tau_m, k;
double Real, Img;
s.setImaginary(y);
s.setReal(x);
```

```
/* Calculate tau_m and tau */
if(0 <= y && y <= M_PI_2 )
tau_m = 0.5;
else if((M_PI_2) < y  && y < M_PI)
tau_m = (M_PI_2/y - 0.5);
tau =tau_m+1.65;
H_G = (s.power(2.0)+s*0.3684+0.1225)/(s.power(2.0)*(s.power(2.0)+0.03));
/*H_G = (s*2.0+1.0)/s.power(3.0);*/
Real = H_G.getReal();
Img = H_G.getImaginary();
k = (exp(x*tau)*cos(y*tau))/(Real-exp(x)*(Real*cos(y)-Img*sin(y)));
return k;
}
%-------------complex.cc--------------------
#include <math.h>
#include "complex.hh"
/* Constructors/Destructors */
Complex::Complex(void)
{ this->x = (double) 0;
this->y = (double) 0;
}
Complex::Complex(const Complex &that)
{ this->x = that.x;
this->y = that.y;
}
Complex::Complex(double mag, double phase)
{ this->x = mag * cos(phase);
this->y = mag * sin(phase);
}
```

```
Complex::Complex(double x)
{ this->x = x;
this->y = (double) 0;
}
Complex::~Complex(void)
{ // empty function
}
/* operators */
Complex Complex::operator+(Complex that)
{ Complex ans;
ans.x = this->x + that.x;
   ans.y = this->y + that.y;
return ans;
}
Complex Complex::operator-(Complex that)
{ Complex ans;
ans.x = this->x - that.x;
ans.y = this->y - that.y;
return ans;
}
Complex Complex::operator*(Complex that)
{ Complex ans;
ans.x = this->x * that.x - this->y * that.y;
    ans.y = that.x * this->y + this->x * that.y;
return ans;
}
Complex Complex::operator/(Complex that)
{ Complex ans;
ans.x = (this->x * that.x + this->y * that.y)
```

```
        /(that.x * that.x + that.y * that.y);
ans.y = (this->y * that.x - this->x * that.y)
         /(that.x * that.x + that.y * that.y);
return ans;
}
Complex &Complex::operator+=(Complex that)
{ this->x = this->x + that.x;
this->y = this->y + that.y;
return *this;
}
Complex &Complex::operator*=(Complex that)
{ Complex ans(*this);
ans.x = this->x * that.x - this->y * that.y;
   ans.y = that.x * this->y + this->x * that.y;
this->x = ans.x;
this->y = ans.y;
return *this;
}
Complex Complex::operator+(double &that)
{ Complex ans;
ans.x = this->x + that;
ans.y = this->y;
return ans;
}
Complex Complex::operator-(double &that)
{ Complex ans;
ans.x = this->x - that;
ans.y = this->y;
return ans;
```

```
}
Complex Complex::operator*(double &that)
{ Complex ans;
ans.x = that * this->x;
ans.y = that * this->y;
return ans;
}
Complex Complex::operator/(double &that)
{ Complex ans;
ans.x = this->x / that;
ans.y = this->y / that;
return ans;
}
Complex &Complex::operator+=(double &that)
{ this->x = this->x + that;
return *this;
}
Complex &Complex::operator*=(double &that)
{ this->x *= that;
this->y *= that;
return *this;
}
Complex &Complex::operator=(double &that)
{ this->x = that;
this->y = 0;
return *this;
}
int Complex::operator==(Complex that)
{ if(this->x = that.x &&  this->y == that.y)
```

```
return 1;
else
return 0;
}
Complex Complex::power(double that)
{ Complex ans(pow(this->getMagnitude(),that), this->getPhase() * that);
return ans;
}
/* basic interface functions */
double Complex::getReal(void)
{ return x;
}
double Complex::getImaginary(void)
{ return y;
}
double Complex::getPhase(void)
{ return atan(y/x);
}
double Complex::getMagnitude(void)
{ return sqrt(x*x + y*y);
}
void Complex::setReal(double x)
{ this->x = x;
}
void Complex::setImaginary(double y)
{ this->y = y;
}
%--------------points.cc---------------------
#include<stdio.h>
```

```
#include "points.hh"
#include "complex.hh"
Points::Points(void)
{ this->next = 0;
this->e = 0;
}
Points::Points(Complex s, double e)
{ this->s = s;
this->next = 0;
this->e = e;
}
Points::Points(Complex s, Complex a, double e)
{ this->s = s;
this->next = 0;
this->e = e;
this->a = a;
}
Points::~Points(void)
{ if(this->next)
delete this->next;
}
Points *Points::add(Complex s, double e)
{ if(this->next)
return this->next->add(s,e);
else
return this->next = new Points(s,e);
}
Points *Points::add(Complex s, Complex a, double e)
{ if(this->next)
```

```
return this->next->add(s, a ,e);
else
return this->next = new Points(s, a, e);
}
Points *Points::find(Complex s)
{ Points *p;
for(p = this; p; p=p->next)
{
if(p->s == s)
return p;
}
return 0;
}
Points *Points::find(Complex s, double e)
{ Points *p;
for(p = this; p; p=p->next)
{
if(p->s == s && e == p->e)
return p;
}
return 0;
}
int Points::print(FILE *fp)
{
int c = 0;
Points *p;
for(p=this;p;p=p->next)
{
fprintf(fp,"\tA root is: %2.10lf + j%2.10lf,
```

```
at point %2.10lf + j%2.10lf, with error %2.10lf\n",
p->s.getReal(), p->s.getImaginary(), p->a.getReal(),
p->a.getImaginary(), p->e);
c++;
}
return c;
}   %----------------End-----------------------
```

Appendix D

Publications

1. "Design of a Wideband Low-power Continuous-time Sigma-delta Modulator in 90 nm CMOS Technology", Fang Chen, T. Kuendiger, S. Erfani, M. Ahmadi, *Analog Integrated Circuits and Signal Processing*, Springer ISSN 0925-1030(Print) Vol. 54, No. 3, pp 187-199, 2008.

2. "A Novel Digitally Controlled Low Noise Ring Oscillator",T. Kuendiger, Fang Chen, L. MacEachern, S. Mahmoud, *IEEE International Symposium on Circuits and Systems*, pp. 1016-1019, Seattle, WA, May 2008.

3. "Improved Direct Stability Analysis of High-Order Continuous-Time Sigma-Delta Modulators", Fang Chen, T. Kuendiger, S. Erfani, *IEEE North-East Workshop on Circuits and Systems*, pp. 73-76, Gatineau, QC, June 2006.

4. "Compensation of Finite GBW Induced Performance Loss on a Fourth-order Continuous-time Sigma-Delta Modulator", Fang Chen, T. Kuendiger, S. Erfani, *IEEE-Canadian Conference on Electrical and Computer Engineering*, pp. 1093-1096, Ottawa, ON, May 2006.

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