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Millimeter-Wave CMOS Digitally Controlled Oscillators for Automotive Radars

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By

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Declaration of Co-Authorship/Previous Publication

I. Co-Authorship

I hereby declare that this thesis incorporates material that is result of joint research. Chapters 2-6 of this thesis were completed under the supervision of Dr. Mitra Mirhassani. In all cases, the key ideas, primary contributions, experimental designs, data analysis, interpretation, statistical analysis, graphing results, and writing, were performed by the author. The contribution of my supervisor (the co-author) was primarily through the provision of checking and comments on the literature review, mathematical derivations, systems architectures, algorithms, providing feedback on refinement of ideas, editing of the manuscript, and advice on selecting peer reviewed journals for publication.

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II. Previous Publication

This thesis includes four original papers that have been previously published for publication in peer reviewed journals and conferences, as follows:

Thesis Chapter	**Publication title/full citation**	**Publication Status**
Chapter 2	I. Taha and M. Mirhassani,"A 24GHz Digitally Controlled Oscillator for Automotive Radar in 65nm CMOS",*in Proc.IEEE International Symposium on Circuits and Systems (ISCAS 2016)*", pp. 2767-2770, May. 2016	Published
Chapter 3	I. Taha and M. Mirhassani,"A 24 GHz DCO with High Amplitude Stabilization and Enhanced Start-up Time for Automotive Radar, *IEEE Transaction on Very Large Scale Integration (VLSI) Systems*",vol. 27, issue 10, pp. 2260-2271, Oct. 2019"	Published
Chapter 4	I. Taha and M. Mirhassani,"Impact of Process and Temperature Variations on the Design of CMOS Colpitts Oscillators", *in Proc. IEEE International Symposium on Signals, Circuits and Systems (ISSCS 2015)*", pp. 1-4, 2015	Published
Chapter 5	I. Taha and M. Mirhassani,"A Varactorless DCO with 7 GHz Tuning Range for 77 GHz Automotive Radars", *IEEE J. Access*",vol. 7, No. 1, pp. 72469-72481, Dec. 2019	Published

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Abstract

All-Digital-Phase-Locked-Loops (ADPLLs) are ideal for integrated circuit implementations and effectively generate frequency chirps for Frequency-Modulated-Continuous-Wave (FMCW) radar. This dissertation discusses the design requirements for integrated ADPLL, which is used as chirp synthesizer for FMCW automotive radar and focuses on an analysis of the ADPLL performance based on the Digitally-Controlled-Oscillator (DCO) design parameters and the ADPLL configuration. The fundamental principles of the FMCW radar are reviewed and the importance of linear DCO for reliable operation of the synthesizer is discussed. A novel DCO, which achieves linear frequency tuning steps is designed by arranging the available minimum Metal-Oxide-Metal (MoM) capacitor in unique configurations. The DCO prototype fabricated in 65 nm CMOS fulfills the requirements of the 77 GHz automotive radar. The resultant linear DCO characterization can effectivelly drive a chirp generation system in complete FMCW automotive radar synthesizer.

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List of Abbreviations

ACC	Automatic Cruise Control.
ADC	Analog to Digital Converter.
ADPLL	All Digital Phase Locked Loop.
CC-DCO	Colpitts Clapp Digitally Controlled Oscillator.
CMOS	Complementary Metal Oxide Semiconductor.
DCO	Digitally Controlled Oscillator.
DSP	Digital Signal Processing.
ECC-DCO	Enhanced Colpitts Clapp Digitally Controlled Oscillator.
EIRP	Effective Isotropic Radiated Power.
FCC	Federal Communications Commission.
FMCW	Frequency Modulated Continuous Wave.
FoM	Figure of Merit.
LRR	Long Range Radar.
mm-wave	millimeter-wave.
NMOS	Negative Metal Oxide Semiconductor.
MiM	Metal- Insulation-Metal.
ML-DCO	Monotonically Linear Digitally Controlled Oscillator.
MoM	Metal-oxide-Metal.
PMOS	Positive Metal Oxide Semiconductor.
PN	Phase Noise.
PVT	Process, Voltage, and Temperature.
RF	Radio Frequency.
SoC	System-on-Chip.
SRR	Short Range Radar.
TG	Transmission Gate.
TR	Tuning Range.
VCO	Voltage-Controlled-Oscillator.

Chapter 1

Introduction

Automotive sensors are mounted around vehicles to enable a 360° safety zone. While different types of driver assistance systems are proposed such as millimeter-wave (mm-wave), infrared, ultrasonic, and laser sensors, the mm-wave automotive sensor offers superior robustness against extreme weather environments such as rain, temperature, snow, and fog [1].

Pre-crash sensing, blind-spot detection, and collision avoidance are enabled by the usage of automotive Short Range Radar (SRR), which detects objects in the distance range of 0.15-30 m.

On the other hand, the automotive Long Range Radar (LRR) senses long distance range of 10-250 m and is primarily used for Automatic Cruise Control (ACC).

The Frequency Modulated Continuous Wave (FMCW) method is usually utilized in automotive radar transceivers. FMCW radar relies on the accuracy of the frequency modulation for a continuously transmitted signal to measure the target properties, which calls for a linear frequency sweep to measure the range and velocity of objects [2]. The accuracy of the measurement in FMCW radar depends on the linearity of the generated frequency sweep of the frequency synthesizer. Non-linearity in the sweeping range widens and shifts the peaks along the frequency

axis, which introduces a systematic bias in distance estimation and increases the estimation variance [2].

1.1 Motivation

Unlike other traditional radar schemes, which use pulses and operate in the lower GHz range, The mm-wave bands of the automotive radar are located near 24 GHz (K-band) or 77 GHz (W-band). FMCW radar for the K- or W-bands offers much smaller form factors. Shorter wavelength allows for the deployment of multiple independent links in close proximity. The wavelength of the W-band (77 GHz) is smaller than that of the K-band 24 GHz automotive radar. Further integration is allowed driven by the significant reduction in the wavelength, which leads to a more compact size [3].

The low cost and the potential for System-on-Chip (SoC) integration make CMOS an appealing technology [4]. The increasing demand for compact, power efficient, and low cost automotive radar as driven by the advances in silicon technology have motivated research on SoC realizations. Automotive radar synthesizers and transceivers in CMOS have been reported in [1], [3], [5], [7], [8].

Digitally intensive or digitally assisted RF architectures are becoming attractive for realizing mm-wave frequency synthesizers. All-Digital-Phase-Locked-Loop (AD-PLL) manifest itself as an attractive system architecture. The analog loop-filter of the analog PLL is transformed to a digital one, which allows full integration and provide scalability with the technology. Moreover, the total loop parameter such as loop bandwidth and phase margin can be reconfigured via programming internal digital registers that adjust the performance and control operation mode [5], [6], [10], [11].

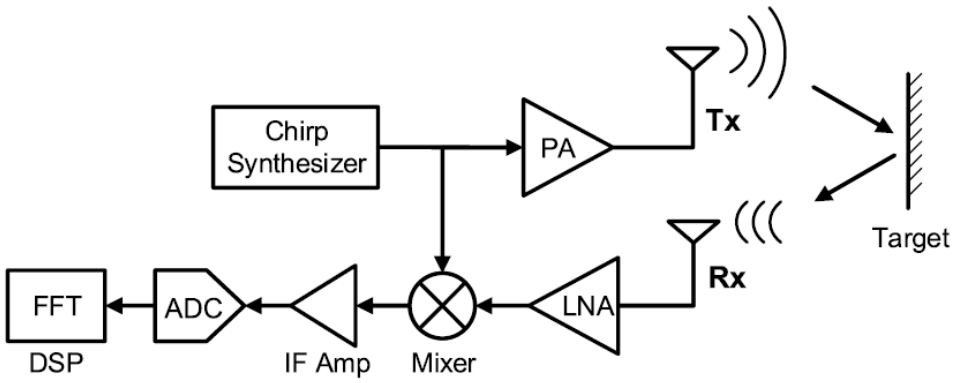

FIGURE 1.1: FMCW radar system.

While the analog PLLs still dominates the mm-wave range. However, ADPLLs for the mm-wave applications still suffer from low in-band phase noise or rely on extensive calibration circuitry. [12], [5], [8].

1.2 FMCW Radar

Fig. 1.1 shows the block diagram of a complete FMCW radar system. FMCW signal is generated by the chirp synthesizer and the power amplifier (PA) feeds the output to the transmit antenna (Tx). The receive antenna (Rx) picks up the returned signal, which is then mixed with the synthesizer output to generate the beat frequency. The baseband is digitized by the Analog-to-Digital (ADC) convertor and the Digital Signal Processing (DSP) back-end performs an FFT on the digitized signal to determine the beat frequencies, which is needed to calculate the distance and the velocity of the target.

Phase-locked loop generates frequency chirps for FMCW radar that continuously transmits a signal whose frequency is linearly modulated during the measurement. Sawtooth chirp is a commonly used chirp profile. It is shown in Fig. 1.2. The propagation delay between the transmitted and the received signals due to the round trip is observed. If the target is moving relative to the radar, the received

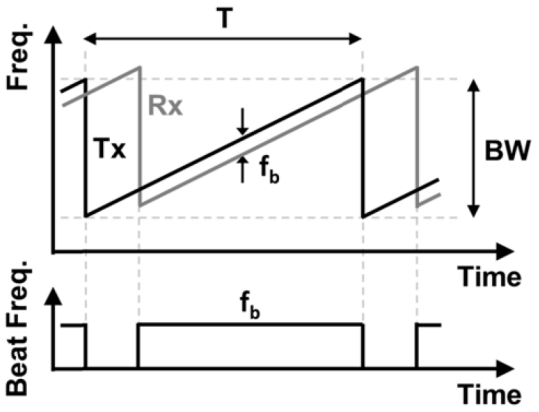

FIGURE 1.2: Triangular FMCW Chirp.

signal frequency experiences a Doppler shift. The target range and velocity are measured being related to the resultant offset frequency between the transmitted and the received signal, which is referred to as the beat frequency. For the sawtooth profile in Fig. 1.2, the beat frequency is expressed as :

$$f_b = \frac{2R}{c}.\frac{BW}{T} + f_d \tag{1.1}$$

where R, BW, c, T, and f_d denote the target range, the chirp modulation bandwidth, the speed of light, the modulation period, and the Doppler frequency respectively [9].

A sequence of chirps with different ramp slopes are transmitted to unambiguously resolve the range R and the relative velocity $v = cf_d/2f_c$. f_c is the center frequency of the chirp.

The range and velocity resolutions are derived and expressed as [5], [13]:

$$\Delta R = \frac{c}{2BW} \tag{1.2}$$

$$\Delta v = \frac{c}{2f_c}\frac{1}{T} \tag{1.3}$$

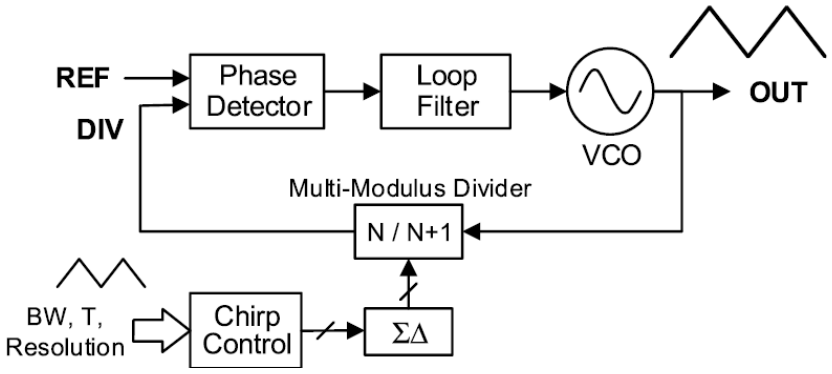

FIGURE 1.3: FMCW synthesizer based on fractional-N PLL with chirp control.

Accordingly, large modulation bandwidth is required for fine range resolution, whereas the velocity resolution can be improved with longer chirp period.

Although Eqs. (1.2) and (1.3) describe the ideal resolution that can be achieved, the actual values are further limited by other factors that includes the overlap of the transmitted and the received chirps due to the time gating to discard highly nonlinear chirp segments near the turnaround points, signal propagation delay, and most importantly, chirp non-linearity [12].

1.3 Chirp Linearity

FMCW radar accuracy is based on the premise that the chirps are perfectly linear so that the beat frequencies accurately represent the parameters of the detected targets.

PLL bandwidth is a key, which needs to be optimized for achieving high chirp linearity. The PLL division ratio in Fig. 1.3 approximates the chirp waveform with a stair-like signal.

This modulation is discrete in output value and time. The PLL bandwidth must be large enough to allow the PLL to follow the trajectory of the ideal linear chirp profile. Therefore, the required bandwidth should be far greater than the

chirp modulation frequency. At the same time, PLL settling must not be so fast to let the PLL output frequency to follow the stepped modulation signal too closely. Therefore, the PLL bandwidth should to be less than the stepping rate of the modulation signal. Consequently, an optimized loop bandwidth satisfies the following inequalities [12]:

$$\frac{1}{T} << BW_{PLL} < \frac{2^{lin}-1}{T/2} \tag{1.4}$$

where lin are the number of bits denoting the chirp resolution. Therfore, the modulation signal comprises 2^{lin} output quantization levels. The stepping rate is descibed as a function of the chirp resolution.

Delicate balance must be maintained between different trade-offs to maintain the stringent requirements on the PLL loop design including settling response and precise bandwidth. The VCO/DCO gain variations across wide frequency range translated to non-linearity imposes a challenge to maintain constant loop properties. Moreover, linearity in the modulation can be hindered by the large changes in the loop properties during frequency modulation [14], [15].

Several approaches are developed to mitigate the PLL/ADPLL bandwidth variation caused by non-linearity in the VCO-DCO.

Typically, non-linearity exists in the DCO transfer function that calls for calibration. The work in [8] introduces digital calibration techniques to mitigate DCO non-linearity by monitoring the frequency error and calculating the gradient of DCO frequency. One tuning bank only is activated at a time while the next bank is enabled based on the convergence direction. The process is repeated across all the tuning banks until the frequency error is diminished.

The FMCW ramp linearity in [5] is improved by reducing the fine tuning step of the DCO and utilizing auto-calibration to linearize the multi-bank DCO tuning curve. Distributed metal capacitor is used to provide ultra-small capacitance for

the fine-tuning bank of mm-wave DCO, which they developed in [17]. However, for such an ultra fine tuning, the width and the height of the metal stubs beneath the inductor become analogous. Therefore, the coupling between adjacent stubs can not be ignored. To keep linear capacitor step, the width of the stubs needs to be optimized through Electromagnetic (EM) simulation. EM simulation is costly in terms of time. Besides, the precision of the EM simulator is curial.

The VCO frequency response is linearized in [15] using averaging varactors. A combination of PMOS and NMOS varactors are proposed in [16] to linearize the VCO gain. However, both Linearization techniques are quite delicate and can be easily degraded with temperature or process variations.

In standard structures the DCO gain exhibits non-linearity and varies substantially throughout the tuning range. Therefore, the conversion gains of the DCO require continuous calibration in the background [6]

While a typical value of the DCO gain error across the tuning range that can be considered is about 20% [5], the complexity of the digital calibration techniques to mitigate DCO non-linearity varies among the reported designs [8], [5], [18], [19].

1.4 Objectives

The objective for this research is to design an mm-wave DCO capable of addressing FMCW radar requirements. The success of the proposed system will allow mm-wave circuits to be realized on digital CMOS technology, which can effectivelly reduces the implementation cost in the field of automotive IC sensor design.

Varactor-less realization of mm-wave DCO is aimed to reduce the design complexity and eliminates the trade-off between wide and linear tuning range requirements.

1.5 Dissertation Structure

- Chapter 2 presents the design Digitally Controlled Oscillator (DCO) with a tuning-range and phase-noise that is able to address Short Range Radar (SRR) requirements. In order to overcome the major challenge to design a wide tuning range DCO, proper oscillator topology is chosen, specific tuning mechanism is implemented, and design optimization strategies are employed without degrading the Phase Noise (PN) performance.

- Chapter 3 investigates design strategies to enhance the performance for implementation of a CMOS DCO presented in 2. Design methodology is developed for the enhanced DCO, which is based on an in-depth mathematical analysis of the start-up condition and amplitude of oscillation.

- Chapter 4 presents a study of temperature and process sensitivity in CMOS Colpitts oscillator. Based on the analysis of linear and non-linear models, temperature and process sensitivity is derived. By defining the process and temperature sensitivity parameters early in the design process, unnecessary design iteration is prevented, and time-to-market is reduced.

- Chapter 5 presents varactor-less DCO with a new tuning structure that is proposed and realized for the first time. Since the proposed DCO provides linear tuning steps, it impacts the generation of linear frequency modulation for the FMCW radar.

- Chapter 6 highlights the summary of this work, conclusions and the future work.

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Chapter 2

A 24GHz Digitally Controlled Oscillator for Automotive Radar in 65nm CMOS

2.1 Introduction

As the CMOS technology scales down, digital architectural solutions for RF systems become increasingly preferred over their analog counterparts to minimize production cost. Very high speed transistors are available therefore making it feasible to integrate Radio Frequency (RF) electronics with digital processing. Digital intensive approaches facilitate a high level of integration to realize System-on-Chips (SoCs) implementations. A DCO is one of the digital architectural solutions to replace the analog Voltage-Controlled-Oscillators (VCOs) circuitry. Instead of having an analog voltage controlling the frequency tuning in the VCO, the DCO frequency is controlled digitally. DCOs are the heart for All-Digital-Phased-Locked-Loops (ADPLLs) [1] and all digital transmitters as a stand-alone block without the PLL [2].

SRR automotive technology enables road safety via collision avoidance, pre-crash sensing, and blind-spot detection [3]. A single chip CMOS radar SRR is desirable for reduced production cost. The FCC allows the $24GHz$ automotive SRR to operate between $22GHz-29GHz$. The wide SRR band enables high range resolution (ΔR). If for example ΔR is $10cm$, using the equation $\Delta R = c/B$, where B is the bandwidth, and c is the speed of light, a bandwidth of $3GHz$ is required. DCOs for automotive SRR mandate a wide tuning range and low PN [4]. Colpitts VCO can offer lower PN and a wider tuning range when compared to the conventional cross-coupled LC tank VCO [5] [6] [7] [8]. However, the stability condition varies across the tuning range imposing the main problem to fulfill wide tuning range requirements. The oscillation condition can be kept constant across the tuning range by employing a Clapp VCO at the expense of limited tuning range [9]. The Colpitts-Clapp VCO was proposed in [10] to increase the tuning range as a hybrid between the Colpitts and the Clapp.

Automotive radar receivers in [6] [11] implement VCOs in SiGe while the proposed CC-DCO is a DCO in CMOS. The work in [10] reported a SiGe mm-wave VCO for automotive radar as well. However, the tuning range was widened using a special varactors available in Infeneon's SiGe production technology. CMOS DCOs for wireless applications were reported in [12] [13] to realize digital synthesizers, but they were based on the conventional LC tank oscillator. Road safety and automotive radar application is a recent research field. DCO for FMCW automotive radar was reported in [4], however, it was based on the conventional LC tank oscillator as well.

In this work, a potential tuning mechanism is discussed to maximize the tuning range for a CC-DCO. In order to prove the concept, a $24GHz$ CC-DCO with a 29% tuning range is designed in $65nm$ CMOS process. To the best of author's knowledge, CC-DCO has not been employed in CMOS to widen the tuning range for automotive radar in most of this prior work.

This chapter is organized as follows. Section II shows the derivation of the negative resistance linear model for the CC-DCO while tuning parameters are investigated. Section III presents the implemented CC-DCO, the design parameters, and the simulation results followed by the conclusion.

2.2 Colpitts-Clapp Design Aspects

2.2.1 Colpitts-Clapp Linear Model

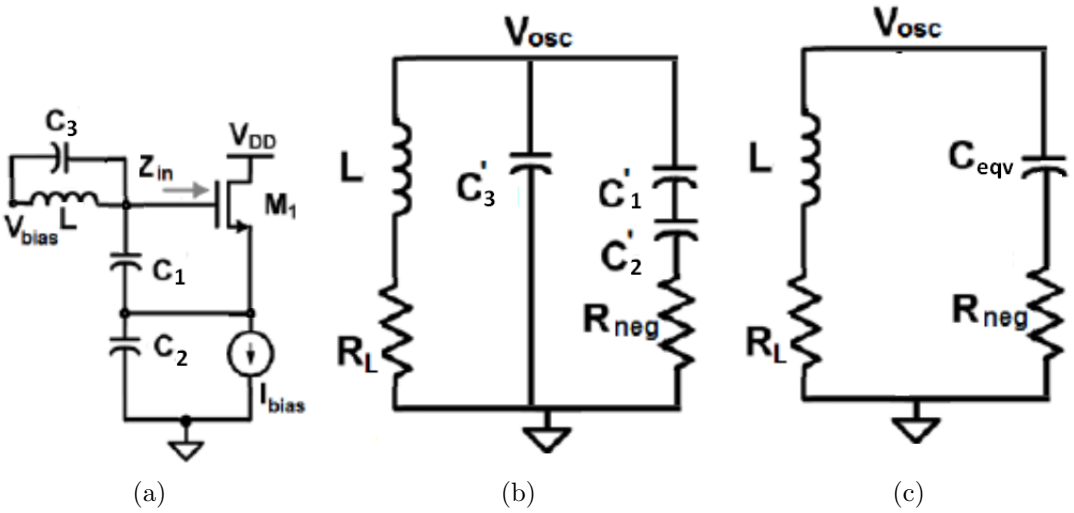
A common-drain Colpitts-Clapp oscillator is shown in Fig. 2.1(a). This topology provides an increase in the tuning range by adding another capacitor in parallel with the inductor [8]. The lossy inductor is modeled as an inductor (L) in series with a parasitic series resistance (R_L). Since the quality factor of the integrated capacitors can be high, the lossy serial resistance associated with $C_{1,2,3}$ can be neglected [14]. The linear model used to describe the oscillator is a negative resistance based model. The impedance (Z_{in}) looking into the gate of M_1 is:

$$Z_{in} = \frac{1}{SC_1'} + \frac{1}{SC_2'} - \frac{g_m}{\omega^2 C_1' C_2'} \tag{2.1}$$

The negative resistance is denoted by:

$$R_{neg} = -\frac{g_m}{\omega^2 C_1' C_2'} \tag{2.2}$$

where g_m is the small signal transconductance of M_1, C_1'= C_1+C_{gs}; C_2'= C_2+C_{sb}. Fig. 2.1(b) shows the negative resistance generator (Z_{in}) in parallel with the lossy inductor and C_3'. C_3'= C_3+C_{gd}. C_{gs}, C_{sb}, and C_{gd} are the parasitic capacitors of M_1. Let C_s' be the equivalent series capacitance of C_1' and C_2'. Converting C_s' in series with R_{neg} to its parallel representative give $C_p' = C_s' Q_{C_s'}/(1 + Q_{C_s'}^2) \cong C_s'$ for high $Q_{C_s'}$, and $R_{neg,p} = R_{neg}(1 + Q_{C_s'}^2)$. Let $C_{eqv} = C_3' || C_p'$. $C_{eqv} || R_{neg,p}$ can



(a) (b) (c)

FIGURE 2.1: Colpitts-Clapp oscillator in common-drain configuration. (a) Schematic of the oscillator. (b) Negative resistance generator (Z_{in}) in parallel with L and C_3. (c) Negative resistance linear model.

be converted back to a series representative. Having $C_{eqv,s} = (1 + Q^2_{C_{eqv}})/Q^2_{C_{eqv}} \cong C_{eqv}$ and $R_{neg,s} = R_{neg,p}/(1 + Q^2_{C_{eqv}}) \cong R_{neg}$, the linear model for Colpitts-Clapp oscillator is shown in Fig. 2.1(c). The negative resistance generator formed by R_{neg} in series with C_{eqv} exhibit the reflection coefficient (Γ_G) greater than 1 to enforce instability. At the frequency of oscillation, L resonates with C_{eqv} having:

$$f_{osc} = \frac{1}{2\pi\sqrt{L(C'_3 + \frac{C'_1 C'_2}{C'_1 + C'_2})}} \tag{2.3}$$

$$C_{eqv} = C'_3 + \frac{C'_1 C'_2}{C'_1 + C'_2} \tag{2.4}$$

The start-up requires that $\mid R_{neg} \mid > R_L$. It can be expressed as:

$$\left| \frac{g_m}{\omega^2_{osc} C'_1 C'_2} \right| > R_L \tag{2.5}$$

2.2.2 Tuning Range

Equation (2.3) holds for Colpitts oscillators if $C_3 = 0$. C_3 is the tuning capacitor in Clapp, while both of C_2 and C_3 are the tuning capacitors in Colpitts-Clapp oscillator. The Tuning Range (TR) is defined as $(f_{max} - f_{min})/f_{center}$ [9]. The frequency range Δf_{osc} is $f_{max} - f_{min}$. Therefore, f_{max} is a function of $C_{eqv,min}$ and f_{min} is a function of $C_{eqv,max}$. Ideally, the larger the tuning capacitor and Δf_{osc} is, the wider the tuning range becomes. By maximizing C_1/C_2 ratio with $C_1 > C_2$, equation (2.4) can be approximated as:

$$C_{eqv} \approx C_3' + C_2' \tag{2.6}$$

If $C_2' = C_3'$ in (2.6), then the effective tuning capacitor is doubled as compared to Clapp topology that just depends on C_3 for tuning. In fact the condition of maximizing C_1/C_2 is also mandatory to satisfy low PN requirements [15]. In this work, a simultaneous tuning mechanism is proposed such that part of C_2 and C_3 are equated, and the condition of $C_1 > C_2$ is valid. Let:

$$C_2' = C_{f2} + C_{sb} + C_{t,coarse} \tag{2.7}$$

$$C_3' = C_{f3} + C_{gd} + C_{t,coarse} \tag{2.8}$$

where $C_{t,coarse}$ is the coarse tuning effective capacitance, and $C_{f,2}$, $C_{f,3}$ are the fixed part of C_2, C_3 respectively. The tuning capacitors C_2 and C_3 should remain greater than the parasitic capacitors that appear in parallel with it, otherwise, the tuning capacitor looses its tuning functionality. Since $C_{gd} > C_{sb}$, then in order to maintain $C_2' = C_3'$ to double the tuning capacitance, C_{f2} should be greater than $C_{f,3}$ by a minimum of $C_{gs} - C_{sb}$. This is a second condition for wide Δf_{osc}.

Equation (2.3) can be simply written as:

$$f_{osc} = \frac{1}{2\pi\sqrt{LC_{eqv}}} \tag{2.9}$$

The derivative of f_{osc} with respect to C_{eqv} is given by $\delta f_{osc}/\delta C_{eqv} = -f_{osc}/2C_{eqv} \approx \Delta f_{osc,min}/\Delta C_{eqv,min}$. Where $\Delta C_{eqv,min}$ is the minimum tuning step that can generate minimum frequency step $\Delta f_{osc,min}$. Thus:

$$\Delta C_{eqv} = \Delta f_{osc} \frac{1}{\delta f_{osc}/\delta C_{eqv}} \tag{2.10}$$

For a specific f_{osc}, Δf_{osc} and ΔC_{eqv} are the fine frequency and capacitor steps respectively. ΔC_{eqv} is constrained by the minimum available size varactor or capacitor in the process. Large tuning range and fine resolutions calls for separate and overlapped tuning capacitance banks to avoid matching difficulties [13]. Separate intermediate and fine tuning mechanisms can be provided as part of C_{f2} retaining Colpitts tuning operation for a certain value of $C_{t,coarse}$, and equation (2.7) is modified to:

$$C_2' = C_{2,fixed} + C_{2,intermediate} + C_{2,fine} + C_{sb} + C_{t,coarse} \tag{2.11}$$

2.3 Design and Simulation

In order to verify the concept, fully differential CC-DCO is designed using TSMC $65nm$ RFIC models. The schematic is shown in Fig. 2.2. The single-ended based analysis presented in Section II can be applied to the differential topology as a half circuit representation.

Minimum width of $M_{1,2}$ should satisfy the required g_m for start-up condition in equation (2.5). $M_{1,2}$ should also be biased to provide a current density of

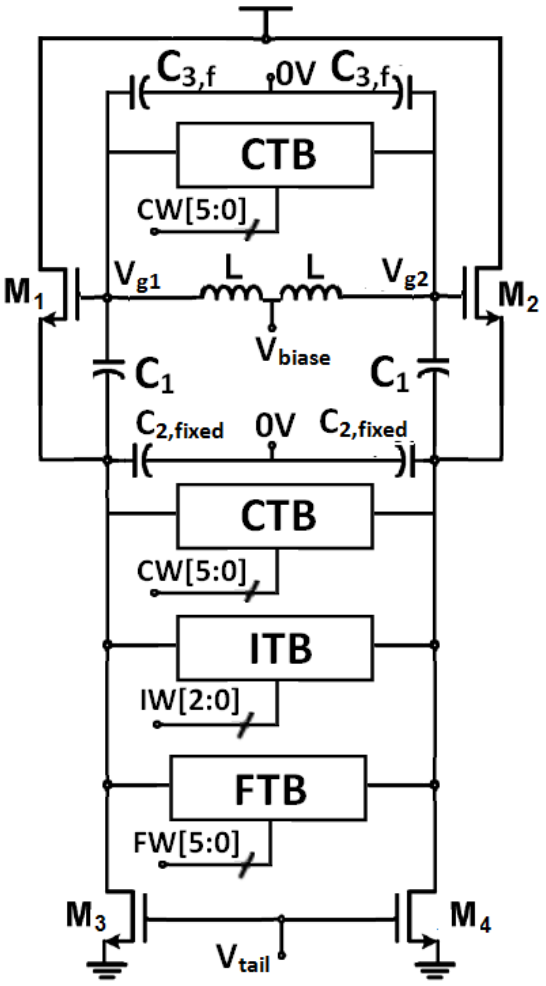
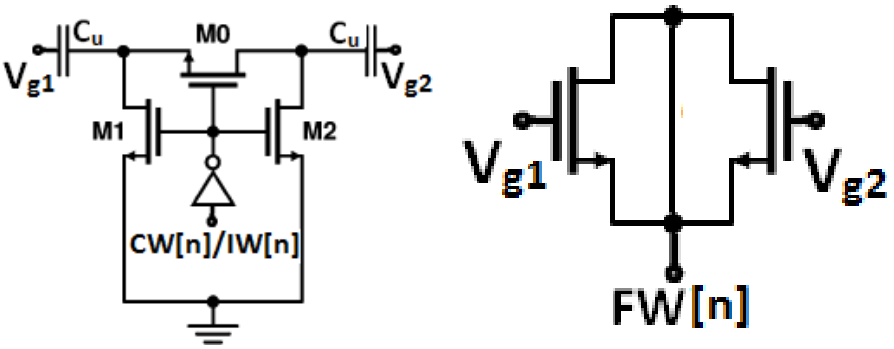


FIGURE 2.2: Colpitts-Clapp digitally controlled oscillator.



(a) (b)

FIGURE 2.3: Unit capacitance cells. (a) CTB and ITB unit cell. (b) FTB unit cell.

$0.15mA/\mu m$ for low PN requirements [9]. The biasing current of $5mA$ is provided by $M_{3,4}$ which are designed with $1\mu m$ channel length to reduce flicker noise that can degrade the PN performance. The inductor L is a $88.3pH$ single turn spiral inductor, having quality factor of 22.3. Two identical Coarse Tuning Banks (CTBs), an Intermediate Tuning Bank (ITB), and a Fine Tuning Bank (FTB) are formed. CTBs and ITB are implemented using binary-weighted Metal-oxide-Metal (MoM) capacitors controlled by a 6-bit Coarse Word (CW[5:0]) and 3-bit Intermediate Word (IW[2:0)] respectively. FTB is implemented using a binary-weighted varactors rather than MoM to provide small ΔC_{eqv}. A 6-bit Fine Word (FW[5:0]) is used to control the FTB. The implemented unit capacitance cells are similar to [16]. Fig. 2.3(a) shows the switched capacitor cell for CTB and ITB. Each cell consists of two identical binary-weighted MoM capacitors connected differentially by a series and two pull-down CMOS switches. Fig. 2.3(b) shows the unit varactor based cell for the FTB. Table 2.1 shows the values of the designed parameters.

Cadence analog design environment is used for simulation using a $65nm$ TSMC models. Fig. 2.4(a) shows the simulated coarse tuning range that extends from $22GHz$ to $29GHz$. Fig. 2.4(b) shows a coarse tuning step of $140MHz$. The intermediate tuning range is $202MHz$ and the intermediate step is $41MHz$ as shown in Fig. 2.4(c). The Fine tuning range is $84MHz$ and the fine step is $1.6MHz$ as in Fig. 2.4(d) and (e). The intermediate range covers 1.4 times the coarse tuning step while the fine tuning range covers 2 times the intermediate step to provide overlapping between the tuning banks which avoids frequency gaps. SpectreRF is used to simulate the CC-DCO phase noise. The PN at $1MHz$ offset from a $24GHz$ is $-187dBc/Hz$ as shown in Fig. 2.4(e).

Table 2.2 presents the CC-DCO performance along with that of previously published CMOS DCOs. Figure of Merit for Tuning range (FoM_T) is defined as:

$$FoM_T = PN - 20log\frac{f_{center}}{\Delta f_{osc,min}} - 20log\frac{TR\%}{10\%} + 10log\frac{PDC}{1mW} \tag{2.12}$$

TABLE 2.1: CC-DCO Design Parameters

Device	**Size**
$M_{1,2}$	$33\mu m/60nm$
$M_{3,4}$	$33\mu m/1\mu m$
L (Spiral)	1 turn Area: width=$188\mu m$, length=$181\mu m$
C_1 (MOM)	W/finger=$100nm$, array=$8X8$, multiply=180
$C_{2,fixed}$ (MOM)	W/finger=$100nm$, array=$8X8$, multiply=78
$C_{3,f}$ (MOM)	W/finger= $100nm$, array=$8X8$, multiply=6
CTB (MOM)	W/finger=$100nm$, array=$8X8$, multiply=$1, 2, 4, 8, 16, 32$
ITB (MOM)	W/finger=$100nm$, array=$8X8$, multiply=$1, 2, 4$
FTB (AMOS)	$240nm/240nm$, multiply=$1, 2, 4, 8, 16, 32$

Where P_{DC} is the power dissipation of the CC-DCO. The CC-DCO achieves the highest tuning range with best-in-class phase noise.

2.4 Conclusions

In this chapter, a tuning mechanism is discussed to widen the tuning range of a $24GHz$ DCO for SRR applications. Phase noise performance has been carefully considered. Tuning range of 29% is achieved by employing Colpitts-Clapp topology, deriving the required design equations, varying two potential capacitor banks simultaneously, and refining the results through simulation. The CC-DCO is designed using Cadence design tool with the available $65nm$ component RF models. Pnoise setup with SpectreRF is used to simulate the PN for the implemented design. The simulated phase noise for a $24GHz$ CC-DCO is better than $-187dBc/Hz$ at $1MHz$ offset frequency.

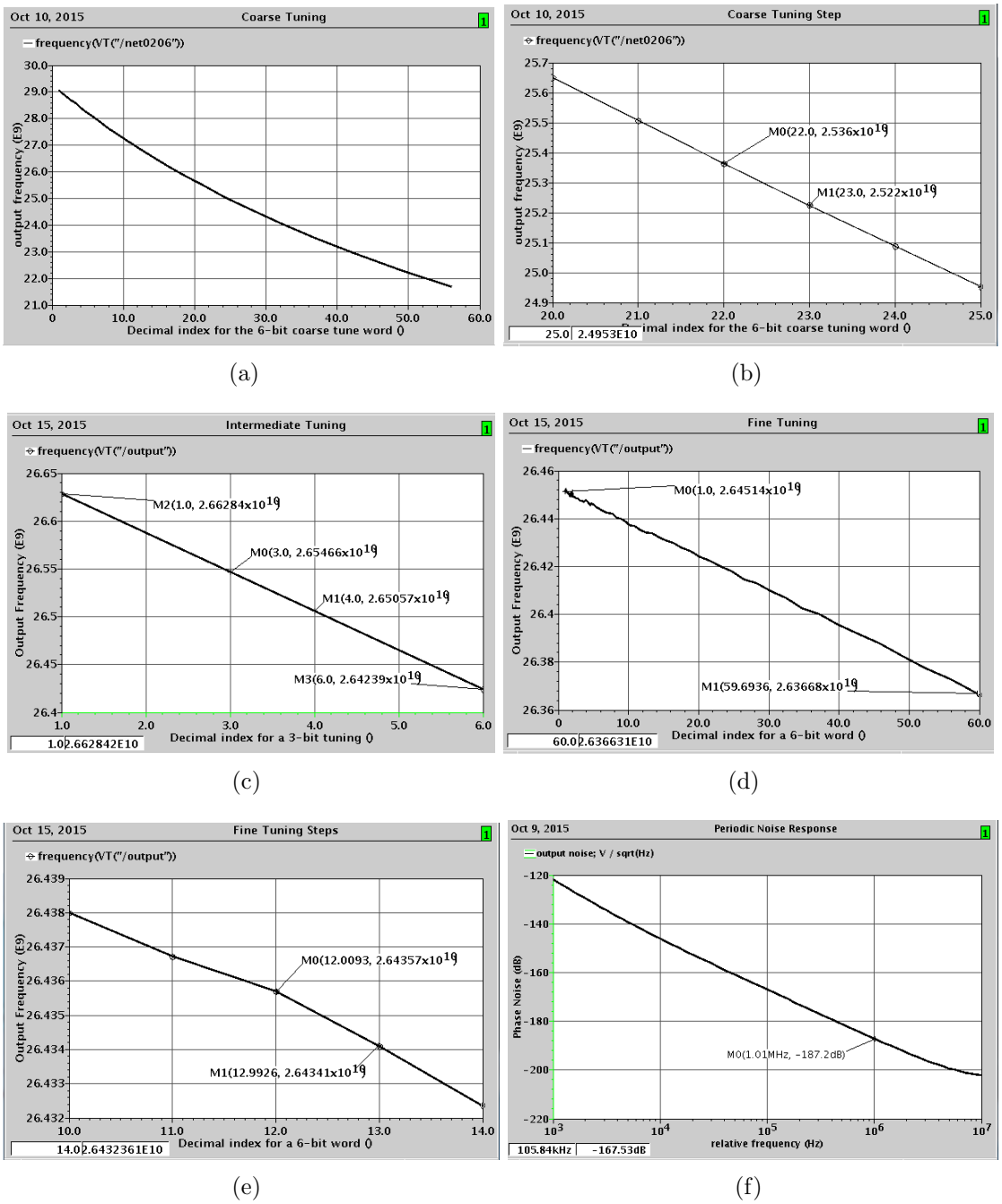


FIGURE 2.4: Simulation results of the CC-DCO. (a) coarse tuning. (b) coarse tuning step. (c) intermediate tuning. (d) fine tuning. (e) fine tuning step. (f) phase noise spectrum.

TABLE 2.2: Comparison of Relevant CMOS DCOs

Ref.	[12]	[2]	[13]	[4]	**This work**
f_{center} (GHZ)	60	2.2	3.15	60	24
TR (%)	10%	3.18%	22.2%	11.6%	29%
$\Delta f_{osc,min}$ (MHZ)	0.160	7	0.012	1.64	1.6
PN (dBc/Hz)	-93 @$1MHz$	-121 @$0.1MHz$	-123 @$1MHz$	-140 @$1MHz$	-186 @$1MHz$
PDC (mW)	12	1.3	9.84	13.2	10
FoM_T (dBc/Hz)	-177	-180	-228	-221	-268
Tech.	$90nm$	$65nm$	$65nm$	$65nm$	$65nm$

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Chapter 3

A 24 GHz DCO with High Amplitude Stabilization and Enhanced Start-up Time for Automotive Radar

3.1 Introduction

Automotive Short Range Radar (SRR) contributes to road safety via pre-crash sensing, blind-spot detection, and collision avoidance [1]. Based on the Federal Communications Commission (FCC) regulations, an automotive SRR is allowed to operate in the frequency range of $22 - 29\ GHz$ [2].

Range resolution (ΔR) is a key requirement of the Frequency-Modulated Continuous-Wave (FMCW) for Short Range Radars, and it depends on the transmitter bandwidth and TR of the local oscillator. The Bandwidth (B) and ΔR are related by $\Delta R = c/B$, where c is the speed of light.

Ultra Wide Band SRR (5 GHz) requires hard range resolution. For such a wide frequency range, amplitude-to-phase conversion needs to be avoided [3]. The amplitude of oscillation and consequently the transmitted output power for the SRR is restricted by the Effective Isotropic Radiated Power (EIRP) of $-41.3\ dBm/MHz$.

The quality factor (Q) of the switched tuning capacitors is sharply degraded in higher frequencies and therefore the overall Q_{tank} is reduced. In order to compensate for the losses, large transistors are required to provide sufficient transconductance. However, the parasitic capacitors of the large transistors impose loading effect and hence affect the TR of the VCO [4]. Therefore, achieving low PN and wide TR simultaneously is challenging.

Unlike ring and relaxation oscillators used at low frequencies for few GHz [5, 6], high frequency oscillators are employed based on highly selective resonator to prevent noise from outside the bandwidth from degrading the PN [9].

A 24 GHz Colpitts VCO with 30% TR was reported in [7]. The work in [8] showed the design of a 30 GHz common-drain Colpitts oscillator. Negative resistance was improved by employing a parasitic cancellation technique. Although the start-up condition was satisfied over a TR of 15.9%, it was based on 0.2 GaAs pHEMT technology which required access to specialized and more costly fabrication process.

However, the steady state oscillation condition for the Colpitts VCO varies across the TR. This condition is kept constant across the TR by employing a Clapp VCO at the expense of limited TR [9]. In order to increase the TR, the Colpitts-Clapp topology was proposed in [10].

VCOs and DCOs for SRR mandate low PN and wide TR [10]. The start-up condition and the amplitude of oscillation in Colpitts Clapp VCOs are functions of the tuning element that can impose difficulties for a design with wide TR requirements [11]. Moreover, the increased reliability factor of the transistor reduced sizes is 2

to 3 times the minimum initially estimated size [9]. The process and temperature variations necessitate extra frequency tuning margins. Furthermore, increasing the device size increases the parasitic capacitors by the same factor, limiting the minimum size of the tuning capacitor, and consequently the maximum possible achieved frequency [8].

The work in [12] employs a special resonator based topology to realize an mm-wave VCO, which relaxes the start-up requirement and stabilizes the amplitude. However, the start-up condition enhancement and amplitude stabilization trade-off with the TR. The reported TR was limited to 1.7%.

In [13], a Colpitts oscillator was designed to work as a frequency reference. A high sheet poly resistor with negative temperature coefficient was used in a constant g_m biasing circuitry. The amplitude was stabilized against temperature variations. However, the TR of this work was limited to 0.625%.

The swing and the start-up were enhanced in [14] for Colpitts VCO by replacing the tail current source with an inductor. However, amplitude stability throughout the TR was not discussed, and the TR for the VCO was limited to 2.5%.

In [15], a CC-DCO was proposed for SRR, which did not require any special fabrication process and was implemented using the conventional CMOS technology.

In this work, a more thorough detailed analysis of this modified topology is derived. The CC-DCO suitable for automotive SRR is designed using the TSMC 65 nm CMOS process. A negatively boosted structure is employed, which increases the amplitude without the need to increase the tail current, and stabilizes the amplitude across the wide TR. Moreover, it relaxes the restriction on the value of the transconductance that is required to start up the CC-DCO. To the best of author's knowledge, a DCO with boosted amplitude and relaxed start-up transconductance has not been employed in CMOS for automotive radar prior to this work. The proposed design methodology takes into consideration these effects

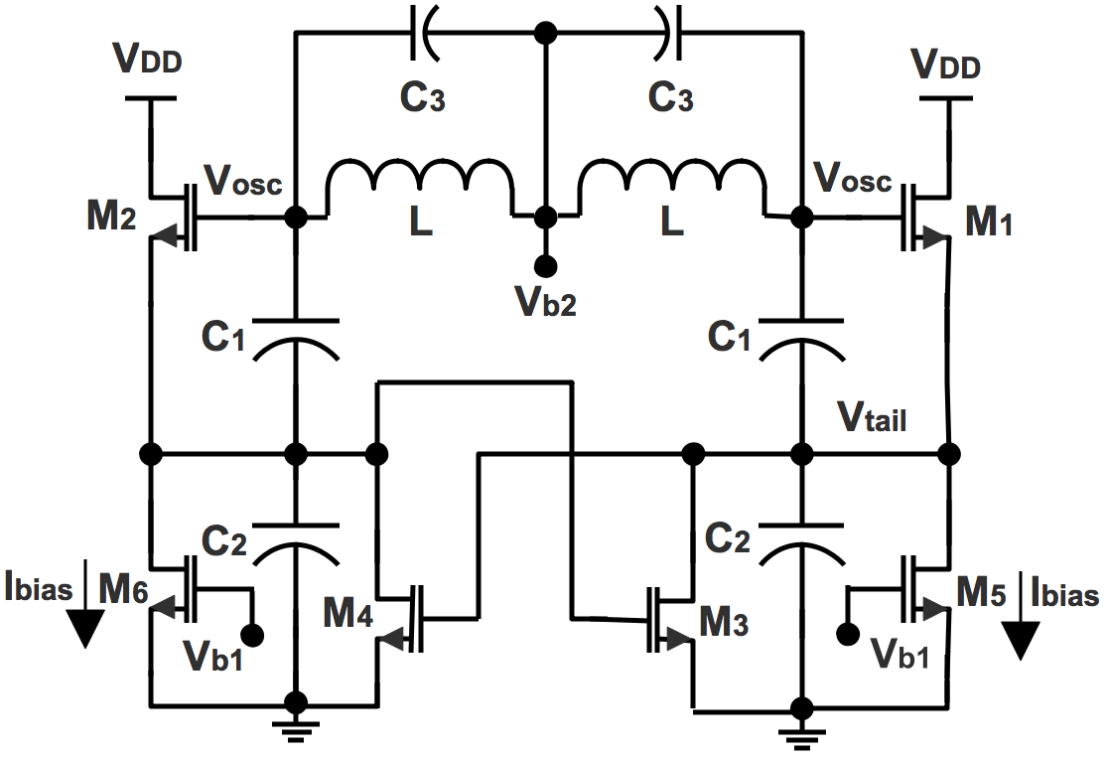


FIGURE 3.1: Differential Enhanced Colpitts Clapp-DCO (ECC-DCO) schematic.

at an early stage of the design, in order to reduce the start-up time and to stabilize the amplitude across the TR. The proposed methodology is geared toward the design of a CC-DCO for use in automotive radars.

The rest of this chapter is organized as follows. Section 3.2 presents the small-signal and the large-signal derivations of the negative resistance-based models that are used to describe the behavior of the oscillator at the onset and the steady state of oscillation. The TR is discussed in section 3.3. The amplitude stability analysis is provided in Section 3.4. Section 3.5 presents the design aspects and the design methodology. The design parameters and pre-layout simulation results are shown in Section 3.6. The post-layout simulation results are shown in Section 3.7 followed by the conclusion in Section 3.8.

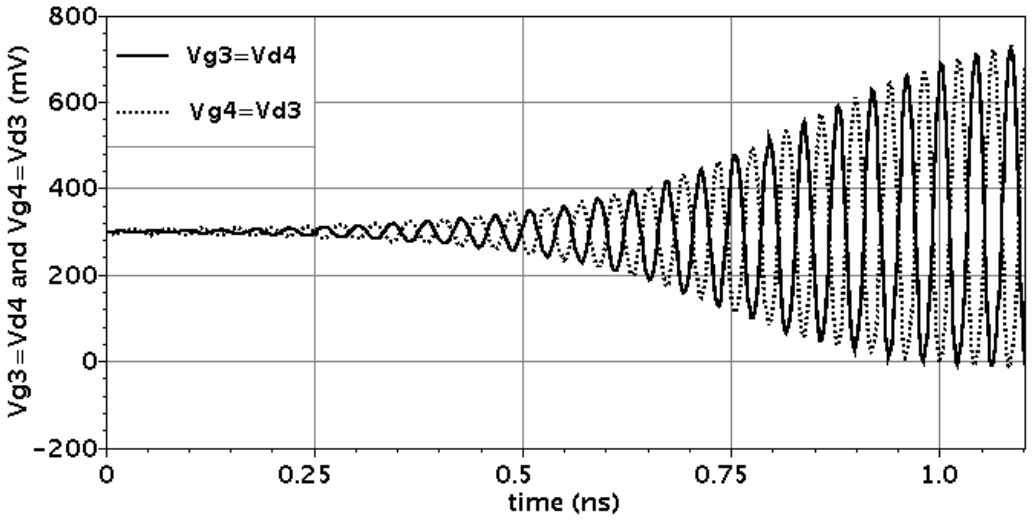


FIGURE 3.2: Simulated Start-up waveforms for the ECC-DCO.

3.2 Colpit-Clapp and CMOS Enhanced Models

The structure of the proposed ECC-DCO is shown in Fig. 3.1. It is a differential common-drain Colpitts oscillator with a negative resistance boosting mechanism and extra capacitors in parallel with the inductors to increase the TR. This has been achieved by employing double tuning capacitors that are comprised of C_3 and part of C_2. The remaining part of C_2 provides the intermediate and the fine-tuning. Differential Colpitts based topology can be analyzed using half circuit representation [14].

3.2.1 ECC-DCO Start-Up Negative Resistance Model

Referring to Fig.3.1, the behavior of M_3,M_4 at the start-up differs from that at the steady oscillation state. The V_{osc} at the onset of oscillation is practically zero and V_{tail} biasing $= V_{gs3,4} = V_{ds4,3}$.

Fig. 3.2 shows the gate and drain signals of M_3,M_4 throughout the start-up till the oscillation grows-up to be steady. With just the biasing is being applied to the

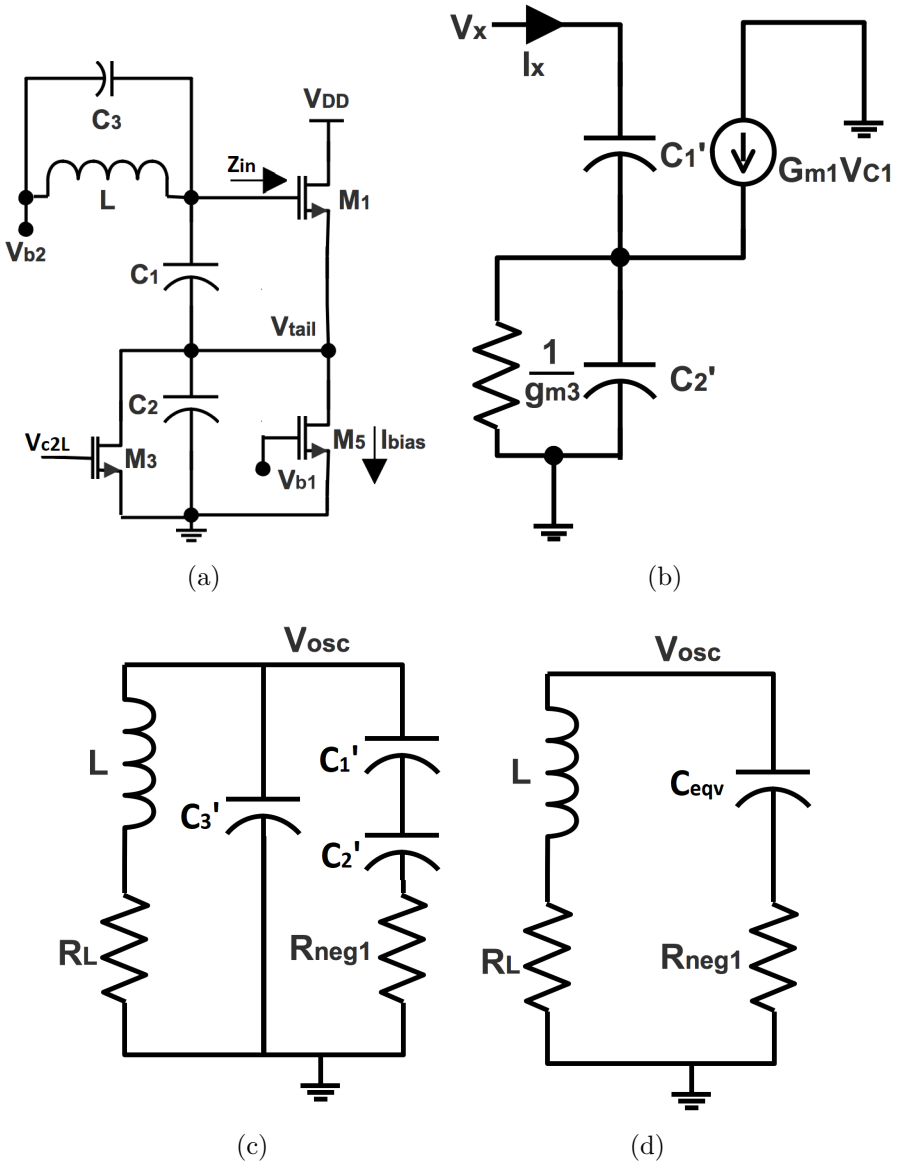


FIGURE 3.3: Reduced circuits used to derive the ECC-DCO negative resistance small-signal model for analyzing the start-up condition. (a) The half circuit representation of the differential ECC-DCO. (b) The small-signal impedance model looking into the gate of M_1. (c) The derived small signal impedance in parallel with L and C_3'. (d) The negative resistance based model for the ECC-DCO at the start-up.

circuit, $V_{g3} \approx V_{d3}$ and $V_{g4} \approx V_{d4}$ at the start-up. Thus, M_3,M_4 behave like diode connected devices and can be modeled as resistors with a value of $1/g_{m3}$, where g_{m3} is the small signal transconductance of M_3.

Fig. 3.3(a) is the half-circuit representation of the ECC-DCO. The input impedance (Z_{in}), looking into the gate of M_1 at the onset of oscillation is derived using the model in Fig. 3.3(b). The integrated capacitors $C_{1,2}$ are implemented in 65 nm CMOS technology with high-quality factor. Thus, the lossy serial resistances associated with $C_{1,2}$ are ignored [16]. Moreover, the intrinsic output resistance and second order effect are neglected for getting an intuitive analysis.

Applying KVL and KCL, V_x in Fig. 3.3(b) can be written as:

$$V_x = \frac{I_x}{sC_1'} + \frac{1}{sC_{2,E}'}\left[I_x + \frac{g_{m1}I_x}{sC_1'} - \frac{V_x - \frac{I_x}{sC_1'}}{\frac{1}{g_{m3}}}\right] \tag{3.1}$$

$$Z_{in} = \frac{V_x}{I_x} \cong \frac{1}{j\omega C_1'} + \frac{1}{j\omega C_{2,E}'} - \frac{g_{m1} + g_{m3}}{\omega^2 C_1' C_{2,E}'} \tag{3.2}$$

The negative resistance is denoted by:

$$R_{neg1} = -\frac{g_{m1} + g_{m3}}{\omega^2 C_1' C_{2,E}'} \tag{3.3}$$

where g_{m1} is the small signal transconductance of M_1 and:

$$C_1' = C_1 + C_{gs1} \tag{3.4}$$

$$C_{2,E}' = C_2 + C_{sb1} + C_{db3} + C_{db5} + C_{gs4} \tag{3.5}$$

where C_{gs}, C_{sb}, and C_{gd} are the parasitic capacitors associated with the transistors. Eq. (3.2) shows that Z_{in} is equivalent to series combination of C_1', $C_{2,E}'$ and R_{neg1}. This input impedance, Z_{in}, in parallel with the lossy inductor and C_3' is shown in Fig. 3.3(c), where

$$C_3' = C_3 + C_{gd1} \tag{3.6}$$

The lossy inductor is modeled as an inductor (L) in series with a parasitic series resistance (R_L). If C_1' in series with $C_{2,E}'$ is equal to C_s', then C_s' in series with R_{neg1} can be converted to a parallel combination of C_p' and $R_{neg,p}$.

For high $Q_{C'_s}$, $C'_p = C'_s Q^2_{C'_s}/(1+Q^2_{C'_s}) \cong C'_s$ and $R_{neg,p} = R_{neg1}(1+Q^2_{C'_s})$. Let $C_{eqv} = C'_3||C'_p$. The parallel combination of C_{eqv} and $R_{neg,p}$ can be converted back to an equivalent series representation. The series resistor and capacitor are $R_{neg,s} = R_{neg,p}/(1+Q^2_{C_{eqv}}) \cong R_{neg1}$ and $C_{eqv,s} = ((1+Q^2_{C_{eqv}})/Q^2_{C_{eqv}})C_{eqv} \cong C_{eqv}$.

Fig. 3.3(d) is the negative resistance based model for the ECC-DCO at the start-up, where $C_{eqv,E}$ is given by:

$$C_{eqv} = C'_3 + \frac{C'_1 C'_{2,E}}{C'_1 + C'_{2,E}} \tag{3.7}$$

Instability is enforced at the start-up when $\mid R_{neg1} \mid > R_L$ [17], such that:

$$\frac{g_{m1} + g_{m3}}{\omega^2_{osc} C'_1 C'_{2,E}} \geq R_L \tag{3.8}$$

At the frequency of oscillation, L resonates with C_{eqv} and $\omega_{osc} = 2\pi f_{osc}$ is given by:

$$\omega_{osc} = \frac{1}{\sqrt{L(C'_3 + \frac{C'_1 C'_{2,E}}{C'_1 + C'_{2,E}})}} = \frac{1}{\sqrt{LC_{eqv}}} \tag{3.9}$$

The resistance $R_{L,P}$ is the equivalent parallel resistance of the R_L, such that $R_{L,P} = R_L(1+Q^2_L) \cong R_L Q^2_L$, where Q_L is the quality factor of L.

Since $Q_L = \frac{\omega_{osc} L}{R_L}$ and $Q_L \gg 1$, $R_{L,P}$ can be expressed as:

$$R_{L,P} \cong R_L Q^2_L = \omega_{osc} L Q_L \tag{3.10}$$

By substituting the R_L by $\omega_{osc}L/Q_L$, multiplying both sides by $R_{L,P}$, replacing $R_{L,P}$ at the right side of the inequality by (3.10), replacing ω_{osc} by (3.9), and substituting C_{eqv} by (3.7), a modified startup condition is obtained as follows:

$$g_{m,E} R_{L,P} \geq \frac{C'_1 C'_{2,E}}{(C'_3 + \frac{C'_1 C'_{2,E}}{C'_1 + C'_{2,E}})^2} \tag{3.11}$$

where $g_{m,E} = g_{m1} + g_{m3}$ is the effective initial transconductance for the ECC-DCO.

The Eq. (3.11) relates the required $g_{m,E}$ to the tuning and the parasitic capacitors.

The largest value of $C_{2,E}$ can not exceed C_1 as constrained by PN requirements [9]. On the other hand, $C'_3 \approx C'_2$ following the simultaneous tuning mechanism design constraints [15]. Therefore, if $C'_1 = C'_2 = C'_3$, the start-up condition requirement can be expressed as a multiplication of the effective initial transconductance and the $R_{L,P}$, as follows:

$$g_{m,E} R_{L,P} \geq \frac{4}{9} \tag{3.12}$$

Eq. (3.12) can be used to design M_1 and M_3 in order to satisfy the start-up requirements, taking into considerations the losses of the tank and the effect of the associated parasitic capacitors.

3.2.2 CC-DCO Start-Up Negative Resistance Model

The start-up negative resistance model is similar to Fig. 3.3(d). However, $C_{eqv,C}$ replaces C_{eqv} and $g_{m3} = 0$. The capacitor $C_{eqv,C}$ can be defined using Eq. (3.7) by replacing $C'_{2,E}$ with $C'_{2,C}$, where:

$$C'_{2,C} = C_2 + C_{sb1} + C_{db5} \tag{3.13}$$

The negative resistance is:

$$R_{neg2} = -\frac{g_{m1}}{\omega_{osc}^2 C'_1 C'_{2,C}} \tag{3.14}$$

Instability is enforced at the start-up when $\mid R_{neg,2} \mid > R_L$. Comparing (3.3) with (3.14) shows that if, as an example, g_{m1}=g_{m3} and $C'_{2,E}$= $C'_{2,C}$, then the absolute value of the start-up negative resistance is doubled in the ECC-DCO and start-up time of the ECC-DCO is lower than that of the CC-DCO.

An alternative start-up requirements, similar to Eq. (3.11) and (3.12) can be obtained by substituting $g_{m3} = 0$, which results in:

$$g_{m1}R_{L,P} \geq \frac{C'_1 C'_{2,C}}{(C'_3 + \frac{C'_1 C'_{2,C}}{C'_1 + C'_{2,C}})^2} \tag{3.15}$$

$$g_{m,C}R_{L,P} \geq \frac{4}{9} \tag{3.16}$$

where $g_{m,C} = g_{m1}$ is the initial transconductance required for the CC-DCO.

If L and M_1 for the CC-DCO and the ECC-DCO are identical, then comparing (3.12) with (3.16) shows that $g_{m,E}$ is stronger. The comparison also shows that the CC-DCO demands higher g_{m1} than the ECC-DCO that requires larger M_1. Increasing the size of M_1 increases C_{gd1} that causes larger C'_3. Even $C'_{2,E}$ has additional parasitic capacitors as compared to $C'_{2,C}$, the larger parasitic capacitors associated with C'_1 and C'_3 for the CC-DCO due to larger M_1 can make C_{eqv} and $C_{eqv,C}$ comparable.

3.2.3 CC-DCO Large Signal Model

Non-linearity due to large signal forces the V_{osc} from increasing while the oscillation continues steadily. By assuming that the average current of the Colpitts switching transistor is equal to the biasing current, the function model in [18] approximates $I_1 \approx 2I_{bias}$, where I_1 is the peak of I_{d1} that appears as a train of pulses.

The describing function for the large signal transconductance (G_m) can be defined as the ratio of the peak pulse current to the amplitude of V_{gs} for the switching transistor, and is equal to:

$$G_{m1} \approx \frac{I_{1,peak}}{V_{C1}} \approx \frac{2I_{bias}}{V_{C1}} \approx \frac{2I_{bias}}{nV_{osc}} \tag{3.17}$$

where I_{bias} is the biasing current for M_1.

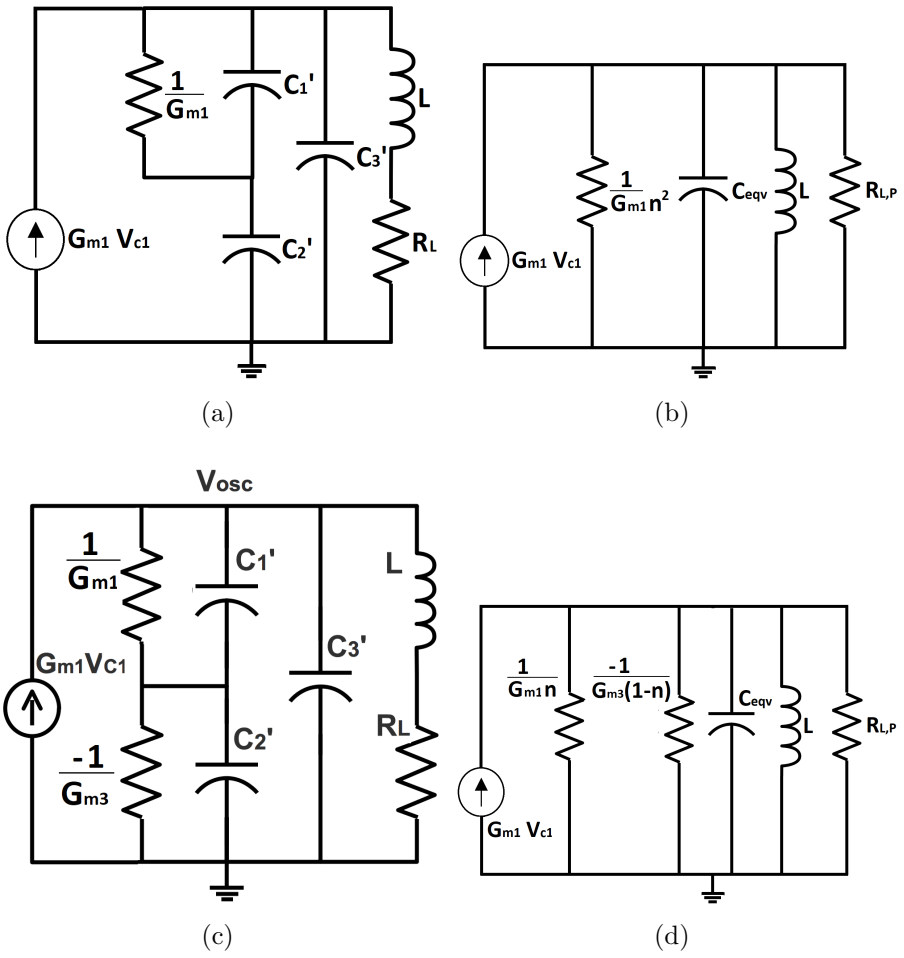


FIGURE 3.4: Steps to derive large signal models for the CC-DCO and the ECC-DCO. (a) Circuit to derive the large signal CC-DCO model. (b) CC-DCO large signal model. (c) Circuit to derive the large signal ECC-DCO model. (d) ECC-DCO large signal model.

With $n = C_2'/(C_1' + C_2')$, V_{C1} is related to V_{osc} by the relation:

$$V_{C1} = nV_{osc} \tag{3.18}$$

Large signal model for amplitude approximation is constructed by using the T model to represent M_1 and replacing g_m by G_m.

The large signal model of the CC-DCO is shown in Fig. 3.4(a). The resistor $1/G_{m1}$ and the tapped capacitors C_1' and $C_{2,E}'$ can be converted to a resistor of $1/G_{m1}n^2$ in parallel with a series combination of C_1' and $C_{2,E}'$ [11]. Fig. 3.4(b) shows the

final model after this transformation. Since C_3' appears in parallel with the series combination of C_1' and $C_{2,E}'$, then the total capacitor is C_{eqv}. The total resistance (R_{total}) is $(1/G_{m1}n^2)\|R_{L,P}$.

At f_{osc}, V_{osc} for the CC-DCO is given by:

$$V_{osc} = 2I_{bias}R_{total} = 2I_{bias}\frac{R_{L,P}}{1 + G_{m1}n^2R_{L,P}} \tag{3.19}$$

By substituting (3.17) in (3.19) and arranging the terms, the output amplitude for the CC-DCO is given by:

$$V_{osc} = 2I_{bias}R_{L,P}(1 - n) = 2I_{bias}R_{L,P}\frac{C_1}{C_1 + C_2} \tag{3.20}$$

The amplitude of oscillation for the CC-DCO in (3.20) varies across the TR by the variation of C_2.

3.2.4 ECC-DCO Large Signal Model

Referring to Fig. 3.1, When the swing at the gate of M_1 is maximum, the swing at the gate of M_2 is minimum, M_3 is turned off, and M_4 is turned on. As V_{g1} starts to drop-down from its maximum value and V_{g2} shoot-up from its minimum level, M_4 conducts current. M_3 conducts peak current in an opposite way. Such that the peak of I_{d3} occurs while V_{g2} is shooting-up and V_{g1} is falling-down.

The average current in M_1,M_2 is equal to the summation of I_{bias} and the average current in M_3,M_4. Since the switching transistors (M_1,M_2) and the cross-coupled transistors (M_3,M_4) conduct in the opposite directions, then the peak of the train of current pulses flowing in the switching transistors can still be approximated to be $2I_{bias}$ and the large signal transconductance can still be approximated by Eq. (3.17).

The opposite polarities of large signals at the gates of cross-coupled devices generate a negative resistance to be seen between the device gates. We may define G_{m3},G_{m4} to be the large signal transconductance for M_3,M_4. Thus, the cross-coupled connected devices M_3,M_4 generate a negative resistance of $-2/G_{m3}$,$-2/G_{m4}$ seen between the gates of M_3 and M_4. It is equivalent to a negative resistance of $-1/G_{m3}$,$-1/G_{m4}$ looking into the gate of M_3,M_4.

Fig. 3.4 (c) is the basic circuitry used to derive the large signal model to describe the amplitude. The transistor M_1 is replaced by an equivalent T model and G_{m1} replaces g_{m1}. The resistors $1/G_{m1}$ and $-1/G_{m3}$ appear in parallel with C_1' and C_2' respectively. By substituting $1/G_{m1} = R_1$ and $-1/G_{m3} = R_2$, the equivalent impedance (Z_{eqv}) for the series combination of $C_1' \| R_1$ and $C_{2,E}' \| R_2$ can be expressed as:

$$Z_{eqv} = \frac{(C_1' + C_2')R_1R_2 + \frac{1}{s}(R_1 + R_2)}{sC_1'C_2'R_1R_2 + C_1'R_1 + C_2'R_2 + \frac{1}{s}} \tag{3.21}$$

At high frequency, $1/s \cong 0$, and therefore the Z_{eqv} is modified as follows:

$$Z_{eqv} \cong \frac{1}{sC_s + \frac{1}{R_2/(\frac{C_1'}{C_1'+C_2'})} + \frac{1}{R_1/(\frac{C_2'}{C_1'+C_2'})}} \tag{3.22}$$

where C_s is the series combination of C_1' and C_2'.

The equivalent impedance (Z_v) for a parallel combination of two typical resistors, R_4 and R_5, and a capacitor C_s can be expressed as:

$$Z_v = \frac{1}{sC_s + 1/R_4 + 1/R_5} \tag{3.23}$$

By comparing (3.22) with (3.23), the series combination of $R_1 \| C_1'$ and $R_2 \| C_{2,E}'$ can be transformed to $R_4 \| R_5 \| C_s$, where:

$$R_4 = \frac{R_2}{C_1'/(C_1' + C_{2,E}')} = \frac{-1}{G_{m3}(1-n)} \tag{3.24}$$

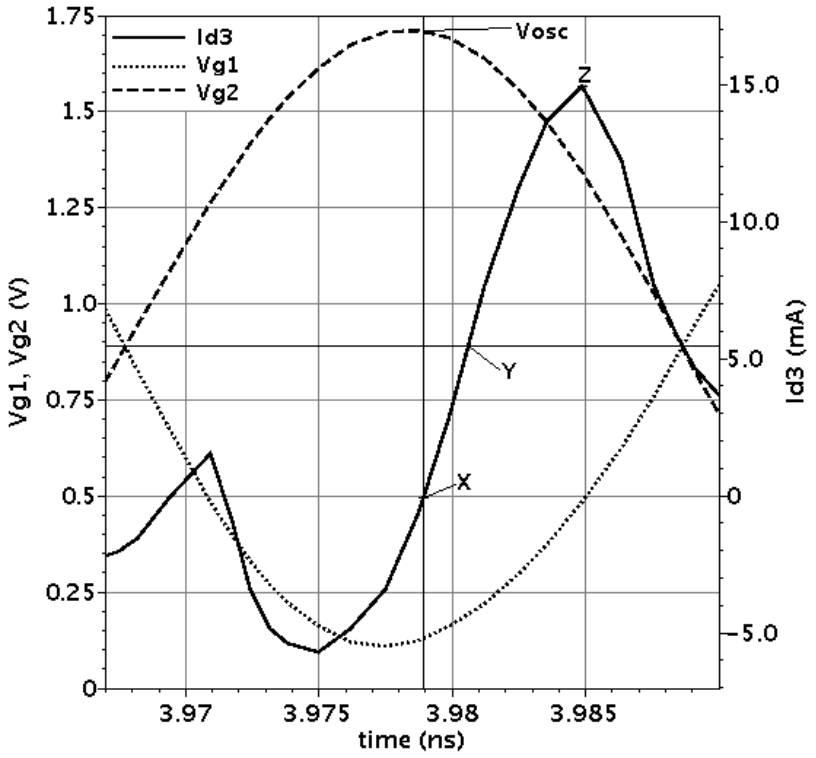


FIGURE 3.5: Simulated drain current of M_3 (I_{d3}) and the oscillating output voltages at the gates of M_1 (V_{g1}) and M_2 (V_{g2}).

$$R_5 = \frac{R_1}{C'_{2,E}/(C'_1 + C'_{2,E})} = \frac{1}{G_{m1}n} \tag{3.25}$$

Fig. 3.4(d) shows the final large signal model after the transformation. The total output resistance R_{total} is the parallel combination of $1/nG_{m1}$, $-1/G_{m3}(1-n)$, and $R_{L,P}$. At f_{osc}, V_{osc}=$2I_{bias}R_{total}$, and can be expressed as:

$$V_{osc} = 2I_{bias}\frac{1}{\frac{1}{R_{L,P}} + nG_{m1} - (1-n)G_{m3}} \tag{3.26}$$

If, as an example, $C_1 = C_2$ and $G_{m1} = G_{m3}$, then for a given I_{bias} and $R_{L,P}$, the ECC-DC amplitude in (3.26) is twice of that of the CC-DCO in (3.20). Moreover,

Eq. (3.26) shows that increasing G_{m3} increases V_{osc}. Since, PN is inversely proportional to the square of V_{osc}, thus larger amplitude is mandatory to satisfy low PN requirements [19].

The derived equations (3.8), (3.9), (3.11), (3.12), (3.14), (3.16), (3.20), and (3.26) contribute to the design methodology and explain the small-signal and large-signal behavior.

3.3 Tuning Range

The TR is equal to $(f_{max} - f_{min})/f_{center}$. Referring to Eq. (3.9) f_{max} and f_{min} correspond to $C_{eqv,min}$ and $C_{eqv,max}$, respectively. The Simultaneous tuning mechanism in [15] equates parts of C_2 with C_3 for the coarse tuning while maximizing the ratio of C_1/C_2 such that:

$$C_2 = C_{2,f} + C_{2,intermediate} + C_{2,fine} + C_{t,coarse} \tag{3.27}$$

$$C_3 = C_{3,f} + C_{t,coarse} \tag{3.28}$$

where $C_{t,coarse}$, $C_{2,intermediate}$, and $C_{2,fine}$ are the coarse, intermediate, and fine tuning effective capacitance, $C_{2,f}$ and $C_{3,f}$ are the fixed part of C_2 and C_3 respectively that are comparable to the associated parallel parasitic capacitors in addition to layout parasitic capacitors.

For $C_{2,min}$ to effectively tune the maximum frequency, it should remain greater than the parasitic capacitors. Increasing the fixed part of capacitance C_2 ($C_{2,f}$), to account for the parasitics, lowers the maximum tuned frequency that may mandate decrease L to retain the maximum frequency.

Moreover, increasing $C_{2,f}$ is constrained by the PN requirements; a low PN requires maximizing C_1' and the ratio of (C_1'/C_2') [9].

3.4 Amplitude Stability Analysis

The oscillation frequency is sensitive to the output amplitude and reduced oscillation amplitude degrades the PN and better PN performance can be achieved by suppressing amplitude-to-phase conversion [12]. Referring to Eq. (3.26), if the following condition holds

$$C_2 G_{m1} = C_1 G_{m3} \tag{3.29}$$

then the amplitude of oscillation for the ECC-DCO can be expressed as:

$$V_{osc} = 2 I_{bias} R_{L,P} \tag{3.30}$$

This means that the amplitude of oscillations could be independent of tuning capacitors, yet it depends on Q_L as related in (3.10).

Since G_{m3} is the large signal transconductance, a special function could be derived to describe it due to the non-linearity associated with large signal behavior.

TABLE 3.1: CC/ECC-DCOs Corner Analysis Results

Design	**$W_{1,2}$, $W_{5,6}$, R** $(\mu m, \mu m)$	**C_2, C_3** (fF)	**Corner**	**Freq.** (GHz)	**Amp.** (mV)	**Start-up time** (nS)	**I_{avrg}** (mA)
ECC1	20, 20, 2	434, 140	typ.	24.04	661	1.6	8.79
			f.b.	26.01	898	0.8	10.48
			s.w.	22.32	283	15	7.04
ECC2	30, 30, 2	412, 117	typ.	24.09	863	0.9	12.66
			f.b.	25.82	1090	0.6	15.24
			s.w.	22.53	595	2	10.39
CC1	20, 20	434, 140	typ.	failed	failed	failed	-
			f.b.	27.36	604	2.1	9.14
			s.w.	failed	failed	failed	-
CC2	40, 40	450, 155	typ.	24.09	616	1.7	14.1
			f.b.	26.2	806	0.9	16.45
			s.w.	22.29	225	7.2	12.5

Fig. 3.5 shows the transient response of I_{d3} along with the oscillating voltages at V_{g1} and V_{g2}, which appear as $(1-n)V_{g2}$ and $(1-n)V_{g1}$ at the gate and the drain of

M_3 respectively. The transistors, M_3,M_4 are designed using low threshold devices. The transistor M_3 conducts and carries positive drain current when V_{g2} is decreasing in the upper half and V_{g1} is increasing in the lower half of the corresponding sinusoidal waveform.

The drain current of Transistor M_3, I_{d3}, overshoots from 0 mA at X to a maximum current at Z when the sinusoidal waveform of V_{g2} starts to drop from its maximum value. The G_{m3} is related to the large current change during the conduction cycle that is associated with V_{gs} change. By approximating the slope of $XZ \approx$ the slope of XY, G_{m3} could be approximated by the ratio of ΔI_{d3} to ΔV_{g3} of the segment line XY. The coordinates (I_d, V_{gs}) of the point X are $I_{d3} = 0$ mA and V_{g3} with an amplitude of $(1-n)V_{osc}$. The point Y lies on the same horizontal line where V_{g1} and V_{g2} cross each other. The crossing point corresponds to the DC biasing point. Therefore, the coordinates (I_d, V_{gs}) of the point Y correspond to the M_3 biasing current I_{b3} and voltage V_{b_3}. The biasing voltage V_{b3} is a fraction of V_{osc}. Let $V_{osc} = f(1-n)V_{osc}$, where f is a fraction factor that is < 1.

Since $V_Y < V_X$, then G_{m_3} is a negative value and related to the dynamic of operation. Therefore, G_{m3} and its absolute value can be described as:

$$G_{m3} = \frac{I_Y - I_X}{V_Y - V_X} = -\frac{I_{b3}}{(1-n)V_{osc}(1-f)} \tag{3.31}$$

$$|G_{m3}| = \frac{I_{b3}}{(1-n)V_{osc}(1-f)} \tag{3.32}$$

Substitution of (3.32) and $G_{m1} \approx \frac{2I_{bias}}{nV_{osc}}$ from (3.17) in (3.29) result in:

$$I_{b3} = 2I_{bias}(1-f) \tag{3.33}$$

The result in Eq. (3.33) reveals that I_{b3} is proportional to I_{bias}. The maximum value of I_{b3} can be set to be equal to I_{bias} with $f = 0.5$, for the design to be justified, while the optimum value is determined by the required G_{m3} considering

the amplitude stability in Eq. (3.29) and verifying the start-up condition in Eq. (3.8).

It should be noted that the slope approximation depends on the biasing condition, and it varies with the class of operation. Moreover, the shape of the current depends on closeness of the frequency of the oscillation to the transistor transit frequency (f_T). Although the approximations are crude, they are useful by providing an intuitive link between the biasing current of the cross-coupled transistor and the tail biasing current.

If the condition represented in Eq. (3.29) is satisfied, then $R_{L,P}$ is the only parameter that can affect the amplitude stability across the TR, since as shown in Eq. (3.10) it changes with the frequency.

In order to investigate the amplitude stability with the TR, ω_{osc} is modified by $\Delta\omega_{osc}$ with $\omega_{osc} \gg \Delta\omega_{osc}$. Since $R_{L,P}$ is related to ω_{osc} in Eq. (3.10), then:

$$R'_{L,P} \cong R_L Q_L^2 = (\omega_{osc} + \Delta\omega_{osc}) L Q_L \tag{3.34}$$

$V'_{osc} = 2I_{bias}R'_{L,P}$ and the normalized amplitude for the ECC-DCO can be expressed as:

$$\frac{V'_{osc}}{V_{osc}} = \frac{(\omega_{osc} + \Delta\omega_{osc})^2}{\omega_{osc}^2} = 1 + 2\frac{\Delta\omega_{osc}}{\omega_{osc}} + \frac{\Delta\omega_{osc}^2}{\omega_{osc}^2} \tag{3.35}$$

If ω'_{osc} is associated with the incremental increase in $C'_{eqv} = C_{eqv} + \Delta C_{eqv}$, then the ratio of $\frac{(\omega_{osc}+\Delta\omega_{osc})^2}{\omega_{osc}^2}$ is equal to $\frac{C_{eqv}}{C_{eqv}+\Delta C_{eqv}}$, and can be expressed as:

$$(1 + \frac{\Delta\omega_{osc}}{\omega_{osc}})^{-2} = 1 + \frac{\Delta C_{eqv}}{C_{eqv}} \tag{3.36}$$

Since $\frac{\Delta\omega_{osc}}{\omega_{osc}} \ll 1$, the left side of Eq. (3.36) can be approximated by first-order Taylor expansion as follows:

$$1 - 2\frac{\Delta\omega_{osc}}{\omega_{osc}} = 1 + \frac{\Delta C_{eqv}}{C_{eqv}} \tag{3.37}$$

Using this transformation, results in:

$$\frac{\Delta\omega_{osc}}{\omega_{osc}} = -\frac{\Delta C_{eqv}}{2C_{eqv}} \tag{3.38}$$

Since the last term in Eq. (3.35) is $\ll 1$, it can be ignored. By substituting Eq. (3.38) in Eq. (3.35), the ECC-DCO normalized amplitude can be approximated to be:

$$\frac{V'_{osc}}{V_{osc}} = \frac{(\omega_{osc} + \Delta\omega_{osc})^2}{\omega_{osc}^2} = 1 - \frac{\Delta C_{eqv}}{C_{eqv}} \approx 1 \tag{3.39}$$

for $\Delta C_{eqv} \ll C_{eqv}$. Therefore, once the condition in Eq. (3.29) is satisfied, the amplitude has poor dependency on the tuning capacitors. Conditions stated by Eq. (3.32) and (3.33) serve as design criterion to assist the simulation based design methodology in obtaining a constant amplitude throughout the TR. Stabilizing the amplitude is important for suppressing the amplitude-to-phase conversion [12].

3.5 Design Considerations

In this section, the result obtained from the previous sections are used to form a robust design methodology. Four oscillators are designed and process corner simulation results are compared with the mathematical derivations of the last sections.

3.5.1 CC-DCO versus ECC-DCO Design Aspects

In order to verify the concept and prove the mathematical analysis, two versions of each fully differential ECC-DCO (ECC1, ECC2) and CC-DCO (CC1, CC2) were developed using TSMC 65 nm RFIC models. Process with corner temperature analysis is performed for all of the four designs. The performance results are listed in Table 3.1. The values of L, C_1, V_{dd}, V_{b1}, and V_{b2} for all designs are 88 pH,

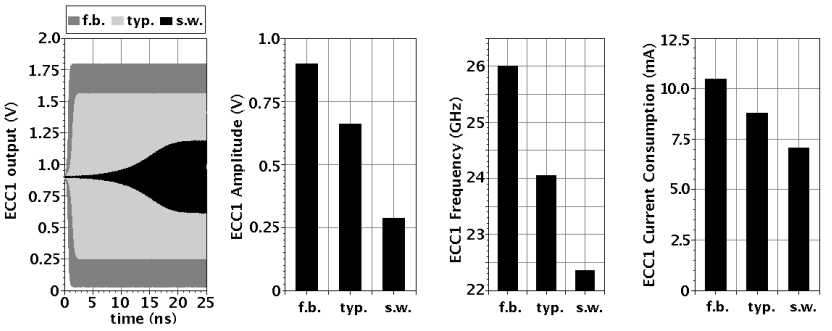
680 fF, 1.2 V, 0.6 V, and 0.9 V respectively, where R is the ratio of $W_{3,4}$ to $W_{5,6}$ and I_{avrg} is the average current consumption. Start-up time is measured as the time to reach 90% of V_{osc}.

The corner simulation results for the four designs are shown in Fig. 3.6. The CC2 is designed to sustain process and temperature variations, and it passes the typical process corner at the typical temperature of $25°C$ (typ.), fast-best process corner at low temperature of $-25°C$ (f.b), and slow-worst process corner at high temperature of $75°C$ (s.w.).

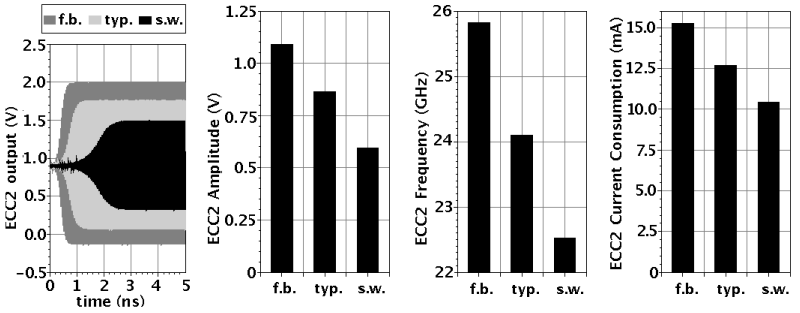
ECC1 is designed with $M_{1,2}$ and $M_{5,6}$ being half of the corresponding devices for CC2. With the same tuning frequency, the performance of ECC1 is comparable or better than that of the CC2, in spite of having G_{m1} and the tail current is being halved. The s.w. corner for a start-up is an exception as the start-up time is worse for the ECC1 than the CC2. ECC1 improves the amplitude as compared to CC2 but does not improve the start-up time.

If the reduced device sizes in ECC1 are applied to design CC1, then CC1 fails to oscillate under typical and slow-worst corners. If these devices are increased from being 1/2 the CC2 device sizes in ECC1 to 3/4 the CC2 device sizes in ECC2, then even with a 25% reduction in the tail current and a reduction in I_{avrg} by 10.2%, 7.4%, and 16.9% for the typ, f.b, and s.w corners, the amplitude is higher by 40% and 35% for the typ and f.b corners, while it is increased by more than 100% for the s.w corner.

The enhanced amplitude result proves the derived mathematical relation in (3.26). $G_{m3,4}$ with its minus sign decreases the denominator and thus increases the amplitude.



(a)



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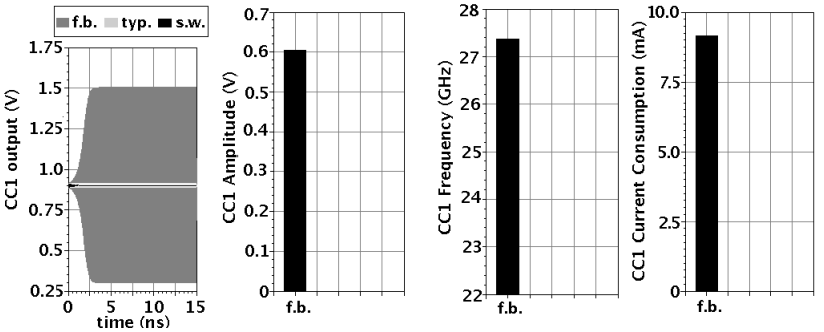
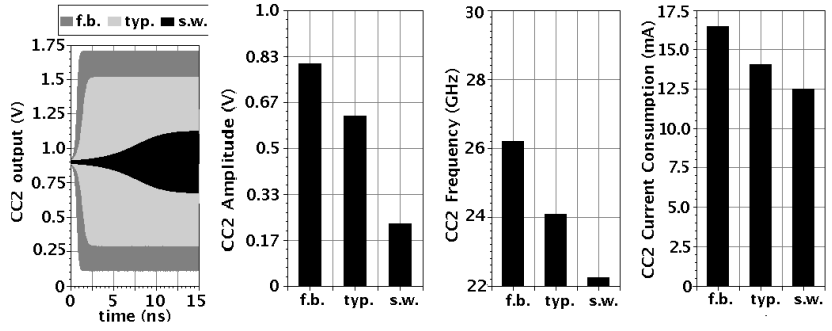


(c)



(d)

FIGURE 3.6: Simulated corner analysis showing the waveform, amplitude, and frequency under typical (typ), fast-best (f.b), and slow-worst (s.w) process and temperature corners. (a) ECC1-DCO (b) ECC2-DCO (c) CC1-DCO (d) CC2-DCO.

The ratio between V_{osc} of the ECC and CC designs (R_{vosc}) can be obtained by dividing Eq. (3.30) over Eq. (3.20) that results in:

$$R_{vosc} = \frac{I_{bias,ECC}}{I_{bias,CC}} \frac{(C_1 + C_2)}{C1} \tag{3.40}$$

The ratio between the simulated amplitudes for ECC2 and CC2 at the typ. corner is 1.4. The calculated value based on Eq. (3.40) is 1.49 which is comparable to the simulation counterpart. Repeating the same for ECC1 and CC2 results in 1 and 1.03 for the simulated versus calculated amplitude ratios. The comparable results between the hand calculations and the simulated results prove the derived mathematical equations.

The start-up time for ECC2 is reduced by 47%, 33%, and 72%, as compared to CC2, for the typ, f.b and s.w corners correspondingly. This result confirms that the negative resistance is stronger as derived in Eq. (3.3). Moreover, even with g_{m1} for ECC2 being 0.75% of that of the CC2, the summing effect of $g_{m,3}$ increases R_{neg1}, and the start-up time is reduced significantly.

3.5.2 Amplitude Boosting and Stability Optimizing

The effectiveness of the ECC-DCO in increasing and stabilizing the amplitude across the TR is validated through simulation, and the expected mathematical results are verified. Fig. 3.7(a) shows the coarse frequency tuning for ECC1,2 and Fig. 3.7(b) indicates the amplitude throughout the TR. Maximum amplitude points exist, and V_{osc} is higher for the ECC2 as expected from the analysis.

M_3,M_4 and M_5,M_6 are low threshold devices of similar types. Prior to optimization, the size of M_3,M_4=M_5,M_6. G_{m3} is optimized based on simulation by changing the sizes of M_3,M_4 through varying R. Fig. 3.7(c) shows the effect of changing the value of R on the amplitude taken at the minimum, middle, and maximum

coarse tuning. The three graphs intercept at a point that corresponds to $R = 3.15$. At this point, the amplitude is independent of the tuning capacitor. Fig. 3.7(d) shows the amplitude versus the TR with $R = 3.15$. The percentage of amplitude variation is calculated as:

$$\%V_{osc} = \frac{V_{osc,max} - V_{osc,min}}{V_{osc,24GHz}} \tag{3.41}$$

Based on the simulation results in Fig. 3.5(b). The amplitude varies across the TR by 22 mV and 32 mV for ECC1 and ECC2 respectively. However, it varies by just 7 mV for ECC2 with $R = 3.15$ in Fig. 3.5(d). Increasing R may stabilize the amplitude within 7 mV across the TR. However, large R increases the parasitic capacitors that affect the TR. Under the restrictions of the tuning design requirements in Section III, R is chosen to be 2 for ECC2 and the ECC-DCO design.

3.5.3 ECC-DCO Design Methodology

The developed design methodology is a combination of hand calculations and simulation-based design. Low PN requirement is considered. The transistors are biased at the optimum noise figure current density of 0.15 $mA/\mu m$. V_{osc} stability is optimized. Minimum I_{bias} is determined by the optimized V_{osc} and start-up condition is verified. The strategy to build up the ECC-DCO structure in Fig. 3.1 is as follows:

1. Set the tank inductor to the minimum feasible value. Get Q_L and $R_{L,P}$ at the maximum tuning frequency and calculate the maximum $R_{L,P}$ ($R_{P,max}$) from (3.10).

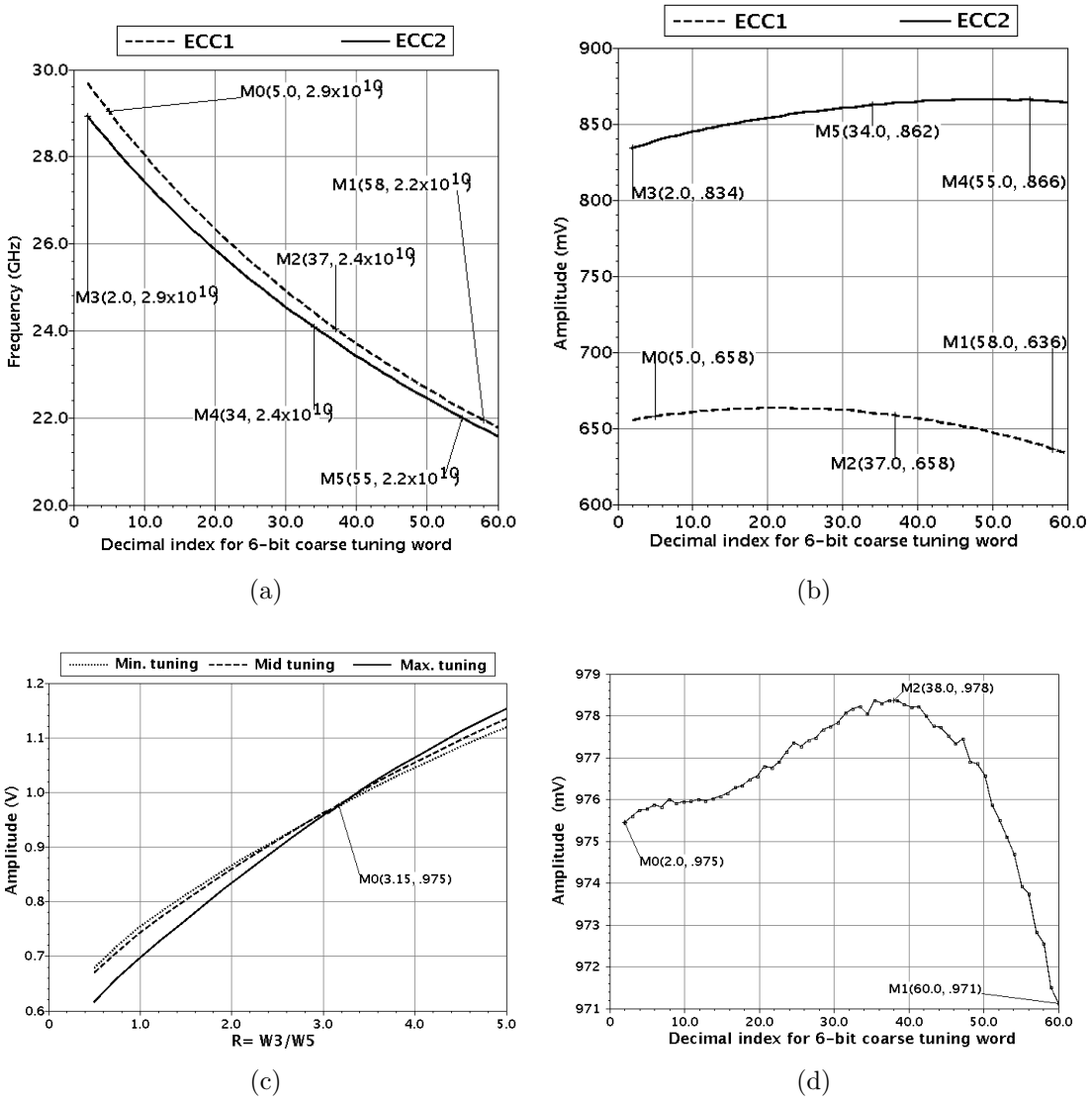


FIGURE 3.7: Amplitude stability Simulation Based optimization. (a) Coarse frequency tuning for ECC1 and ECC2 to show the TR. $R = 2$. (b) The amplitude of ECC1 and ECC2 across the TR. $R = 2$. (c) Parametric analysis for ECC2 amplitude vs. R at the minimum, middle, and maximum tuning. (d) ECC2 amplitude across the TR with $R = 3.15$.

2. Based on L, use (3.9) to calculate the maximum and the minimum C_{eqv} ($C_{eqv,max}$ and $C_{eqv,min}$) that corresponds to the minimum and maximum tuning frequency ($f_{osc,min}$ and $f_{osc,max}$) respectively.

3. Let $C_{2,max'} = mC'_1$ and $C'_{2,max} > rC_{3,max}$, where m and r are variables for design optimization. Low PN mandates that $C'_{2,max} \leq C'_1$. Therefore, $m \leq 1$. Since the intermediate and the fine tuning design are part of C_2, r should be > 1. Let $m = 1$ and $r = 4$, calculate C'_1 from in (3.9).

4. Design $C'_{3,min}$= $C'_{2,min}$. Substitute $C'_{eqv,min}$ from step 2 and C'_1 from step 3 in (3.7), calculate $C'_{2,3,min}$.

5. Set V_{osc} to the maximum allowed value $V_{osc,max}$ by the technology and the system requirements. Get I_{bias} from (3.30) using $R_{P,max}$ from step 1 and $V_{osc,max}$.

6. $M_{1,2}$ are designed with a minimum length defined by the process. Considering the biasing at a current density of 0.15 $mA/\mu m$ for low PN noise requirement, determine the size of M_1 from $W_1 = I_{bias}/0.15$. Get g_{m1} and the values of the parasitic capacitors from the simulator by employing a simple simulating test circuitry.

7. Let $I_{b3} = I_{bias}$ by assuming $f = 0.5$ in (3.33). Use low thresholds device model, size M_3 using the simulator considering $V_{ds3} = V_{gs3}$=V_{s1}. Get V_{s1} from the outcome of step 6. Get g_{m3} and the values of the parasitic capacitors from the simulator.

8. Verify the start-up condition at the maximum tuning frequency in (3.8) from the outcome of g_{m1}, g_{m3}, C'_1, and $C'_{2,min}$ in step 6, 7, 3, and 4 respectively.

9. Iterate between step 6, 7, and 8, to verify the start-up condition in step 8, by changing W_1 or W_3 or both, keeping the same current density.

10. Use low thresholds device model, set the bias and the size M_5 using the simulator considering V_{ds5}=V_{s1}. Get the values of the parasitic capacitors from the simulator.

11. Using Eqs. (3.4), (3.5), and (3.6), subtract C'_1, $C'_{2,max}$, and $C'_{3,max}$ from the values of the parallel associated parasitic capacitors to calculate C_1, $C_{2,max}$, and $C_{3,max}$ respectively.

12. Verify that $C'_{2,min}$ and $C'_{3,min}$ are not less than the parallel parasitic capacitors in (3.5) and (3.6).

13. Optimize V_{osc} throughout simulation as in section B.

14. Iterate between the steps 3-13 by optimizing m, r, I_{bias}, W_1, W_3 and W_5.

3.6 ECC-DCO Design and Pre-Layout Simulation

The main structure of the ECC-DCO is constructed as shown in Fig. 3.8. Based on (3.3), the ECC-DCO adds more negative resistance at the start-up. Moreover, it enlarges and stabilizes the amplitude of oscillation.

3.6.1 ECC-DCO Design

Based on the design methodology in section $V-C$, Single turn central tap tank inductor (L_t) with 176.6 pH is first selected and implemented in Metal 9. It achieves Q_L of 43 at 24 GHz. Tail biasing current (I_5,I_6) and M_5,M_6 size is determined by the required V_{osc} based on (3.30). PN is inversely proportional to the square of V_{osc} that calls for maximizing V_{osc}. However, larger V_{osc} is restricted by the allowed safe voltage that can be applied to the transistor junctions without

causing a breakdown. The output is taken from the drain of $M_{1,2}$ that is connected to V_{dd} through $R_d \| L_d$. Such that an output buffer is not needed and the output power is increased with the drain inductor L_d.

Process corner analysis is conducted for the CC-DCO and the ECC-DCO and the magnitude and the phase of the loop-gain are shown in Fig. 3.9 (a)-(b) respectively. The worst case for both designs is at the s.w. corner of the minimum frequency. Based on the worst-case, the minimum size of the transistors is optimized. While M_1,M_2 size for CC2 includes the required reliability factor to ensure start-up under temperature and process variations. W_1,W_2 and W_5,W_6 for the ECC-DCO are decreased by 25%. W_3,W_4 is triple W_5,W_6 with $R = 3$.

Table 3.2 shows the values of the designed parameters for the ECC-DCO.

Based on the describing function approximation in (3.17), the plot of G_{m1} across the TR is shown in Fig. 3.10. The maximum required G_{m1} for the CC-DCO and the ECC-DCO are 19.6 mS and 18.6 mS respectively, such that CC-DCO needs an extra 1 mS to keep the oscillation steady.

The ECC-DCO PN at 1 MHz offset is simulated against process corners. The resultant PN are tabulated in Table 3.3 at the minimum, middle, and maximum tuning frequency. The ECC-DCO PN is always better than -101 dBc/Hz.

Considering mismatch and process variations, montecarlo analysis is conducted for 1100 samples. Fig. 3.11 shows the simulated montecarlo analysis results for the amplitude and the loop-gain magnitude taken at the minimum, middle, and maximum tuning frequency. The standard deviation for V_{osc} at the minimum and middle tuning frequency is 1.3 mV, while it is 1.4 mV at the maximum tuning frequency. The $\%V_{osc}$ considering the mean values at the three tuning frequencies is as low as 1.6%.

The mean value for the loop-gain magnitude is the worst at the minimum tuning frequency as expected and agrees with the process corner analysis.

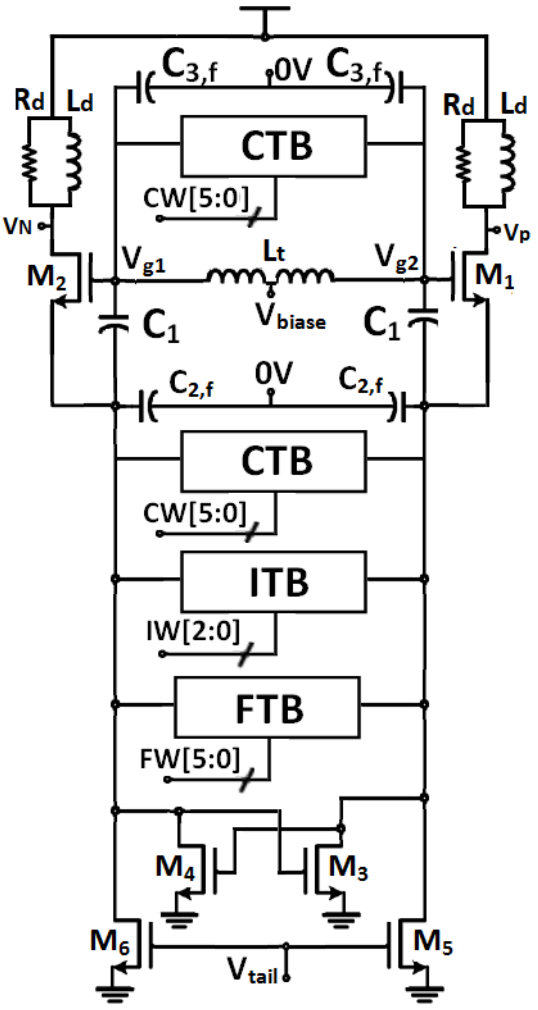
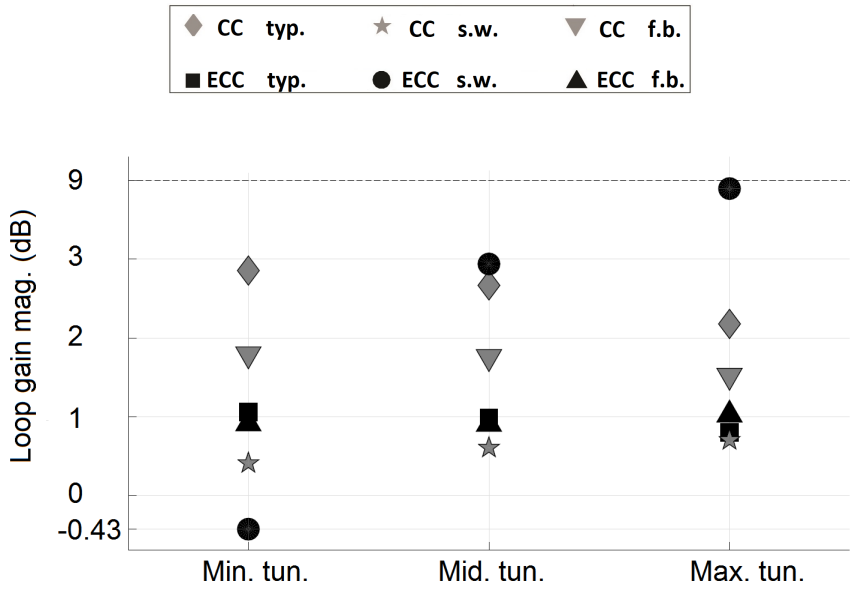


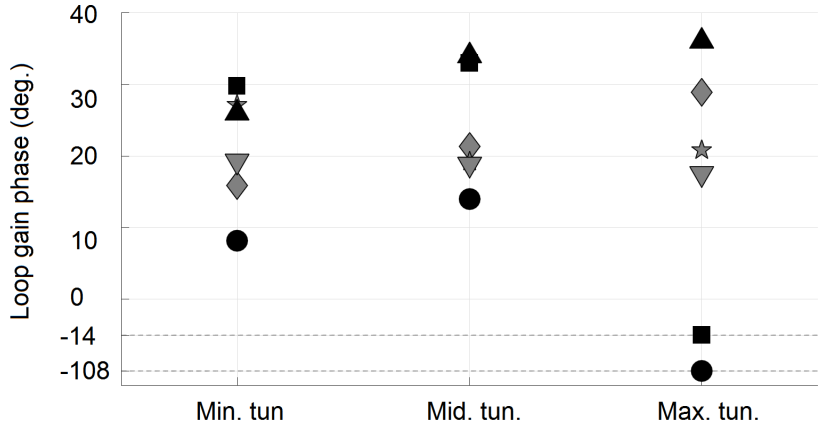
FIGURE 3.8: Schematic of the Enhanced Colpitts Clapp-DCO (ECC-DCO)

3.6.2 ECC-DCO Frequency Tuning

Simultaneous tuning mechanism for wide TR with fine resolution is obtained by separate and overlapped tuning capacitance banks based on (3.27) and (3.28). The two Coarse Tuning Banks (CTB) and the Intermediate Tuning Bank (ITB) are implemented using binary-weighted Metal-oxide-Metal (MoM) capacitors controlled by a 6-bit Coarse Word (CW[5:0]) and 3-bit Intermediate Word (IW[2:0)] respectively. The Fine Tuning Bank (FTB) is implemented using binary-weighted varactors. It is controlled using a 6-bit Fine Word (FW[5:0]). The unit capacitance cells are shown in Fig. 3.12. It is implemented to be similar to [20].



(a)



(b)

FIGURE 3.9: Simulated process corner analysis. (a) Process corner analysis for the CC-DCO and the ECC-DCO loop-gain magnitude. (b) Process corner analysis for the CC-DCO and the ECC-DCO loop-gain phase.

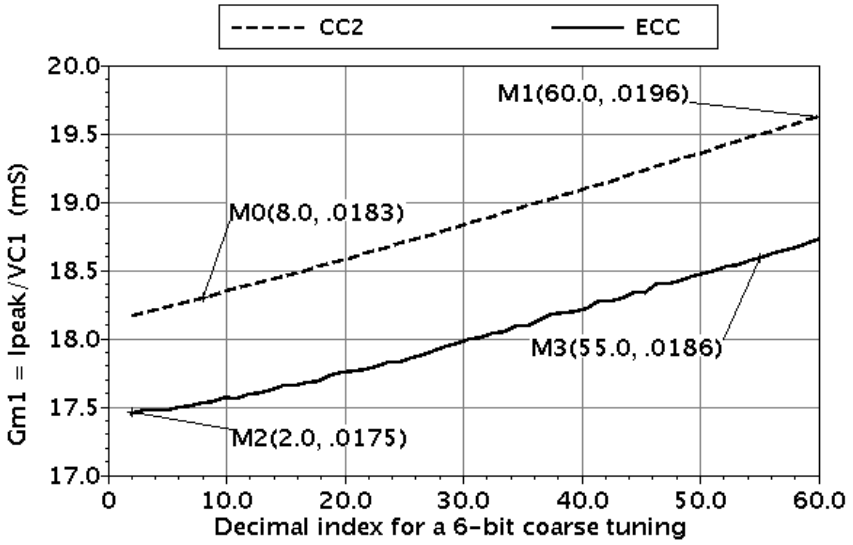
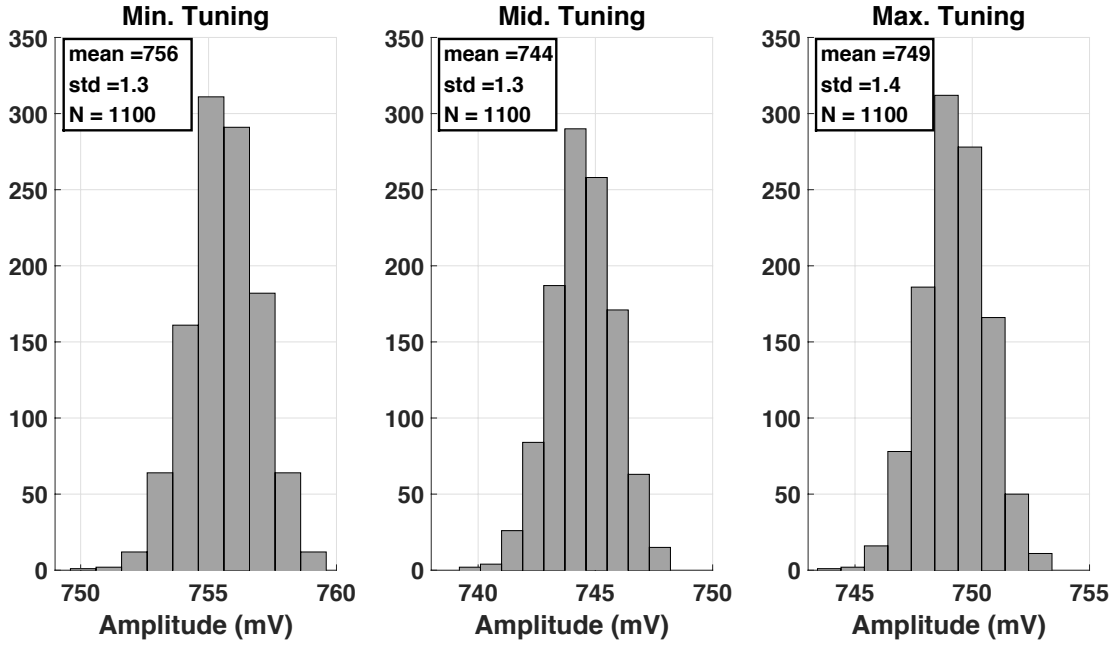


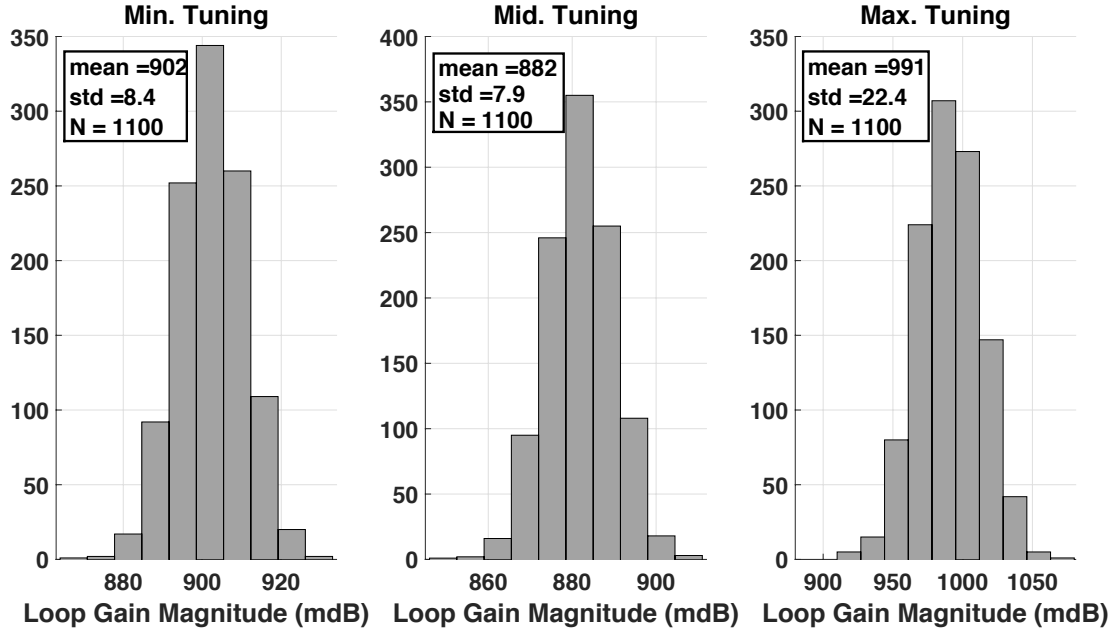
FIGURE 3.10: Simulated Large Signal Transconductance (G_m) of the CC2 and the ECC vs. the Coarse Tuning Index.

TABLE 3.2: ECC-DCO Design Parameters

Device	**Size**
$M_{1,2}$	$30\mu m/60nm$
$M_{3,4}$	$30\mu m/120nm$, multiply=3
$M_{5,6}$	$30\mu m/120nm$
L_t (Spiral)	1 turn center tab Area: width=$265\mu m$, length=$238\mu m$
C_1 (MOM)	W/finger=$100nm$, array=$8X8$, multiply=182
$C_{2,f}$ (MOM)	W/finger=$100nm$, array=$8X8$, multiply=80
$C_{3,f}$ (MOM)	W/finger= $100nm$, array=$8X8$, multiply=1
CTB (MOM)	W/finger=$100nm$, array=$8X8$, multiply=$1, 2, 4, 8, 16, 32$
ITB (MOM)	W/finger=$100nm$, array=$8X8$, multiply=$1, 2, 4$
FTB (AMOS)	$300nm/300nm$, multiply=$1, 2, 4, 8, 16, 32$

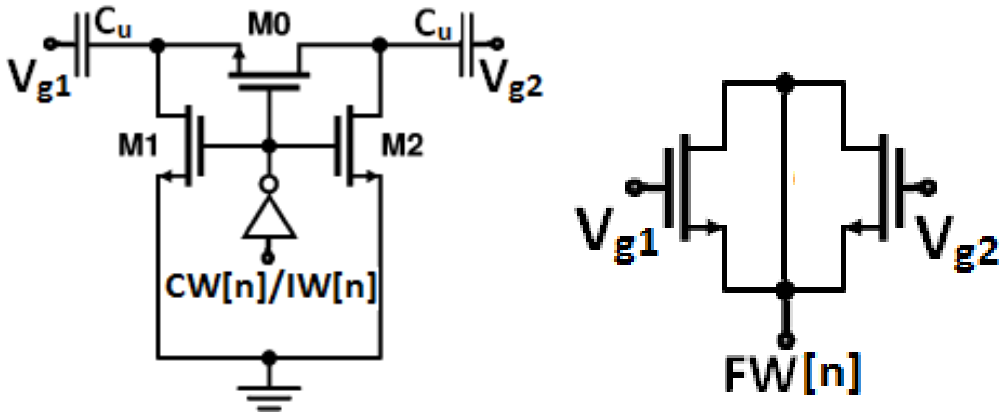


(a)



(b)

FIGURE 3.11: Simulated Montecarlo analysis considering process and mismatch at the minimum, middle, and maximum TR. (a) Montecarlo analysis for the ECC amplitude. (b) Montecarlo analysis for the ECC loop-gain magnitude.



(a) (b)

FIGURE 3.12: Unit capacitance cell structure. (a) MoM switched capacitor cell for the coarse and intermediate tuning banks
. (b) Varactors unit cell for the fine tuning bank.

TABLE 3.3: ECC-DCO PN against process Corners

Corner	**PN (dBc/Hz)** @Min-Freq	**PN (dBc/Hz)** @Mid-Freq	**PN (dBc/Hz)** @Max-Freq
s.w.	-106	-104	-101
typ.	-109	-106	-102
f.b.	-112	-110	-107

TABLE 3.4: Post-Layout Performance Comparison

Parameter	**CC-DCO**	**ECC-DCO**
Min. Amp. (mV)	525	747
Max. Amp (mV)	628	759
Amp at 24 GHz (mV)	613	758
% Amp. Var.	19.6%	1.5%
Start-up time (ns)	2.2	1.3
Power consumption (mW)	16.9	12.8
PN (dBc/Hz)	-104	-106

3.7 Post-Layout Results

To verify the effectiveness of the modified topology, layout is accomplished for the designed ECC-DCO and CC2. The post-layout with parasitic extraction performance results for the CC-DCO and the ECC-DCO are tabulated in Table 3.4.

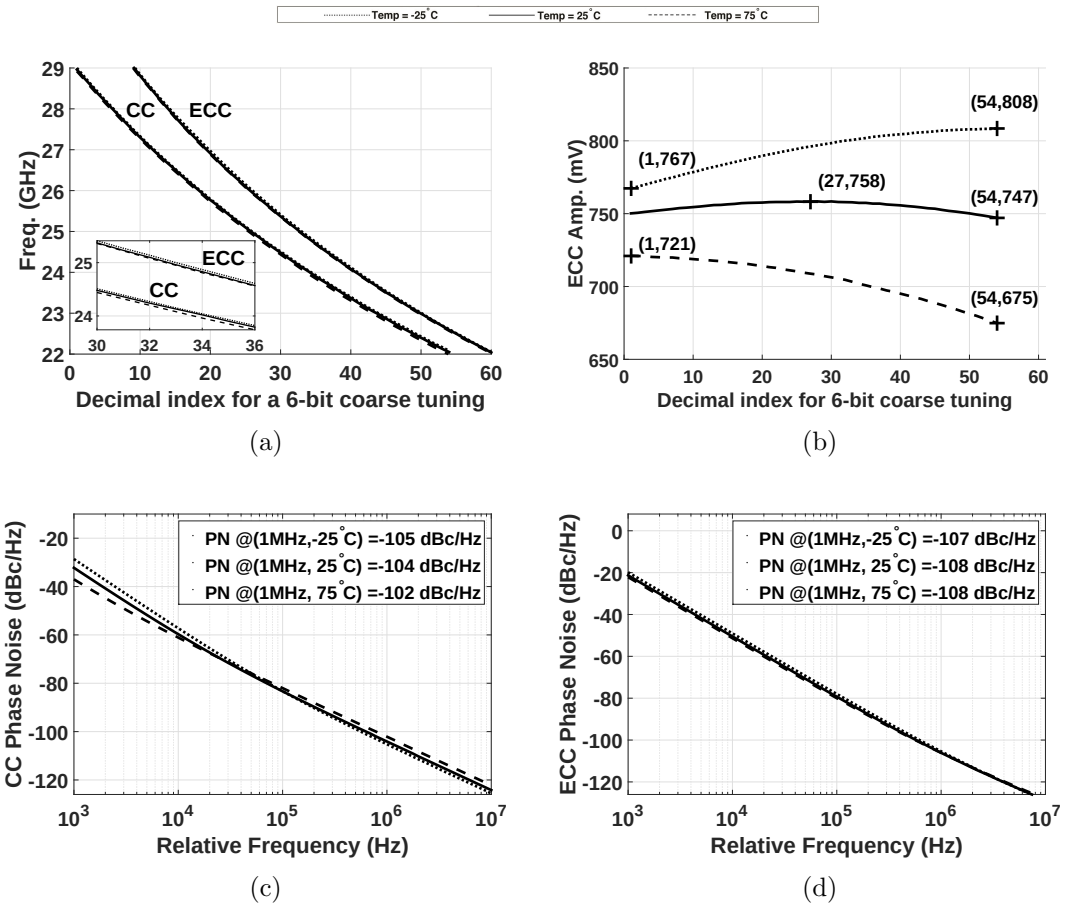


FIGURE 3.13: Post-Layout Simulation Results. (a) The frequency vs coarse tuning. (b) The ECC-DCO amplitude across the TR at $-25°C$, $25°C$, and $75°C$. (c) Oscillating at 24 GHz, the CC PN at $-25°C$, $25°C$, and $75°C$. (d) Oscillating at 24 GHz, the ECC PN at $-25°C$, $25°C$, and $75°C$.

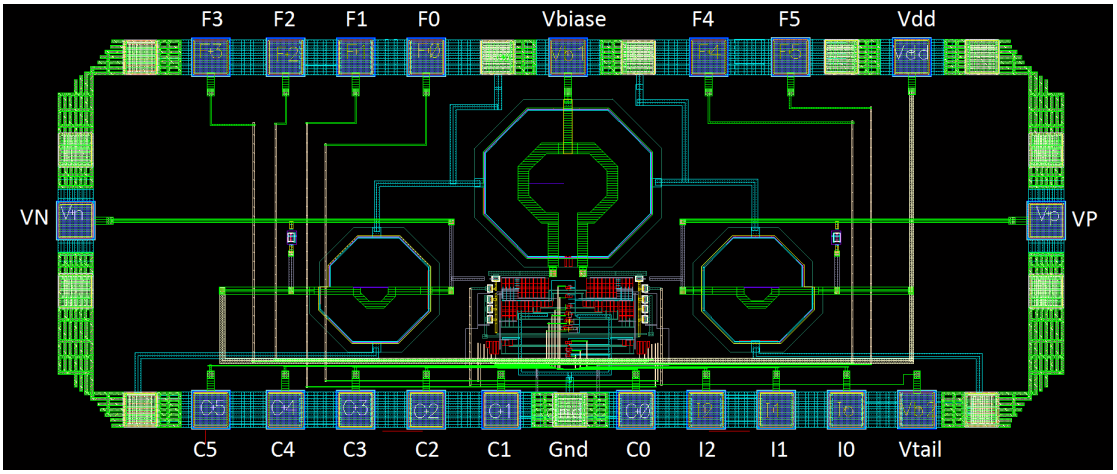


FIGURE 3.14: Chip layout of the proposed 24 GHz ECC-DCO

While the CC2 amplitude varies across the TR by 103 mV, the ECC-DCO amplitude varies by 12 mV.

Fig. 3.13(a) shows the post-layout frequency tuning for the CC and the ECC at $-25°C$, $25°C$, and $75°C$. The tuning index for the CC starts at 9 caused by less parasitic capacitors in parallel with C_2. The temperature has minimal effect on the coarse tuning for both designs. The coarse, intermediate and fine tuning steps for the ECC-DCO are 160 MHz, 50 MHz, and 1.1 MHz respectively. The intermediate and fine TR are 350 MHz and 66 MHz respectively to provide the overlapping between the banks.

Fig. 3.13(b) shows the amplitude variation with temperature across the TR. The amplitude variations across the TR are as low as 5.3%, 1.5%, and 6.8% at $-25°C$, $25°C$, and $75°C$ respectively. The increase/decrease of G_{m1} and G_{m3} is of the same polarity that is subtracted at the denominator of Eq. (3.26) making the ECC-DCO less sensitive to temperature variations.

Oscillating at 24 GHz, the PN at 1 MHz offset is shown in Fig. 3.13(c)-(d) for the CC and the ECC respectively. The ECC improves the PN by 2 dB at $25°C$ and by 4 dB at $75°C$, as compared to the CC PN. Driven by low amplitude variations with temperature, the ECC PN deviates by only 1 dBc/Hz with temperature variation between $-25°C$ and $75°C$, as compared to 3 dBc/Hz deviation for the CC.

Fig. 3.14 shows the chip for the ECC-DCO. CC-DCO chip has the same dimension and pads. The total chip area is 1 mm^2, which is pad limited. The core area fits in a rectangular of 1.3 $mm \times 0.5$ mm. To quantify the overall performance, the Figure of Merit (FoM) and Figure of Merit for TR (FoM_T) are defined in (3.42) and (3.43) as in [4].

$$FoM = PN - 20log\frac{f_{center}}{\Delta f} + 10log\frac{PDC}{1\ mW} \tag{3.42}$$

$$FoM_T = PN - 20log\frac{f_{center}}{\Delta f}.\frac{TR\%}{10\%} + 10log\frac{PDC}{1\ mW} \tag{3.43}$$

Where P_{DC} is the power dissipation and Δf is the offset from the center frequency (f_{center}) of 24 GHz. Table 3.5 shows the resultant comparison with state-of-the-art mm-wave VCOs and DCOs. The reported PN in [28] is $-146.7\ dBc/Hz$ because the VCO consumes power in the range of a hundred, while the maximum reported power among the rest is 24 mW. The ECC-DCO has the best FoM_T and the highest FoM with the power consumption limited to few tens of mW.

Table 3.5: Performance Summary and Comparison

Ref	**Type**	**F_o (GHz)**	**TR (%)**	**Δf (MHz)**	**PN (dBc/Hz)**	**PDC (mW)**	**FoM (dBc/Hz)**	**FoMT (dBc/Hz)**	**CMOS**
[12] measurement	VCO	19.1	4.8	1	-103	5	-182	-175	130 nm
[4] measurement	VCO	26	25	1	-104	9.96	-182	-190	130 nm
[21] measurement	DCO	60	10	1	-93	12	-178	-178	90 nm
[22] measurement	DCO	25	16	10	-117	23	-171	-175	40 nm
[23] measurement	VCO	38.5	11	1	-87	11.7	-168	-169	65 nm
[24] measurement	VCO	26.3	40.3	10	-119	4.3	-180	-192	65 nm
[25] measurement	VCO	27.5	43.3	10	-109	7.2	-169	-182	65 nm
[26] measurement	VCO	24.7	22.9	10	-127.3	24	-181	-188.6	32 nm SOI
[27] measurement	VCO	57.8	25.4	1	-100	24	-181.5	-189.6	40 nm
[28] measurement	VCO	4.07	18.6	3	-146.7	126.85	-189	-192	65 nm
CC-DCO post-layout	DCO	24	29	1	-104	16.9	-179	-188	65 nm
ECC-DCO post-layout	DCO	24	29	1	-106	12.8	-185	-194	65 nm

3.8 Conclusions

In this chapter, the modified topology of ECC-DCO achieves better performance over a wide TR of 29% for SRR applications. Oscillation initiation is boosted up by an extra negative resistance without the need to increase the tail current.

The amplitude and start-up enhancement are achieved by analyzing the proposed circuitry at start-up and the large-signal steady oscillation state. The derived equations serve as design criterion and assist in the simulation-based design methodology to optimize the amplitude stability.

The ECC-DCO is designed in Cadence using 65 nm RF component models. Pnoise setup with SpectreRF is used to simulate the PN. Simulation results for the ECC-DCO and a robust CC-DCO show that, even with 24% reduction in the power consumption, the amplitude of oscillation for the ECC-DCO is boosted by 23%. The ECC-DCO amplitude varies by 1.5% across the TR as compared to 19.6% variation for the CC-DCO. Start-up time is reduced by 41%. The ECC-DCO PN is 2 dB better than the CC-DCO PN. The ECC-DCO achieves better FoM and FoM_T than the CC-DCO that confirms the enhanced achievements. In the future, the ECC-DCO is to be implemented as part of ADPLL, which is suitable for frequency modulated continues wave generation or an industrial measurement applications.

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Chapter 4

Impact of Process and Temperature Variations on the Design of CMOS Colpitts Oscillators

4.1 Introduction

The ideal oscillator output signal is a perfect periodic waveform. However, random and systematic errors can affect the amplitude and phase of the output oscillating signal. Random errors are due to noise in physical components constituting the oscillator phase noise. Systematic errors are caused by Process, Voltage, and Temperature (PVT) variations [1].

Crystal-less CMOS realization reference oscillators are motivated by reducing the size and the cost for system-on-chip (SoC) implementations. High temperature stability and low phase noise mainly characterize quartz crystals. Thus RF frequency oscillators replacing quartz crystal should offer similar behavior. Colpitts

oscillator is popular for its excellent phase-noise performance [2] [3]. Colpitts oscillator replacing crystal was reported in [4].

Temperature stability and process variation analysis is usually performed for oscillators replacing quartz-crystals. However, all oscillators can benefit from such analysis. Thus, design methodology based on the estimated process and temperature dependencies early in the design process can save the need for unnecessary design-loop iteration and thus minimizes the time-to-market.

In this work, a detailed design methodology of the systematic frequency drift for CMOS Colpitts oscillator is presented. It can reduce iteration in the design process by identifying key parameters that need to be optimized at the early stages to be refined later by computer simulations. To the author's knowledge, temperature and process sensitivity, in the contest of start-up condition, has not been explored to be generic for Colpitts Voltage Controlled Oscillator (VCO) in most of this prior work.

In [5] tuning range was derived showing process spread parameters, but it was implemented in silicon bipolar technology. The work in [6] presents temperature sensitivity analysis and the derived equation presented can serve as a design criterion, but it was for LC type VCO. Temperature stability for CMOS Colpitts oscillator was analyzed in [4], but it lacks start-up temperature analysis.

This chapter is organized as follows; in the next section negative resistance linear model for Colpitts oscillator is derived. Non-linear model is presented using the describing functions. Section III presents process and temperature sensitivity analysis. Section IV shows the design and simulation results of Colpitts oscillators followed by the conclusion.

4.2 Colpitts Models

4.2.1 Negative Resistance Linear Model

Common-Drain (CD) Colpitts oscillator is shown in Fig. 4.1(a). Linear model of the Colpitts oscillator can be described as a negative resistance generator in parallel with a resonant load [7]. The resonator load consists of a lossy inductor modeled as an inductor L in series with the parasitic series resistance R_L. Negative resistance generator exhibits reflection coefficient (Γ_G) greater than 1 to enforce instability.

The integrated capacitors C_1,C_2 implemented in $65nm$ CMOS technology can have high quality factor [8], thus the lossy serial resistances associated with $C_{1,2}$ can be neglected. Channel length modulation and body effect are not considered in this chpater. However, parasitic capacitors C_{gs}, C_{sb}, and C_{gd} are considered.

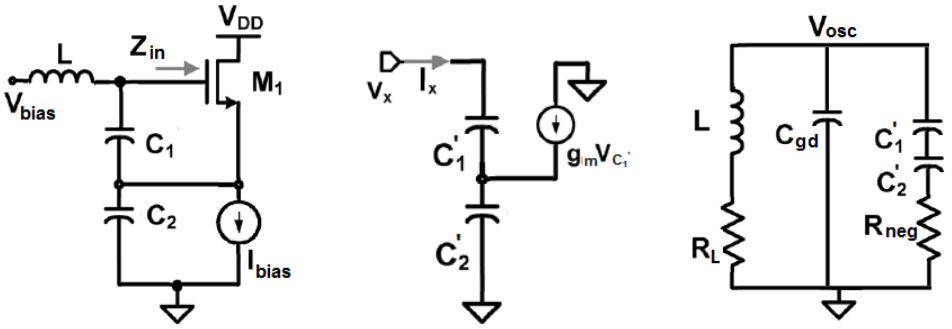
The impedance Z_{in}, looking into the gate of the transistor M_1, is derived using the model shown in Fig. 4.1(b). By substituting C_1'= C_1+C_{gs}; C_2'= C_2+C_{sb}. The impedance Z_{in} is equal to:

$$Z_{in} = \frac{V_x}{I_x} = \frac{1}{sC_1'} + \frac{1}{sC_2'} - \frac{g_m}{\omega^2 C_1' C_2'} \tag{4.1}$$

The negative resistance is denoted by:

$$R_{neg} = -\frac{g_m}{\omega^2 C_1' C_2'} \tag{4.2}$$

where g_m is the small signal transconductance of M_1. The negative resistance linear model for the CD Colpitts oscillator is shown in Fig. 4.1(c). At the frequency of oscillation (ω_{osc}), the inductance L resonate with C_{gd} in parallel with the series combination of C_1' and C_2' [7]. C_{eqv} is the series equivalent capacitance of C_1' and C_2'. Under the assumption that the $C_{gd} \ll C_{eqv}$. ω_{osc} is given by:



(a) (b) (c)

FIGURE 4.1: CD Colpitts oscillator: (a) shows a single-ended CD Colpitts oscillator, (b) and (c) show the steps to derive the negative resistance linear model. (a) CD Colpitts Oscillator. (b) AC Equivalent to Determine the Input Impedance. (c) Negative Resistance Linear Model.

$$(\omega_{osc})^2 \approx \frac{1}{LC_{eqv}} \tag{4.3}$$

The amplitude of oscillation V_{osc} at the onset of oscillation is practically zero. The start-up requires that $\mid R_{neg} \mid > R_L$ [9]. It can be expressed as:

$$\left| \frac{g_m}{\omega_{osc}^2 C_1' C_2'} \right| > R_L \tag{4.4}$$

4.2.2 Non-Linear Model

Large signal analysis based on the describing function model in [10] is used to analyze the behavior of the oscillator at the steady state oscillation. It is based on the expectation that the drain current has the shape of a series of very narrow pulses. Non-linearity of the negative resistance device stabilizes V_{osc} and the amplitude of the drain current is approximated by $I_d = 2I_{bias}$ [10]. I_{bias} is the biasing current for the NMOS device shown in Fig. 4.1(a). The describing function model approximates the large signal transconductance (G_m) by:

$$G_m \approx \frac{2I_{biase}}{V_1} \approx \frac{2I_{biase}}{\frac{C_2'}{(C_1'+C_2')}V_{osc}} \approx 2I_{biase}\frac{1+\frac{C_1'}{C_2'}}{V_{osc}} \tag{4.5}$$

where V_1 is the amplitude of oscillation across C_1', V_{osc} is the amplitude of oscillation across L. At steady state oscillation, G_m can replace g_m in (4.2) such that:

$$R_{neg} = -\frac{G_m}{\omega^2 C_1' C_2'} \tag{4.6}$$

Steady state oscillation condition requires that (4.6) = R_L.

4.3 Sensitivity Analysis

Process and temperature stability analysis set bases to design frequency references and crystal-less oscillators that mandates high accuracy and temperature stability.

4.3.1 Process Variation Analysis

If L changes by $\pm\Delta L$, C_{eqv} changes by $\pm\Delta C_{eqv}$, then ω_{osc} changes by $\pm\Delta\omega_{osc}$. Therefore (4.3) is modified as follows:

$$(\omega_{osc} \pm \Delta\omega_{osc})^2 = \frac{1}{(L \pm \Delta L)(C_{eqv} \pm \Delta C_{eqv})} \tag{4.7}$$

We define the relative percentage variations $\rho_\omega = \frac{\Delta\omega_{osc}}{\omega_{osc}}$, $\rho_L = \frac{\Delta L}{L}$, and $\rho_C = \frac{\Delta C_{eqv}}{C_{eqv}}$. By dividing (4.3) over (4.7), and eliminating possibilities that may lead to $\rho_\omega > 1$, (4.7) is simplified to:

$$(1+\rho_\omega)^{-2} = (1-\rho_L)(1-\rho_C) \tag{4.8}$$

Being the percentage variation, ρ_ω is much smaller than one, hence the left side of (4.8) can be approximated by first-order Taylor expansion that results in:

$$(1 - 2\rho_\omega) \cong (1 - \rho_L)(1 - \rho_C) \tag{4.9}$$

Therefore the relative process variation of ρ_ω is:

$$\rho_\omega \cong \frac{1}{2}(\rho_L + \rho_C - \rho_L\rho_C) \tag{4.10}$$

Inductance is process independent [5][7]. The integrated inductance and capacitance are not correlated. Therefore the process spread of ω_{osc} can be expressed as:

$$\rho_\omega \cong \frac{1}{2}(\rho_C) \tag{4.11}$$

Process spread of the integrated capacitors depends on its type. Typical process spread for Metal-Insulator-Metal capacitors (MIM) and junction capacitors is about $\pm 10\%$ and $\pm 20\%$ respectively [1]. Once the process spread is estimated, process shift compensation circuitry can be designed such as using a programmable discrete frequency calibration method implemented as a switched-capacitor array [11].

4.3.2 Temperature Coefficient Analysis

The temperature coefficient of a parameter P is defined as:

$$TC_P \equiv \frac{1}{P}\frac{\delta p}{\delta T} \tag{4.12}$$

The frequency of oscillation is given by (4.3). Partial derivative rule is applied as follows:

$$2\omega_{osc}\frac{\delta\omega_{osc}}{\delta T} = \frac{1}{L}\frac{(-1)}{(C_{eqv})^2}\frac{\delta C_{eqv}}{\delta T} + \frac{1}{C_{eqv}}\frac{(-1)}{(L)^2}\frac{\delta L}{\delta T} \tag{4.13}$$

Dividing (4.13) by (4.3), it can be shown that:

$$TC_{\omega_{osc}} = -\frac{1}{2}\{TC_{Ceqv} + TC_L\} \tag{4.14}$$

Similarly, the temperature coefficient for C_{eqv} can be derived. The expression can be generalized to be applied for an equivalent series capacitor as follows:

$$TC_{C_{eqv}} = C_{eqv}\sum_{i=1}^{n}\frac{1}{C_n}TC_{Cn} \tag{4.15}$$

Temperature coefficient for an equivalent parallel capacitor, such as C_1', can also be generalized in a similar way as follows:

$$TC_{C_1'} = \frac{1}{C_1'}\sum_{i=1}^{n}C_nTC_{Cn} \tag{4.16}$$

Linear and non-linear behavior contributes to the frequency of oscillation [4]. The harmonic injection of the non-linear negative resistance circuit to the resonator modifies the oscillation frequency. The error due to non-linearity (ϵ) is defined in [1] as:

$$\epsilon = \frac{(\omega_{osc} - \omega_{osc,non-linear})}{\omega_{osc}} = 1 - \frac{\omega_{osc,non-linear}}{\omega_{osc}} \tag{4.17}$$

Substitute for $\omega = \omega_{osc}$ in (4.2) and $\omega = \omega_{osc,non-linear}$ in (4.6). Divide (4.2) over (4.6) after modification. The ratio between $\omega_{osc,non-linear}$ and ω_{osc} comes to be G_m/g_m, and (4.17) can be written as:

$$\epsilon = 1 - \sqrt{\frac{G_m}{g_m}} \tag{4.18}$$

The value of ϵ depends on the current shape of $M_{1,2}$. Temperature dependency of ϵ can be minimized by employing constant g_m biasing scheme. Equation (4.5) reveals that G_m varies with V_{osc} as well. V_{osc} changes with the supply voltage that calls for a regulated supply.

4.3.3 Frequency Tuning

Start-up analysis is important to ensure that the oscillator operates over the desired tuning range and different process corners [12]. In the CD Colpitts topology, the small parasitic capacitor C_{sb} appears in parallel with C_2. Thus implementing C_2 as a varactor diode maximizes the available tuning range. Start-up condition is expressed in (4.4) reveals that the condition of oscillation changes across the tuning range if C_2 is the varactor. Equation (4.4) can be modified by substitute for ω_{osc}^2 from (4.3) and R_L by $(\omega_{osc}L/Q_L)$, where Q_L is the quality factor of L:

$$g_m > \frac{\omega_{osc}(C_1' + C_2')}{Q_L} \tag{4.19}$$

C_2' should satisfy the condition:

$$C_2' < (\frac{g_m Q_L}{\omega_{osc}} - C_1') \tag{4.20}$$

Process variation effect on this critical condition may be investigated in terms of worst case scenario. The condition should stay valid for $C_{2,max}$, $g_{m,min}$, and $C_{1,max}$.

The total temperature variation of a parameter P across a temperature range R can be obtained from its temperature coefficient TC_P as follows:

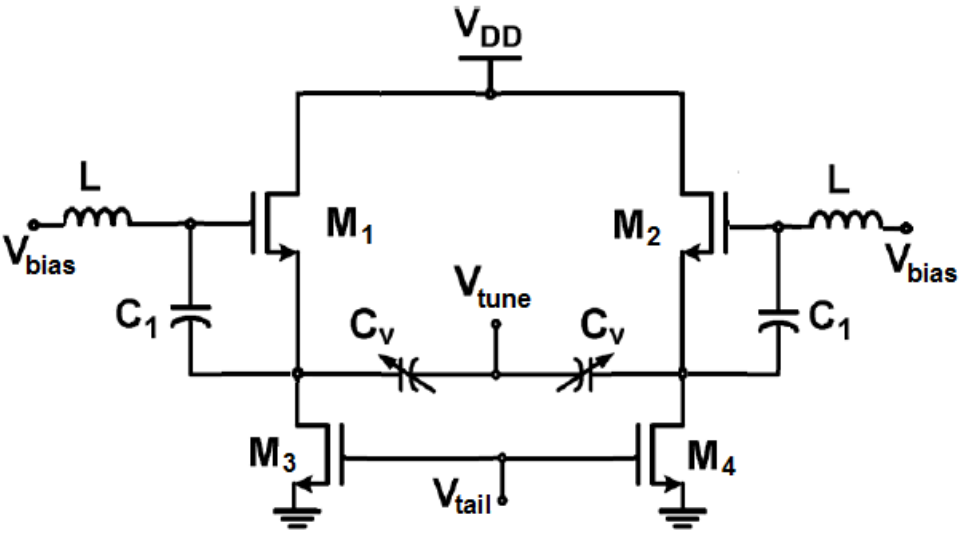


FIGURE 4.2: Differential Colpitts Oscillator

$$\Delta P = P.R.TC_P \tag{4.21}$$

The relation presented by 4.20 should be held under temperature variation for the start-up condition to stay valid:

$$(C_2' + \Delta C_2') < (\frac{(g_m + \Delta g_m)(Q_L + \Delta Q_L)}{(\omega_{osc} + \Delta\omega_{osc})} - (C_1' + \Delta C_1')) \tag{4.22}$$

The minimum value of C_2' ($C_{2,min}'$) corresponds to the maximum possible tuned frequency ($\omega_{osc,max}$). $C_{2,min}'$ is constrained by the implemented C_{var} versus V_{tune} characteristic and is related to the required V_{osc} in (4.5). Since C_1' and C_2' are ac coupled, V_{osc} varies with supply voltage. The maximum value of C_2' ($C_{2,max}'$) corresponds to the minimum tuned frequency ($\omega_{osc,min}$). It is constrained by the phase noise requirements. Low phase noise requires maximizing C_1' and the ratio of (C_1'/C_2') [7]. $C_{2,max}'$ should satisfy (4.20) and (4.22) for the start-up condition.

4.4 Design and Simulation

In order to verify the derived design equations, $24.2GHz$ single-ended and $23.2GHz$ fully differential CD Colpitts oscillators are designed using TSMC $65nm$ RFIC models. The single-ended Colpitts is based on Fig. 4.1(a), while the fully differential is shown in Fig. 4.2 with a tuning voltage V_{tune}.

TABLE 4.1: Colpitts Oscillators Design Operators

Device	**Size**
$M_{1,2}$	120μ/60n
$M_{3,4}$	40μ/130n
L (Spiral)	1 turn 256μ/240u
$C_{1,2}$ (MOM)	W/finger= 100nm array=32X32 Multlply= 10
C_v (MOS varacror)	W/finger= 1.6 μm L/finger=400nm finger/group=4, group=3 Multiply= 17

The analysis presented in section II can be applied to the differential Colpitts as half circuit representation [12]. The capacitors $C_{1,2}$ are Metal-Oxide-Metal (MOM) capacitors. MOS varactor C_{var} replaces C_2 in Fig. 4.4. The inductor L is a single turn spiral inductor. Table 1 shows the values of designed parameters.

Capacitors $C_{1,2}$ and the L used in the PDK tool have positive TC. Fig. 4.3(a) shows the frequency versus temperature for the single-ended Colpitts oscillator. The curve has negative temperature dependency, as expected based on (4.14). C_2 is swept from $0.5C_1$ to C_1 changing the frequency up to $26.69GHz$ as in Fig. 4.3(b). Fig. 4.3(c) shows the frequency versus temperature for the differential Colpitts oscillator. The graph shows positive temperature dependency. It is due to the negative temperature dependency of a voltage dependent parameter that builds the varactor model. Fig. 4.3(d) shows the frequency versus V_{tune}. The effective V_{tune} is above $1V$, limited by the circuit biasing and the type of the varactor that is available in the PDK tool. The tuning range is within $22.8-23.8GHz$. It covers

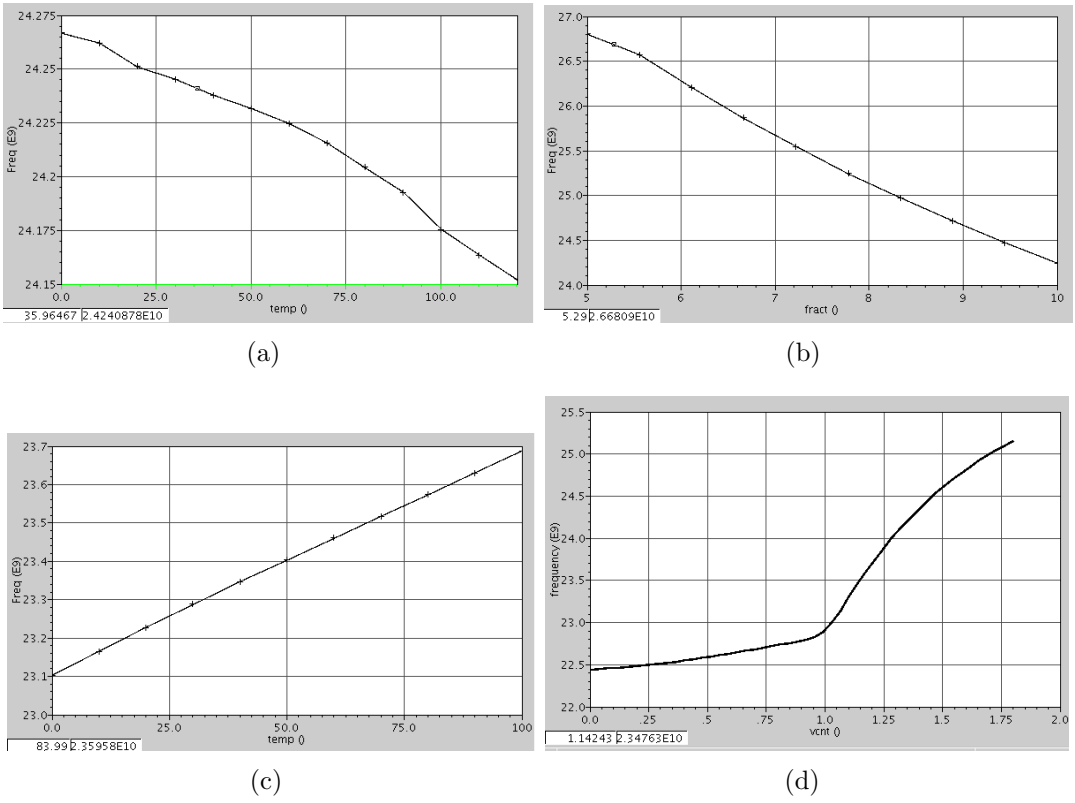


FIGURE 4.3: Simulation Results. (a) Frequency vs. Temperature for Single-ended Colpitts. (b) Frequency vs. C_2 for Single-ended Colpitts. (c) Frequency vs. Temperature for Differential Colpitts. (d) Frequency vs. V_{tune} for Differential Colpitts.

the frequency drift of $23.1 - 23.6GHz$ due to temperature change within $0 - 80°C$. It is interesting to note that the frequency temperature dependency for the two types of oscillators is opposite, due to different capacitor type.

4.5 Conclusion

The presented analysis contributes directly to the Coplitts oscillator design methodology. The shift of the nominal frequency due to process and temperature variations is usually compensated separately. The derived equations (4.11), (4.14), (4.15), (4.16), (4.18), (4.20), and (4.22) serve as design criterion. The presented analysis allows the designer to pinpoint the effect of the process and temperature

deviation prior to design for compensation. Throughout the analysis, C_1' and C_2' are treated separately to allow studying the behavior of the tuning capacitor regardless of the implementation type. The chosen tuning range has to be larger than the frequency shift of the uncompensated oscillator within the target temperature range. The value of the tuning capacitor is constrained by the required tuning range, amplitude of oscillation in addition to the start-up requirements.

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Chapter 5

A Varactor-less DCO with $7\ GHz$ Tuning Range for $77\ GHz$ Automotive Radars

5.1 Introduction

Automotive radar sensors are mounted around vehicles to enable a 360° safety zone. While millimeter-wave (mm-wave), infrared, laser, and ultrasonic sensors have been proposed, the mm-wave automotive sensor offers superior robustness against extreme weather environments such as temperature, snow, fog, and rain [1].

The automotive Short Range Radar (SRR) detects objects in the distance range of 0.15-30 m, enabling pre-crash sensing, blind-spot detection, and collision avoidance. On the other hand, the automotive Long Range Radar (LRR) is primarily used for Automatic Cruise Control (ACC), which senses long distance range of 10-250 m.

The Frequency Modulated Continuous Wave (FMCW) method is usually utilized in automotive radar transceivers, which calls for a linear frequency sweep to measure the range and velocity of objects [2]. The accuracy of the measurement in FMCW radar depends on the linearity of the frequency sweep generated by the frequency synthesizer, which in turn requires linearizing the DCO frequency response. Non-linearity in the sweeping range widens and shifts the peaks along the frequency axis, which increases the estimation variance and introduces a systematic bias in distance estimation [2].

5.1.1 Motivation

CMOS is an appealing technology due to its low cost and potential for System-on-Chip (SoC) integration [3]. CMOS automotive transceivers for automotive radar have been reported in [1], [4]. The typical distance resolution for commercial SRR and the LRR are 10 cm and 50 cm respectively [2]. The mm-wave automotive radar operating bands are located near 24 GHz or 77 GHz. The wavelength of the 77 GHz W-band is smaller than that of the 24 GHz K-band automotive radar. The significant reduction in the wavelength leads to a more compact size allowing for further integration [4].

The All-Digital-Phase-Locked-Loop (ADPLL) is an attractive system architecture for realizing a frequency synthesizer in the W-band. The digital implementation for the loop-filter allows full integration to provide scalability with the technology and total loop parameter reconfigurability such as loop bandwidth and phase margin [5]. The DCO is the heart of ADPLL and its application in FMCW radar mandates low Phase-Noise (PN) and wide Tuning Range (TR) [6].

5.1.2 Our Contribution

In [7], we report a 77 GHz DCO with 5 GHz linear TR, which alleviates the need for an ideal switch. This chapter expands and optimizes the work in [7] to present more detailed design considerations and rigorous analysis for the proposed ML-DCO.

The contributions of this chapter are as follows.

1. We design a varactor-less DCO with TR as wide as 7 GHz to allow for Process, Voltage, and Temperature (PVT) calibration while still covering the bands of the 77 GHz automotive SRR and LRR.

2. We demonstrate the operation of the varactor-less new frequency step generating mechanism, which can potentially open a new era for the design of a linear wide TR mm-wave DCO.

3. We analyze the amplitude stability across the TR, which is enforced by the new tuning mechanism without the need for extra circuitry to automatically stabilize the amplitude. Moreover, amplitude stability is not in trade-off with the wide TR.

4. We evaluate the innovative linear coarse, intermediate and fine-tuning steps and the DCO performance with post-layout simulations.

The rest of this chapter is organized as follows. Section 5.2 details the design challenges. Section 5.3 presents related work in overcoming the trade-off in the design requirements. The Colpitts oscillator and the negative resistance models are presented in Section 5.4. Section 5.5 discusses design constraints, drawing attention to the tuning constraints and analyzing the amplitude stability. The mechanism of the new frequency step generator is presented in Section 5.6. Section 5.7 describes the circuit design. The corners, Monte Carlo, post-layout simulations, and fabrication measurements for the first prototype are reported in section 5.8.

5.2 Design Challenges

Low PN oscillators call for Colpitts or LC-tank based topologies. The start-up condition for the conventional LC-tank topology is more relaxed than the Colpitts. However, the LC-tank topology suffers from narrow TR, low output power, and higher PN [8–10]. Moreover, the TR of the LC-tank operating beyond 20 GHz is inadequate since the binary-weighted band-switching technique is no longer applicable [11].

Range resolution (ΔR) is a crucial requirement of the FMCW radar, which depends on the transmitter bandwidth and consequently on the TR of the local oscillator. The bandwidth (B) and ΔR are related by $\Delta R = c/2B$, where c is the speed of light. The 77 GHz FMCW automotive radar mandates a DCO with 5 GHz TR to realize ΔR of 3 cm.

The frequency of oscillation for a resonator based oscillators is expressed by:

$$f_o = \frac{1}{2\pi\sqrt{LC_L}} \tag{5.1}$$

where f_o is the oscillating frequency, L is the tank inductor, and C_L is the effective capacitor, which appears in parallel with the L.

By taking the derivative $\frac{\delta f_o}{\delta C_L}$, the frequency resolution is approximated by:

$$\Delta f_o = \Delta C_L \frac{f_o}{2C_L} \tag{5.2}$$

where the frequency resolution $\Delta f_o \approx \delta f_o$ and $\Delta C_L \approx \delta C_L$ is the minimum capacitance step.

Since Δf_o in Eq. (5.2) is proportional to ΔC_L, the fine frequency step gets worse in higher frequencies if the minimum unit capacitor is not decreased by the same

factor. Therefore, the fine frequency step becomes an issue in the design of W-band DCO [12].

Another significant issue related to the PN is the quality factor of the LC tank, which is expressed by:

$$\frac{1}{Q_T} = \frac{1}{Q_L} + \frac{1}{Q_{C_L}} \tag{5.3}$$

where Q_T, Q_L, and Q_{C_L} are the quality factors of the tank, the tank inductor, and the effective capacitor respectively.

The value of Q_L tends to increase with frequency, while Q_{C_L} decreases with frequency [13].

When the radar is operating in the W-band frequency, the effect of Q_{C_L} dominates Q_T. The PN performance is affected by the degradation of the Q_T and is a major challenge in designing W-band DCOs [8].

The linearity and the quality factor of the NMOS transistor in N-well Accumulation MOS (AMOS) varactors are better than the transistor or the diode varactors [13]. However, AMOS is sensitive to PVT variations. Here, the AMOS is avoided in the design of mm-wave DCOs due to the significant drop in its quality-factor at mm-wave frequencies which severely degrade the PN performance [14]. Moreover, DCOs tuned with switched AMOS suffer from poor frequency resolution. As an example, if L and C_L of a 77 GHz LC-tank DCO are 80 pH and 53 fF respectively, then a fine-tuning step of 1 MHz requires a minimum varactor size ΔC_L=1.4 aF that may not be justified in the CMOS process.

A unit capacitor cell consisting of an NMOS switch connecting two series MoMs or Metal-Insulation-Metal (MiM) capacitors are often used to provide the large tuning step for the DCOs [1, 15]. While this configuration could be utilized to facilitate wide tuning requirements, it is restricted for the coarse tuning. The precision and

matching of the minimum switched MoM capacitor for the fine tuning is affected by the series parasitic capacitance of the NMOS switch and the interconnections being higher than minimum MoM capacitance [6].

5.3 Related Work

In order to overcome the design challenges in Section 5.2, the effect of the switch and varactor loading were addressed in [11] by proposing a nonuniform standing-wave oscillator topology with switched transmission lines. The reported TR and centre frequency are 20% and 40 GHz respectively. However, the wide TR is non-linear and is segmented into several smaller linear tuning regions. Moreover, the distributed VCO structure is at the expense of area and power consumption.

[6] propose a varactor-less CMOS 60 GHz DCO with 6 GHz TR. The magnetic field of the resonator is disturbed by digitally varying the position of the metal strips (acting as switched capacitors) distributed beneath the resonator. The reported PN is limited to -94 dBc/Hz. The disturbed field can deteriorate the quality-factor of the inductor and increase the design complexity. One of the conventional techniques used to reduce the substrate loss and to improve the inductor quality factor is to place a patterned ground shield below the inductor [8], [16]. Transformer coupling was also proposed by [6] for the fine-tuning. However, a small coupling factor is needed to scale down the switched capacitor turning it to be sensitive to process variations.

While MOS switches are not used in [12], a 60 Hz CMOS DCO with 14% TR is designed based on C-2C switched capacitor ladder technique. However, non-linearity is still present, and it was assumed that it would be calibrated later in the digital domain.

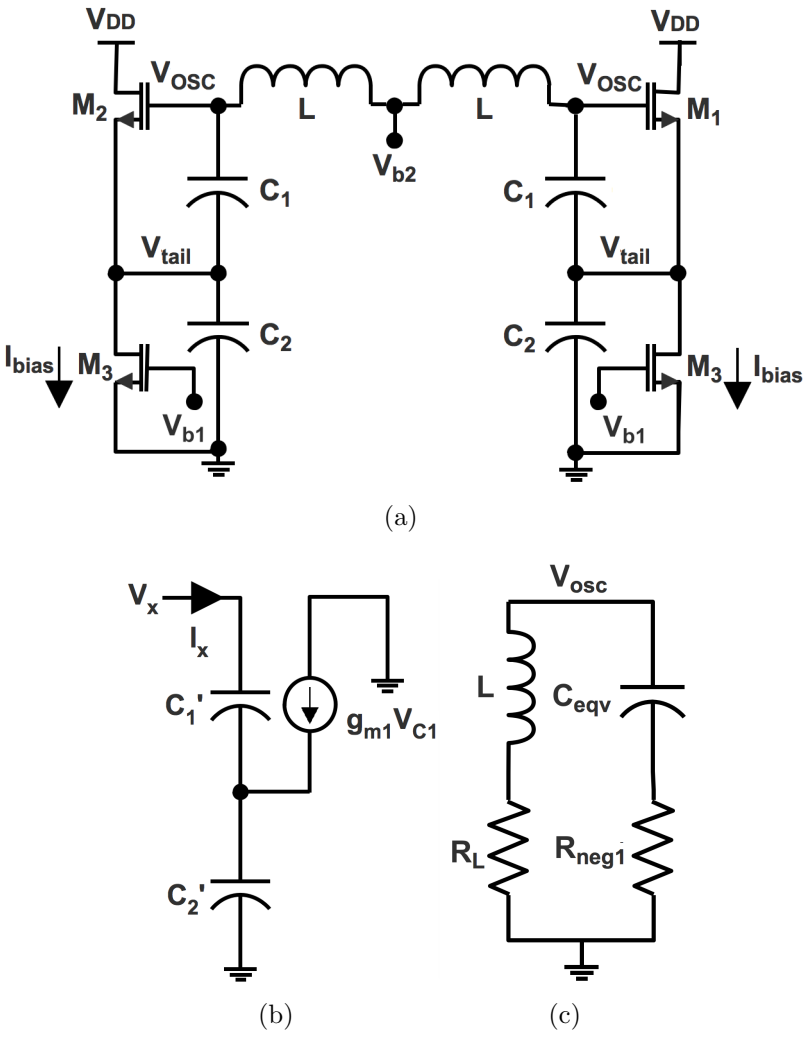


FIGURE 5.1: (a) Differential Colpitts schematic. (b) Small-signal impedance model looking into the gate of M_1. (c) Colpitts small signal negative resistance based model.

The variation of the amplitude of oscillation (V_{osc}) is another issue to be avoided in wide TR DCOs. Stabilizing V_{osc} at the steady-state oscillation suppresses the amplitude-to-phase conversion [17]. However, V_{osc} variation changes the phase of oscillation that appears in the impulse response of the DCO [18]. Moreover, the decrease in V_{osc} leads to an increase in the PN [19].

The amplitude of an mm-wave VCO is stabilized in [20] by employing vackar topology. However, the amplitude stability is in trade-off with the TR limitation and the TR is limited to just 1.7%. The work in [21] reports a 4.56% amplitude

variation for 24 GHz SRR that is not in trade-off with wide TR requirement of 29%. The Colpitts-Clapp topology is implemented and an automatic amplitude stabilization circuitry is added to adjust the biasing current based on the coarse tuning bits.

5.4 Colpitts Negative Resistance Model

Fig. 5.1(a) shows a common-drain differential Colpitts oscillator, where the capacitor C_2 is the tuning capacitor of the Colpitts oscillator. The impedance (Z_{in}), looking into the gate of M_1 is derived using the half circuit model shown in Fig. 5.1(b), and can be expressed by:

$$Z_{in} = \frac{V_x}{I_x} \cong \frac{1}{j\omega C_1'} + \frac{1}{j\omega C_2'} - \frac{g_{m1}}{\omega^2 C_1' C_2'} \tag{5.4}$$

where C_1' is the combination of the feedback capacitor between the gate and the source of the switching device M_1 and the parallel parasitic capacitors of M_1 ($C_1' = C_1 + C_{gs1} + C_{gd1}$), C_2' represents the tuning capacitor of the Colpitts and the associated parallel parasitic capacitors ($C_2' = C_2 + C_{sb1}$), and g_{m1} is the small signal transconductance of M_1.

Equation (5.4) reveals that Z_{in} is equivalent to a series combination of C_1' with C_2' and a negative resistance R_{neg1} that is equal to:

$$R_{neg1} = -\frac{g_{m1}}{\omega^2 C_1' C_2'} \tag{5.5}$$

The small-signal negative resistance model is shown in Fig. 5.1(c). The lossy inductor L in series with the parasitic resistance R_L is connected to Z_{in}.

If $\mid R_{neg1} \mid > R_L$, instability is enforced and oscillation starts, where V_{osc} grows-up till it is stopped by non-linearity of the circuit.

At the frequency of oscillation, the inductor L resonates with C_1' in series with C_2' and the central frequency $f_{o_{colpitts}}$ is given by:

$$f_{o,colpitts} = \frac{1}{2\pi\sqrt{L(\frac{C_1'C_2'}{C_1'+C_2'})}} \tag{5.6}$$

5.5 Design Considerations

In this section, we illustrate the design considerations for tuning at the W-band operation frequency. We explain the MOS Transmission Gate (TG) switch Model and analyze the oscillation amplitude to establish independence from the tuning capacitors and remain stable across the wide TR.

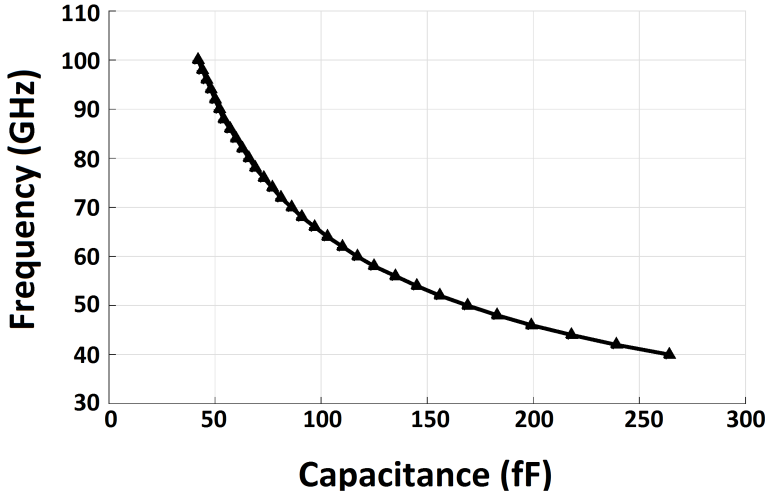
5.5.1 Tuning Constraints

While the Colpitts oscillator in Fig. 5.1(a) is tuned by C_2, the ML-DCO [7] utilizes the capacitors C_1 and C_2 together to perform the tuning functionality by setting $C_1 = C_2 = C$. At the resonance frequency, C_{eqv} (C_1' in series with C_2') is converted to an equivalent parallel capacitor (C_L) as follows:

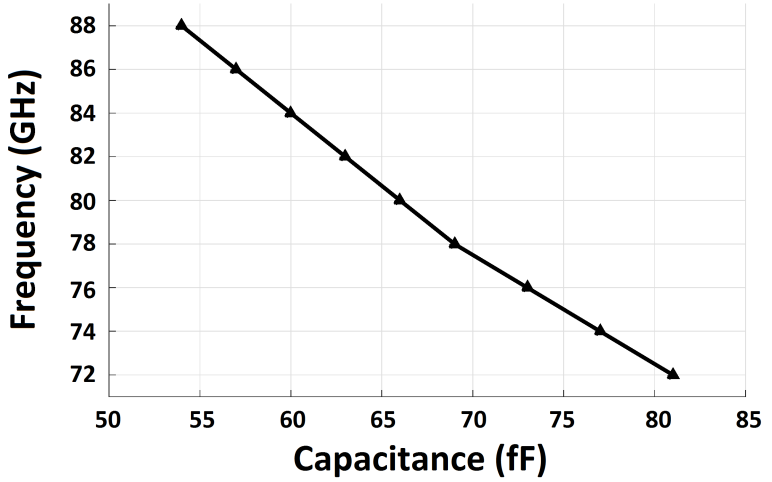
$$C_L = C_{eqv}Q_{C_{eqv}}/(1 + Q^2_{C_{eqv}}) \tag{5.7}$$

where Q_{C_eqv} is the quality factor of C_{eqv}. Such that for high $Q_{C_{eqv}}$, $C_L \cong C_{eqv} = \frac{1}{2}C$.

The frequency of oscillation is similar to the LC-tank as given in Eq. (5.1), and shows a non-linear relation between f_o and C_L, assuming that L is kept constant. The plot in Fig. 5.2 (a) shows f_o vs. C_L where L is fixed at 60 pH. The non-linear relations can be considered as a piecewise linear function.



(a)



(b)

FIGURE 5.2: (a) Frequency versus C_L for LC-tank and ML-DCO. (b) Piecewise linear regions.

Fig. 5.2 (b) shows two linear segments in the range of $72-78\ GHz$ and $80-88\ GHz$ that can cover 16 GHz TR. The piecewise linear function for the two segments can be defined by:

$$f = \begin{cases} 124 - 0.7C_L & : 54 \leq C_L \leq 66 \\ 112 - 0.5C_L & : 69 \leq C_L \leq 81 \end{cases}$$

The units for f and C_L are GHz and fF respectively. The higher the frequency, the sharper is the slope which calls for smaller coarse step.

As an example, working in the linear segment $f = 112 - 0.5\ C_L$, a coarse step of $0.2\ GHz$ requires $0.4\ fF$ change in C_L which is translated to a change of $0.8\ fF$ in C. The minimum MoM/MIM provided by the foundry is typically limited to a few fF. As an example, the minimum MoM size in the 65 nm TSMC process is $2.16\ fF$ and this capacitive change in C corresponds to $1.08\ fF$ change in C_L that results in $0.5\ GHz$ coarse step for the same line segment.

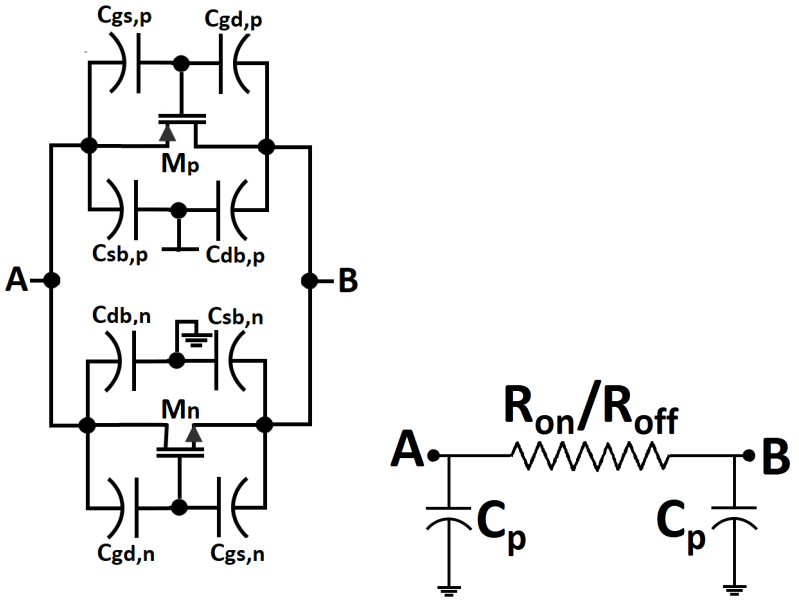
Tuning capacitors are partitioned into an overlapped Coarse Bank (CB), an Intermediate Bank (IB), and a Fine Bank (FB) to maximize linearity in the step size of the tuning characteristics. A large coarse step relaxes the number of coarse tuning bits, but also leads to additional intermediate and fine-tuning bits.

The resolution (Δf_o) defines the fine step. Based on Eq. (5.2), for $\Delta f_o = 1\ MHz$ and with $f_o = 78\ GHz$ and $C_L = 69\ fF$, $\Delta C_L = 1.8\ aF$ and hence ΔC as low as $3.6\ aF$ should be realized. Thus the realization of the three tuning banks capacitors are the major constraints in the design of a W-band DCO.

5.5.2 Transmission Gate Switch Design Considerations

The parasitic capacitors associated with the PMOS and NMOS devices (M_p and M_n) of the MOS TG switch are shown in Fig. 5.3(a).

During the OFF TG state, M_n and M_p are turned OFF. The TG off-resistance (R_{off}) is high and is equal to the parallel combination of the substrate resistance R_{sub} and the n-well resistance (R_{nw}). The parasitic capacitors at the terminals



(a) (b)

FIGURE 5.3: Transmission Gate equivalent circuits (a) Parasitic capacitors contribution in the TG. (b) Equivalent ON/OFF TG models.

A, B are given by

$$C_{A_{off}} = C_{gs_p} + C_{gd_n} + C_{sb_p} + C_{db_n} \tag{5.8}$$

$$C_{B_{off}} = C_{gd_p} + C_{gs_n} + C_{sb_n} + C_{db_p} \tag{5.9}$$

Advanced CMOS technology offers placing the switch inside an isolated deep n-well to add a large resistance of few $K\Omega$ in series with the substrate resistance to improve isolation.

At the ON state, at least one of the MOS switches is turned ON. Since $M_n||M_p$, the TG on-resistance (R_{on}) can be expressed as

$$(R_{on_p}||R_{on_n}) \leq R_{on} \leq (R_{on_n} or R_{on_p}) \tag{5.10}$$

where R_{on_n} and R_{on_p} are the on-resistance for M_n and M_p respectively.

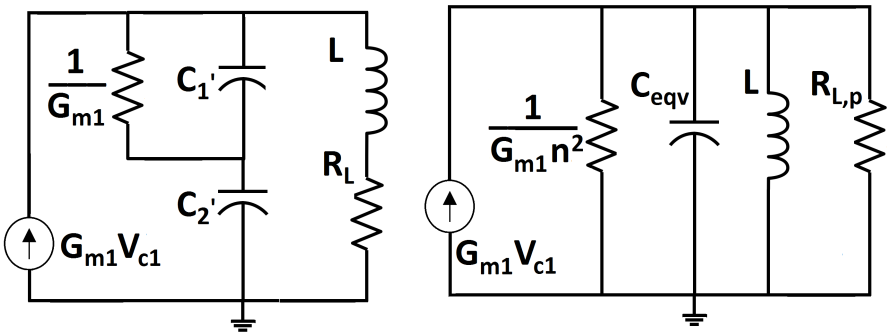


FIGURE 5.4: Steps to derive the ML-DCO large signal model. (a) Circuit to obtain the ML-DCO large signal model. (b) ML-DCO large signal model.

The Nanoscale CMOS technology provides improved symmetric switch topologies that make use of the improved p-MOSFETs. Equal NMOS and the PMOS sizes present the same parasitic capacitors and thus C_p can be defined to be the equivalent parasitic capacitor that appears at the terminal A and B.

$$C_p = C_{gs} + C_{gd} + C_{sb} + C_{db} \tag{5.11}$$

The TG ON/OFF model is shown in Fig. 5.3(b).

5.5.3 Oscillation Amplitude: Impact and Stability Analysis

If the start-up condition is satisfied, such that $\mid R_{neg1} \mid > R_L$, then oscillation continues steadily until non-linearity forces the signal to stop growing. The steady-state oscillation amplitude is an important characteristic and can have a significant impact on other neighboring system blocks.

The describing function model in [22] approximates the large signal transconductance (G_m) of the steady-state oscillation by:

$$G_{m1} \approx \frac{I_{1,peak}}{V_{C1}} \approx \frac{2I_{bias}}{V_{C1}} \approx \frac{2I_{bias}}{nV_{osc}} \tag{5.12}$$

where $I_{1,peak}$ is the peak of the pulse current in $M_{1,2}$, I_{bias} is the biasing current, V_{osc} is the amplitude of oscillation, V_{C1} is the amplitude of the gate-source voltage, and $n = C_2/(C_1 + C_2)$. The function model approximates $I_{1,peak} \approx 2I_{bias}$.

The Large signal representation, based on the NMOS T model and shown in Fig. 5.4 (a) is employed to calculate the oscillation amplitude. The tapped capacitors C_1' and C_2' with $1/G_{m1}$ are transformed to a capacitor C_{eqv} (C_1' in series with C_2') in parallel with a resistor $1/G_{m1}n^2$ [23].

At the resonanet frequency, the equivalent parallel resistance of the inductor L can be derived from the series losses equivalent resistor R_L by:

$$R_{L,P} = R_L(1 + Q_L^2) \cong R_L Q_L^2 \tag{5.13}$$

where $R_{L,P}$ is the losses equivalent parallel resistance of the L. With $Q_L \gg 1$, $Q_L = \frac{\omega_o L}{R_L}$, and $\omega_o = 2\pi f_o$, $R_{L,P}$ can be approximated by:

$$R_{L,P} \cong R_L Q_L^2 = Q_L \omega_o L \tag{5.14}$$

The inductor losses characterized by R_L eventually become a function of the oscillating frequency due to the induced losses from the substrate eddy current and the skin effect.

Fig. 5.4(b) shows the transformed model. The total parallel resistance is expressed as follows:

$$R_{total} = (1/G_{m1}n^2) \| R_{L,P} \tag{5.15}$$

At ω_o, the amplitude V_{osc} is given by:

$$V_{osc} = 2I_{bias}R_{total} = 2I_{bias}\frac{R_{L,p}}{1 + G_{m1}n^2R_{L,P}} \tag{5.16}$$

Substitution of Eq. (5.12) in (5.16) and rearranging the terms result in:

$$V_{osc} = 2I_{bias}R_{L,P}(1 - n) = I_{bias}R_{L,P} \tag{5.17}$$

where n=1/2 in the ML-DCO. Finally substitution of $R_{L,p}$ from Eq. (5.14) results in:

$$V_{osc} = I_{bias}Q_L\omega_o L \tag{5.18}$$

To investigate amplitude stability with the TR, ω_o is modified by $\Delta\omega_o$ with $\Delta\omega_o \ll \omega_o$. This change results in modification of $V'_{osc} = I_{bias}Q_L\omega'_o L$, where V'_{osc} is associated with the incremental increase of $\omega'_o = \omega_o + \Delta\omega_o$ enforced by the incremental change in $C'_L = C_L + \Delta C_L$.

The normalized amplitude is:

$$\frac{V'_{osc}}{V_{osc}} = \frac{(\omega_o + \Delta\omega_o)^2}{\omega_o^2} = 1 + 2\frac{\Delta\omega_o}{\omega_o} + \frac{\Delta\omega_o^2}{\omega_o^2} \tag{5.19}$$

Similarly, the ratio of $\frac{(\omega_o+\Delta\omega_o)^2}{\omega_o^2} = \frac{C_L}{C_L+\Delta C_L}$ can be derived based on the relation $\omega_o^2 = \frac{1}{LC_L}$ and expressed by:

$$(1 + \frac{\Delta\omega_o}{\omega_o})^{-2} = 1 + \frac{\Delta C_L}{C_L} \tag{5.20}$$

Since $\Delta\omega_o/\omega_o$ is much smaller than one, the left side of Eq. (5.20) can be approximated by the first-order Taylor expansion that results in:

$$1 - 2\frac{\Delta\omega_o}{\omega_o} = 1 + \frac{\Delta C_L}{C_L} \tag{5.21}$$

Therefore

$$\frac{\Delta\omega_o}{\omega_o} = -\frac{\Delta CL}{2C_L} \tag{5.22}$$

The last term in Eq. (5.19) is $\ll 1$ and can be ignored. With the substitute of Eq. (5.22) in Eq. (5.19), the normalized amplitude of the ML-DCO can be approximated to:

$$\frac{V'_{osc}}{V_{osc}} = \frac{(\omega_{osc} + \Delta\omega_o)^2}{\omega_o^2} = 1 - \frac{\Delta C_L}{C_L} \approx 1 \tag{5.23}$$

for $\Delta C_L \ll C_L$.

Therefore, the amplitude of oscillation of the ML-DCO can be stable across the TR being independent on the tuning capacitors.

Stabilizing the amplitude is important for suppressing the amplitude-to-phase conversion [20]. Amplitude stability needs to be addressed in the design of the frequency synthesizer. The pre-scaler (or divider) is a neighboring system block whose performance is affected by the DCO amplitude stability. If the DCO is part of a synthesizer inside the receiver, then the conversion gain of the mixer would vary if the DCO amplitude changes widely.

5.6 New Frequency Step Generating Mechanism

Fig. 5.5(a) presents the proposed frequency step generating mechanism formed by two special capacitive structures (C_s) connected in series. Each C_s consists of two unit capacitors (C_u) and a TG, where C_u is the minimum available MoM capacitor supplied by the foundry. The TG connects the bottom plates of C_u, while the top plates are shorted together. In constructing the TG, deep-n-well low V_{th}, which is available in the process design kit, and minimum size devices are used for both of M_n and M_p to keep the minimum size parasitic capacitors.

For the sake of obtaining an intuitive analysis, R_{on} in the model of Fig. 5.3(b) is assumed too small to be replaced by a short circuit. For the same reason, it is assumed that R_{off} is large enough to disconnect the TG terminals A and B. The

resulting frequency step generating units at the ON and OFF states are shown in Fig. 5.5(b) and(c) respectively.

In 65 nm CMOS technology, the value of the parasitic capacitors C_{gs}, C_{sb}, and C_{db} for $1\mu m/65nm$ NMOS and PMOS devices is 0.7 fT. C_{gd} is 0.4 fT and C_u is around 2 fF [8]. C_p per $1\mu m$ wide device in Eq. (5.11) comes to be 2.5 fF, which is translated to 0.5 fF by scaling the width down to 200 nm. The equivalent ON and OFF capacitor of the frequency step generator in Fig. 5.5 (b), (c) are 2.22 fF and 1.58 fF respectively. The resulting $\Delta C = 0.64$ fF is translated to $\Delta f = 0.4$ GHz in Eq. (5.2) for $f_o = 82$ GHz and $C_L = 63$ fF. The frequency step is generated utilizing the minimum size MoM and low V_{th} devices that can be supplied by the foundry.

5.7 Circuit Design of the Proposed 77 GHz DCO

The W-band ML-DCO is designed based on the proposed topology in Fig. 5.1. Fig. 5.6 shows the schematic of the W-band ML-DCO. The switching NMOS RF devices (M_1, M_2) of 60 nm length and 20 um width provide sufficient gain to sustain the oscillation. The transistors M_1 and M_2 are biased at the minimum noise figure current density of 0.15 $mA/\mu m$ to obtain low PN.

A single turn central tap tank inductor (L_1) with 120 pH is selected and implemented in Metal layer 9 of the 65 nm CMOS technology. It achieves Q_L of 49 at 82 GHz. The current source tail is replaced with a resistor (R_2), a capacitor (C_t), and an inductor (L_2) to filter out the noise introduced by the bias circuitry [8]. The output is taken from the drain such that an output buffer is not needed and the output power is increased with the drain inductor (L_3) without reducing the headroom for the transistor [24].

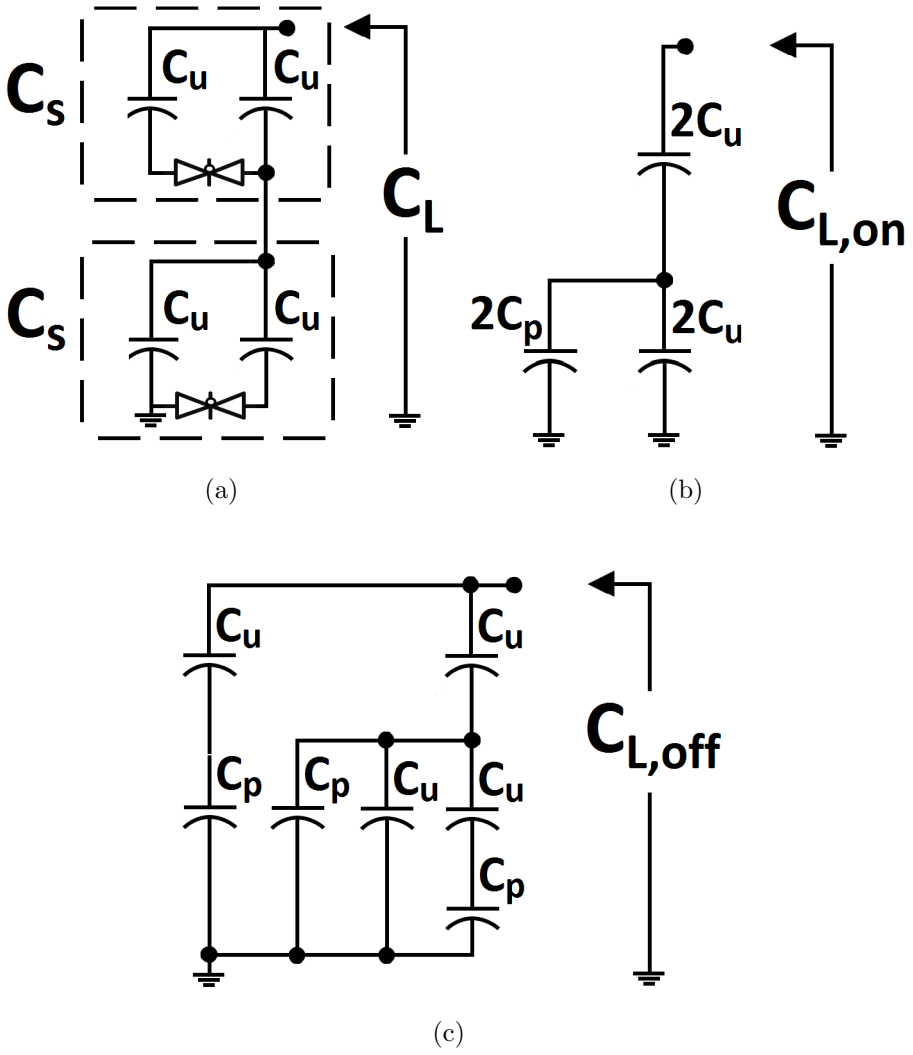


FIGURE 5.5: (a) Frequency step generating mechanism. (b) The frequency step generator at the ON state. (c) The frequency step generator at the OFF state.

The ML-DCO offers three-stage tuning; the coarse, intermediate, and fine-tuning networks, which bridge the gap between the coarse and the fine frequency step size. Thermometer encoding is employed to ensure monotonicity, which controls the new tuning mechanism.

The three tuning networks providing the coarse, intermediate, and fine-tuning steps are configured as shown in Fig. 5.7. Intermediate and fine-tuning steps are accomplished by adding more C_u in series to reduce the total effective capacitance and hence the step. Placing C_u in series with the TG enhances the intermediate

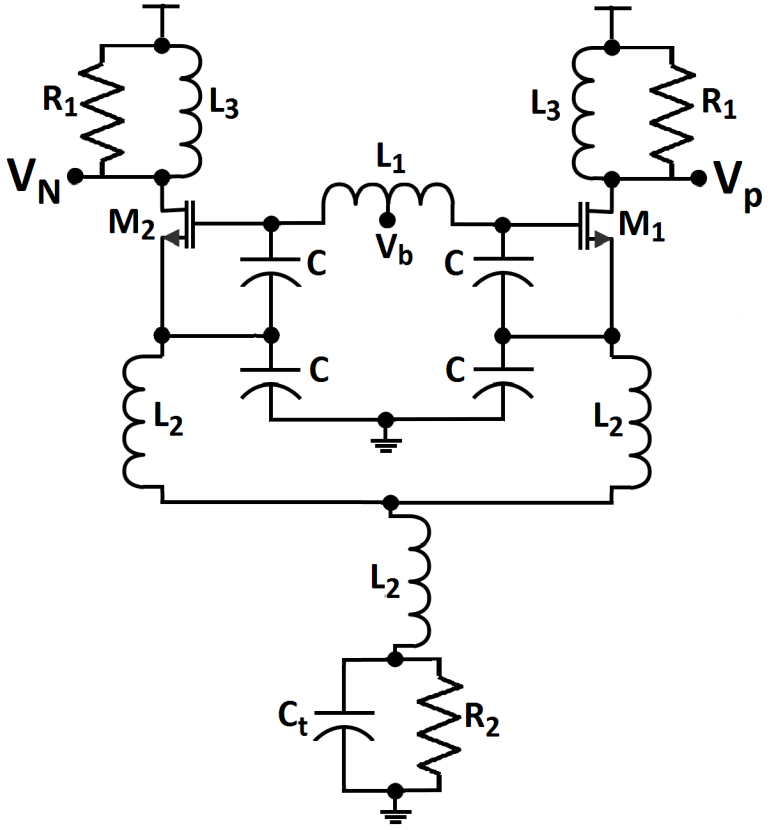


FIGURE 5.6: Schematic of the proposed 77 GHz ML-DCO.

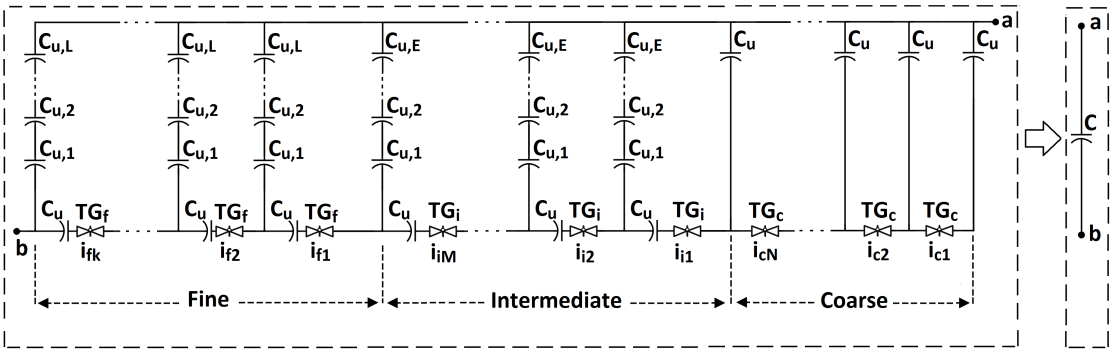


FIGURE 5.7: Tuning network banks.

and the fine steps to maintain the consistent effect. If all the leftmost TG in the network is OFF while the rest are ON, then the frequency is stepped up by flipping next TG to the OFF state.

The thermometer indices are (i_{c1}-i_{cN}), (i_{i1}-i_{iM}), and (i_{f1}-i_{fK}) for the coarse, intermediate, and fine network respectively. The unit MoM capacitor (C_u) is 2.16 fF. The number of the series C_u to realize the intermediate and fine steps are E and L respectively. In this design, $N = M = K = 31$ for 5 binary bits controlling each network, while $E = 3$ and $L = 7$.

All the TGs incorporate symmetrical low threshold NMOS and PMOS devices. If the gate capacitors are equal, opposite charge packets injected by the NMOS and PMOS transistors of the TG cancel each other that results in minimal charge injection effect [25].

The width/length of the PMOS and NMOS transistors of all the TGs are identical in each tuning bank. The sizes of the transistors for the coarse (TG_c), the intermediate (TG_i), and the fine (TG_f) TGs are (200 nm/120 nm), (200 nm/60 nm), and (200 nm/60 nm) respectively. The length of TG_c is twice that of TG_i and TG_f to increase the coarse step enforced by increasing the effective parasitic capacitors.

The layout of the proposed ML-DCO is accomplished in 65 nm bulk CMOS process. The chip layout is shown in Fig. 5.8. The total chip area is 1 mm^2, which is pad limited. The ML-DCO core fits in a rectangular of 1.3 $mm \times 0.5$ mm. The power dissipation is 14 mW from a 1.2 V supply.

5.8 Simulation And Fabrication Measurement Results

Post-layout simulation is conducted to plot the coarse, intermediate, and fine tuning shown in Fig. 5.9, Fig.5.10, and Fig. 5.11 respectively. The coarse tuning

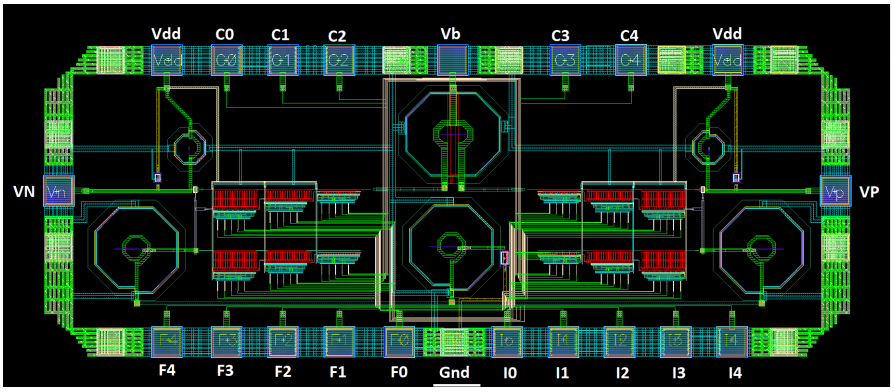


FIGURE 5.8: Chip layout of the proposed 77 GHz DCO

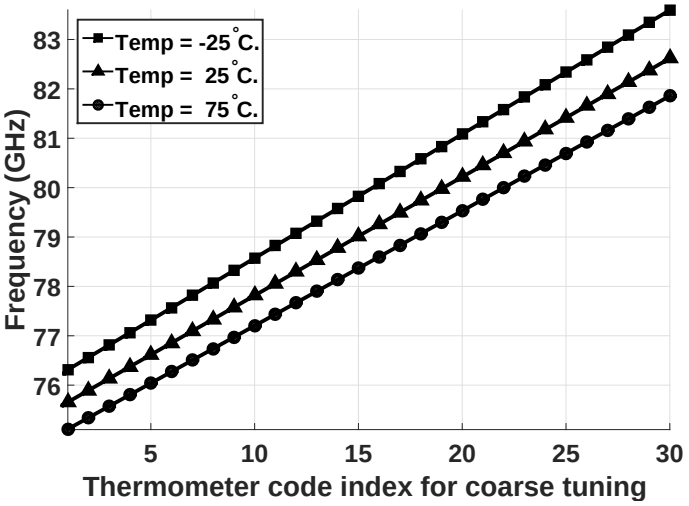


FIGURE 5.9: Coarse tuning for the ML-DCO.

is plotted in Fig. 5.9 in three different temperatures. At 25°C, the TR extends from 75.5 GHz to 82.5 GHz, and the ML-DCO realizes linear coarse tuning step at 220 MHz with less than 12% variation. The average linear coarse steps are 240 MHz and 211 MHz at $-25°C$ and 75°C respectively.

The linear intermediate tuning at each coarse thermometer code index ($C01-C29$) is plotted in Fig. 5.10 to provide 10 MHz intermediate step. More than 9% overlap between the adjacent intermediate tuning curves guarantees continuous tuning across the entire range.

Fig. 5.11 plots the fine-tuning step against the thermometer index while the ML-DCO is oscillating at three different frequencies, being 76 GHz, 77 GHz, and 81 GHz. The average fine steps are 385 KHz, 346 KHz, and 408 KHz when oscillating at 76 GHz, 77 GHz, and 81 GHz respectively. Thus a TR as wide as 7 GHz and a frequency resolution of 346 KHz are achieved simultaneously using the new mechanism.

Monte Carlo statistical analysis is performed in TSMC 65 nm to check the effect of the inter-die and the intra-die variations on the frequency and the amplitude of oscillation. A proper Monte Carlo configuration is set up by varying the process and mismatch of the NMOS and PMOS transistors in order to evaluate the effect of the inter-die and the intra-die variations on the oscillating frequency and the amplitude of oscillation. Simulations are performed under the minimum, middle and maximum index coarse tuning code of the oscillating frequency, with 1100 runs per simulation. The simulation results corresponding to these cases are presented in Fig. 5.12(a), (b), and (c) respectively. The mean (mu) oscillating frequencies for the minimum, middle and maximum indices are $75.508, 79.005, 82.506$ GHz and the standard deviations (sd) are $14, 13, 13.2$ MHz respectively. The process and mismatch statistical coefficient variation for all cases is less than 0.02%. The robustness is due to the uniqueness of the topology, which depends on varying C_1 and C_2 (Fig. 5.1) simultaneously throughout the tuning process that makes the frequency depends on ratio of capacitors and consequently less sensitive to process variations.

Monte Carlo simulation is also performed to check the process and mismatch fluctuation effect on the amplitude while the design is oscillating at 77 GHz. The results of the 1100 runs are depicted in Fig. 5.12(d). The values of mu and sd are 941 mV and 22 mV respectively. The amplitude varies by just 2.34% with process and mismatch for 1100 runs. All Monte Carlo simulations and subsequent analyses show Gaussian distributions, highlighting the robustness of the design. The results show that the proposed design is very promising.

Process corner analysis is performed to simulate the frequency, the current consumption, and the V_{osc}. The analysis is repeated for seven different coarse indexes ($C01$, $C05$, $C11$, $C16$, $C21$, $C26$, $C30$). The corners are the typical process at $25°C$ (Typ.), fast-best corner at $-25°C$ (F.B.), and slow-worst corner at $75°C$ (S.W.). The results are shown in Fig. 5.13. The frequency tuning across the entire range at the three process corners is presented in Fig. 5.13(a) and tabulated in Table 5.1. The TR is the same for all frequency corners and linearity is maintained. The highest current consumption of 16 mA appears in the F.B at $C26$ coarse index shown in Fig. 5.13(b). The maximum amplitude variation with process corners across the TR in Fig. 5.13(c) occurs at the S.W corner, and V_{osc} varies by 25% between 0.6 V and 0.75 V. At the Typ. corner, V_{osc} varies by 9% across the TR between 0.84 V and 0.94 V. The results of the process corner effect on PN are shown in Table 5.2. The analysis is conducted at 75.5 GHz, 79 GHz, and 82.5 GHz. The results show that the PN at 1 MHz offset frequency is better than -95 dBc/Hz among all cases.

Post-layout simulation for the PN at $-25°C$, $25°C$, and $75°C$ are presented in Fig. 5.14 corresponding to an oscillation frequency of 77 GHz. The PN at 1 MHz offset at $-25°C$, $25°C$, and $75°C$ is -98.73 dBc/Hz, -98.53 dBc/Hz, and -97.12 dBc/Hz respectively.

The first prototype resembles a half circuit of the differential ML-DCO in Fig. 5.6. It is implemented in TSMC 65 nm 1P9M CMOS process. The die photo is shown in Fig. 5.15. The prototype draws 6 mA current from 1.2 V supply. The core occupies an area of $700 \times 500 \mu m^2$.

Fabrication measurement is conducted to test the performance of the first prototype. Oscillating at 77 GHz, Fig. 5.16 shows the measured PN spectrum. The PN at 1 MHz offset is -96.32 dBc/Hz. Fig. 5.17 shows 4-bit coarse tuning and the measured PN ranging from -94 dBc/Hz to -96.55 dBc/Hz at a $1MHz$ offset throughout a linear tuning range from 76 GHz to 81 GHz.

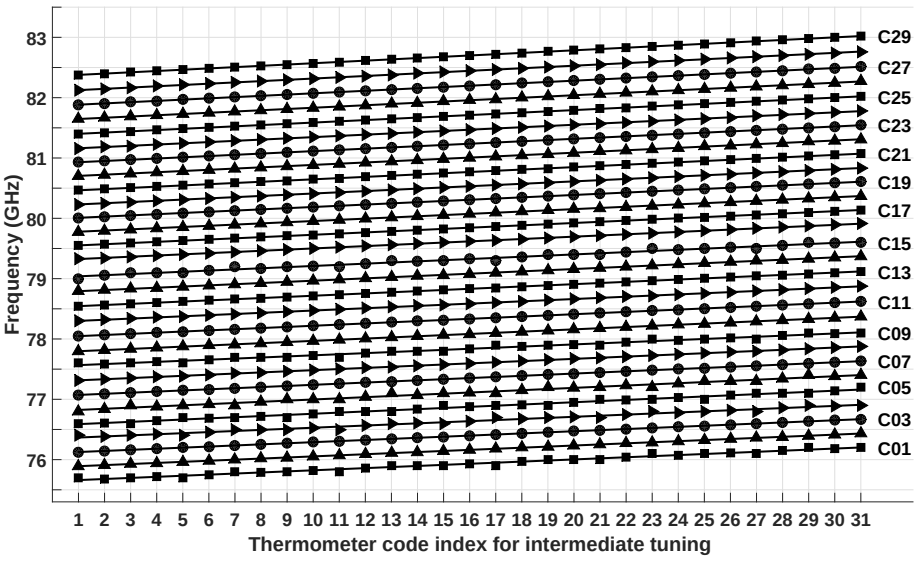


FIGURE 5.10: ML-DCO intermediate tuning curves for each coarse thermometer index tuning.

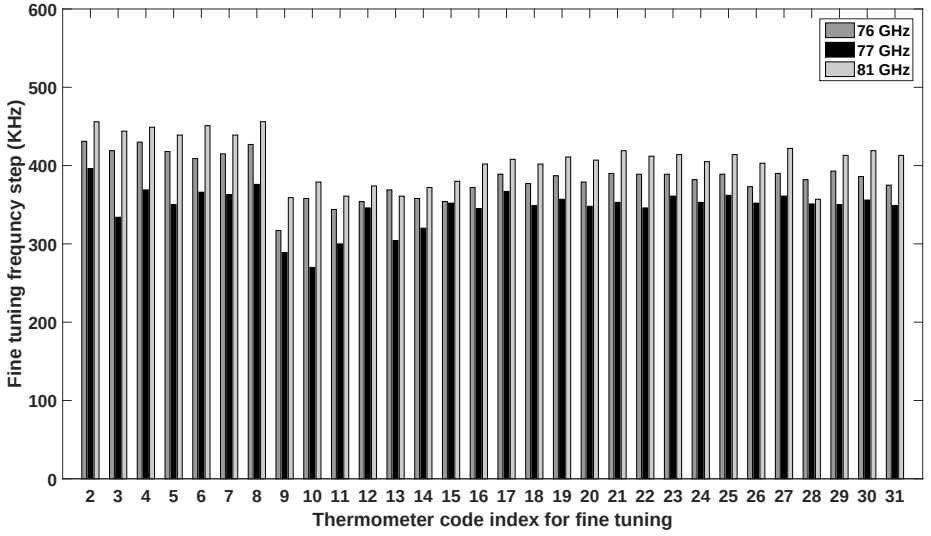


FIGURE 5.11: ML-DCO fine-tuning frequency steps in three different oscillating frequencies.

To quantify and compare the overall performance with other designs from the current literature, the Figure of Merit (FoM) and Figure of Merit for Tuning range (FoM_T) are defined similarly to [12] as follows:

$$FoM = PN - 20log\frac{f_{center}}{\Delta f} + 10log\frac{PDC}{1\ mW} \tag{5.24}$$

$$FoM_T = PN - 20log\frac{f_{center}}{\Delta f}.\frac{TR\%}{10\%} + 10log\frac{PDC}{1\ mW} \tag{5.25}$$

where PDC is the power dissipation, PN is the phase-noise and Δf is the offset from the center frequency (f_{center}) of 77 GHz and 1.2 V supply is used.

Table 5.3 shows the comparison results with state-of-the-art mm-wave VCOs and DCOs. Except for 10 MHz in [26], the Δf for all the references is 1 MHz. The prototype has -185 FoM and -181 FoM_T. The proposed ML-DCO has the highest FoM and FoM_T of -185 and -184 respectively.

Operating in W-band frequency, the new tuning technique alleviates the varactors while effectively stretches the TR in uniform linear steps across a 7 GHz TR.

TABLE 5.1: Frequency Over Process Corners And Temperature Variations

Corner Temp.	C01 (GHz)	C06 (GHz)	C11 (GHz)	C16 (GHz)	C21 (GHz)	C26 (GHz)	C30 (GHz)
S.W. $75°C$	72.59	73.71	74.87	76.09	77.17	78.28	79.2
Typ. $25°C$	75.66	76.84	78.05	79.33	80.47	81.65	82.61
F.B. $-25°C$	79.19	80.44	81.76	83.16	84.37	85.64	86.65

TABLE 5.2: Phase Noise Over Process Corners

Corner Temp.	PN (dBc/Hz) of 76 GHz @ 1MHz offset	PN (dBc/Hz) of 77 GHz @ 1MHz offset	PN (dBc/Hz) of 82 GHz @ 1MHz offset
S.W. $75°C$	-97	-96	-95
Typ. $25°C$	-98.5	-98	-96.5
F.B. $-25°C$	-100	-99	-97

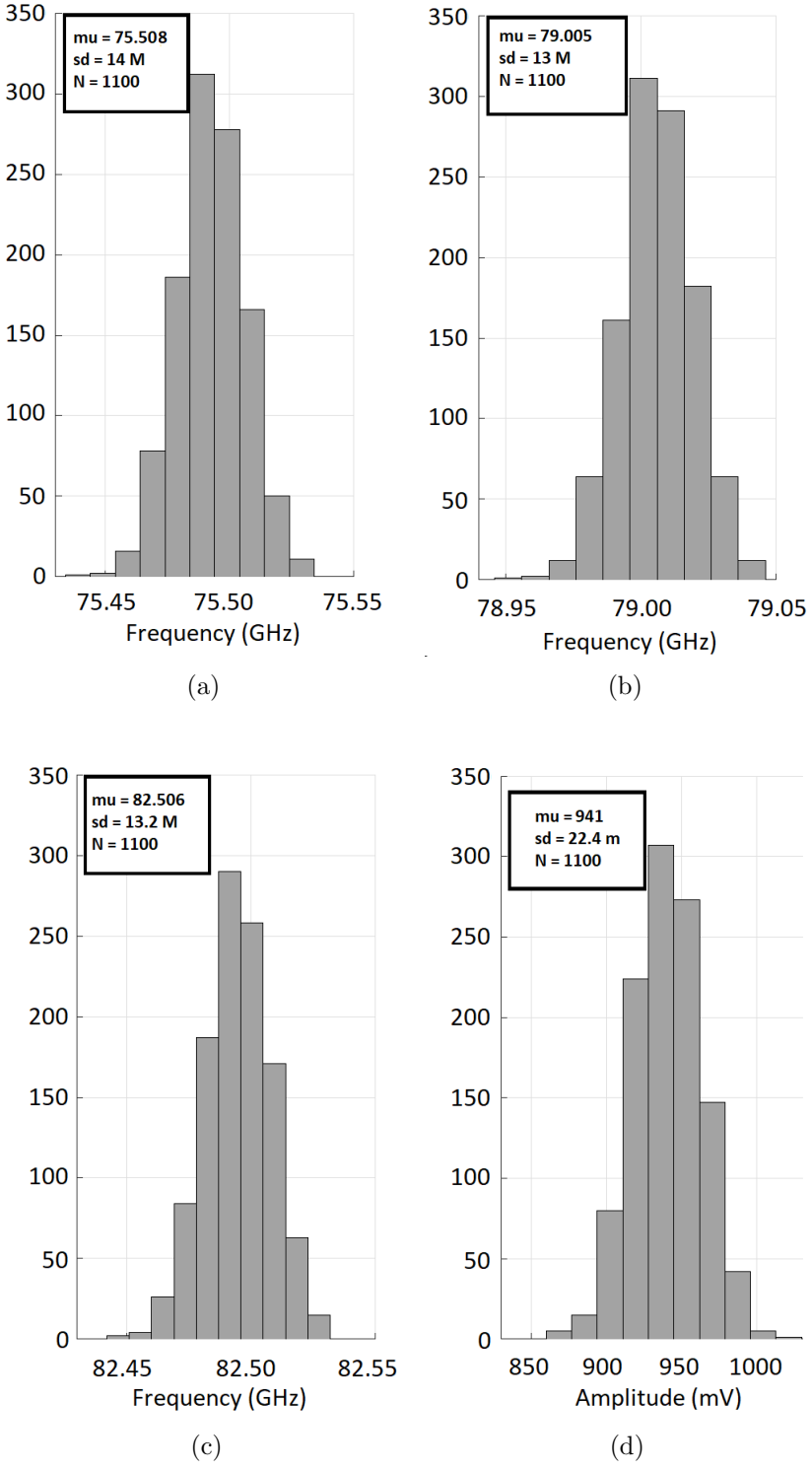
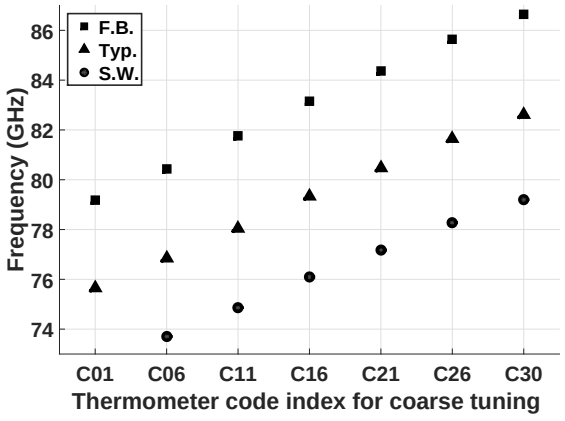
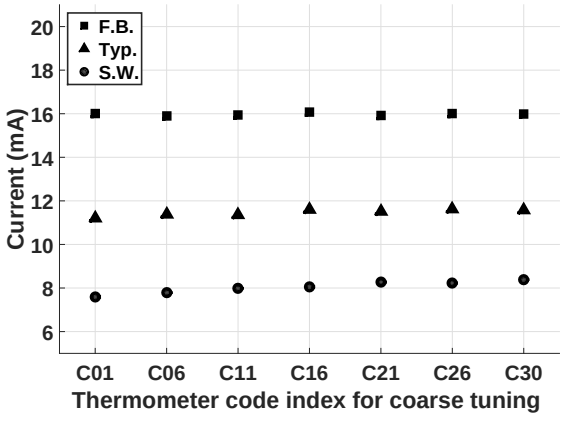


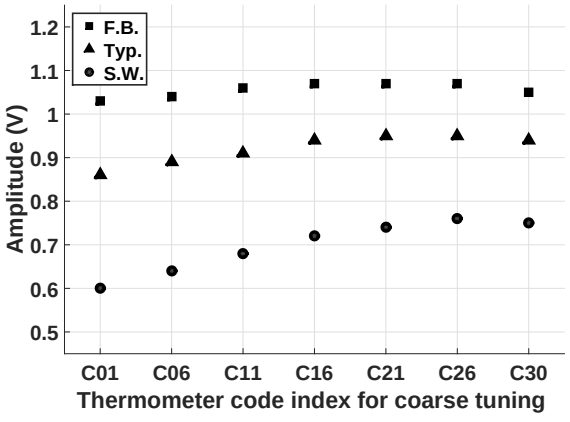
FIGURE 5.12: Monte Carlo simulation results. (a) minimum tuning frequency variation. (b) middle tuning frequency variation. (c) maximum tuning frequency variation. (d) Amplitude variation.



(a)



(b)



(c)

FIGURE 5.13: Corners simulation results at (Typ. $25°C$), (F.B. $-25°C$), and (S.W. $75°C$), repeated in (a)-(c) for seven coarse tuning codes (C01, C05, C11, C16, C21, C26, C30). (a) The frequency. (b) The current consumption. (c) The amplitude of oscillation.

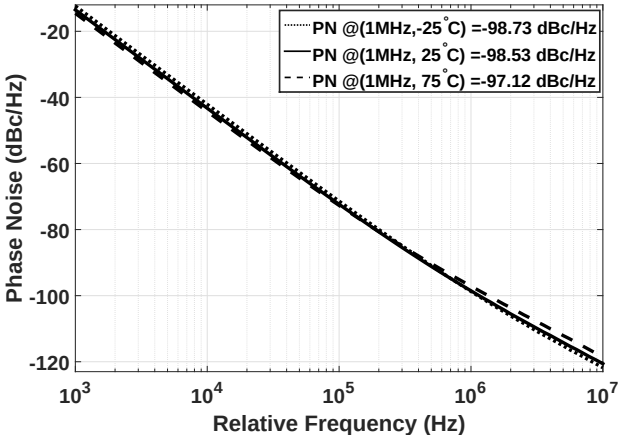


FIGURE 5.14: Phase-noise of the ML-DCO

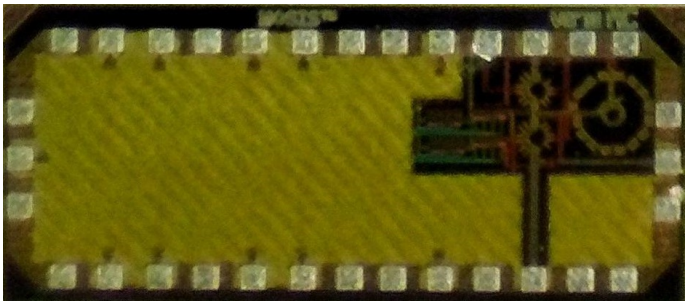


FIGURE 5.15: Chip photograph for the prototype.

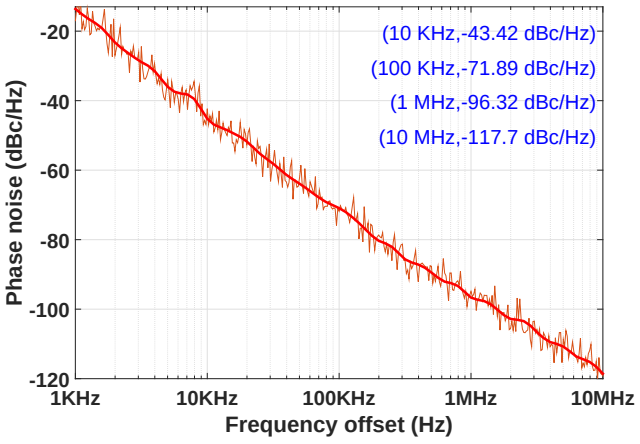


FIGURE 5.16: Measured phase-noise spectrum at 77 GHz for the ML-DCO prototype.

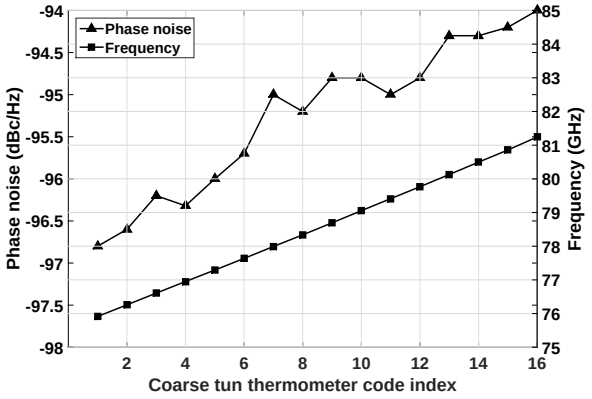


FIGURE 5.17: Measured results for oscillation frequencies and phase-noises at 1 MHz offset with respect to the frequency of the ML-DCO prototype across the tuning range.

TABLE 5.3: Performance Summary And Comparison

[Ref]Type	F_o (GHz)	TR (%)	PN ($\frac{dBc}{Hz}$)	PDC (mW)	FoM ($\frac{dBc}{Hz}$)	FoMT ($\frac{dBc}{Hz}$)	CMOS (nm)
[12]DCO	60	14	-90.7	18	-169	-176.6	130
[27]VCO	26	25	-104	9.96	-182	-190	130
[6]DCO	60	10	-93	12	-178	-178	90
[26]DCO	25	16	-117	23	-171	-175	40
[1]VCO	38.5	11	-87	11.7	-168	-169	65
Prototype	77	6.5	-96.3	7.2	-185	-181	65
ML-DCO	77	9	-98.5	14	-185	-184	65

5.9 Conclusions

Simultaneous wide tuning-range and small tuning steps are achieved for a 77 GHz DCO. MoM capacitors are employed for the coarse, intermediate as well as the fine-tuning banks. Thus low quality-factor MOS varactors are avoided. High linearity overlapped tuning banks are obtained to be perfect for FMCW ADPLL applications. A New coarse, intermediate, and fine-tuning techniques and configurations have been demonstrated in 77 GHz ML-DCO in 65 nm CMOS. Oscillating at 77 GHz, the ML-DCO achieves a total TR of 7 GHz while the average fine frequency resolution is 346 KHz, corresponding to a capacitance change of ΔC_L=1.6 aF. The phase-noise is better than -98.53 at 1 MHz offset. The tuning bits of the three banks can be readjusted to obtain a better fine resolution while

still maintaining the overlap of the three tuning banks and the TR. Moreover, since the three tuning banks are linear, a simple binary-to-thermometer decoder is sufficient for tuning word generation in an ADPLL. The distributed switchable MoM capacitors make a wide-band and high-resolution DCO feasible at W-band operation.

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Chapter 6

Conclusion

6.1 Summary of Conclusions

This dissertation is mainly focused on design and CMOS realization of mm-wave DCO that addresses the FMCW automotive radar requirements and to reduce the complexity of the calibration that is required to compensate the non-linearity in the DCO tuning characteristics.

- Chapter 2 presents a design of a CMOS $24GHz$ Clapp-Colpitts Digitally Controlled Oscillator (CC-DCO) with $22GHz - 29GHz$ tuning range for automotive Short Range Radar (SRR) aplication. The major challenge is to design a wide tuning range DCO. Proper oscillator topology is chosen, specific tuning mechanism is implemented. The CC-DCO is implemented in $65nm$ CMOS process. A wide tuning range of 29% and a fine tuning step of $1.6MHz$ are achieved simultaneously. The CC-DCO consumes $10mA$ from a $1V$ supply.

- Chapter 3 optimizes the CC-DCO topology by introducing a boosting mechanism, which is based on an in-depth mathematical analysis of the start-up condition and amplitude of oscillation. The improved performance is achieved through negative resistance boosting mechanism, which enhances the start-up time and

increases amplitude stabilization across the wide Tuning Range (TR). Moreover, it improves the Phase Noise (PN) performance while suppresses the amplitude-to-phase conversion. The proposed 24 GHz CMOS Enhanced Colpitts Clapp-DCO (ECC-DCO) is implemented in 65 nm TSMC CMOS process. It can effectively reduce the start-up time by 41%. Also, it boosts and stabilizes the amplitude across a TR of 29%. The amplitude varies by 1.5% across the $22 - 29$ GHz TR. The ECC-DCO consumes 12.8 mW.

- Chapter 4 presents a study and the analysis of process and temperature sensitivity in CMOS Colpitts-based oscillator. By defining the process and temperature sensitivity parameters early in the design process, unnecessary design iteration is prevented and time-to-market is reduced.

- Chapter 5 presents the analysis, design, and CMOS implementation of a $75.5 - 82.5$ GHz Monotonically Linear Digitally Controlled Oscillator (ML-DCO), which fulfills the requirements of the 77 GHz automotive radar. Non-linear large varactors are avoided. New tuning mechanism is developed by arranging the available minimum Metal-Oxide-Metal (MoM) capacitor in a unique configuration. Linear coarse, intermediate, and fine-tuning ranges are achieved to impact the generation of linear frequency modulation for millimeter-wave automotive radars and to reduce the complexity of the calibration that is required to compensate the non-linearity in the DCO tuning characteristics. The new arrangement results in a minimal amplitude variation while the ML-DCO is tuned. The coarse, intermediate, and fine-tuning steps are 0.22 GHz, 10 MHz, and 346 KHz respectively. The power consumption is 14 mW from a 1.2 V supply. The achieved phase-noise is -98.53 dBc/Hz at a $1MHz$ offset when oscillating at 77 GHz.

6.2 Suggested Future Work

This work opens the door for future CMOS implementation of ADPLL that can take advantage of the high linearity characteristics of the ML-DCO.

ADPLL is an attractive solution for radar sensors. Accurate FMCW chirp signal generator using two-point modulation ADPLL architecture is able to produce wide-band, precise, and linear frequency sweep in mm-wave. The dynamics of the frequency modulation mandates a DCO with high linear tuning characteristics. The ML-DCO can be perfectly adopted to provide this requirement.

Calibration complexity will be reduced significantly. The new tuning mechanism could also employed to the conventional LC-tank DCO, which is another widelly used topology and comparison between the performance could be confirmed. The future CMOS ADPLL can be used as an IP core for the 77 GHz automotive radar transceivers.

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