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A PLL based built-in self-test for MEMS sensors

Tareq Supon

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A PLL based built-in self-test for MEMS sensors

by

Tareq Muhammad Supon

A Thesis
Submitted to the Faculty of Graduate Studies
through Electrical and Computer Engineering
in Partial Fulfillment of the Requirements for
the Degree of Master of Applied Science at the
University of Windsor

Windsor, Ontario, Canada

2012

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A PLL based built-in self-test for MEMS sensors

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ABSTRACT

A new readout circuit for capacitive Micro-Electrical-Mechanical System (MEMS) devices has been proposed, developed and simulated in this thesis. The readout circuit utilizes a Phase Locked Loop (PLL) to convert variations of MEM capacitance to time domain signals. The proposed circuit demonstrates a robust performance against process, power supply and temperature variations due to inherent feedback of PLL systems. Post layout simulation results in Cadence environment using TSMC CMOS 65nm technology indicate that the implemented readout circuit can successfully measure and detect minor variations of MEMS capacitance from its nominal value.
DEDICATION

Dedicated to my respected parents whose prayers are always with me and my loving wife Mithua Zafrin who inspires and encourages me in every step of my life.
ACKNOWLEDGEMENTS

First of all I want to thank the Almighty Allah for passing me through the research work easily and allowing me to fulfil the requirements without difficulty.

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CHAPTER I
INTRODUCTION

The field of micro-electro-mechanics achieved a milestone when W.S. Trimmer and K.J. Gabriel came up with an idea [1] to design electrostatic motors utilizing silicon wafers. That actually built the concept of a Micro Electro Mechanical System (MEMS). The MEMS technology has come a long way since then. It has been proven to be more efficient in various aspects such as performance, size, cost, speed and so on. The introduction of CMOS-MEMS devices [2] has revolutionized the field of Microsystems. MEMS technology has enabled the integration of sensors, actuators and signal processing circuits on a single chip [3]. MEMS technology has added a new dimension to the available integrated circuit technology. Manufacturing equipment, processes, modeling and simulation tools, and materials have been developed for MEMS fabrication and packaging [4].

1.1 MEMS Devices:

In the past 25 years MEMS has flourished from a research interest to a multibillion dollar commercial enterprise. Most of the prototype devices created as part of research and development efforts did not become commercially successful products [5]. Currently, the vast majority of MEMS are either sensors or actuators. Sensors and actuators are commonly the interface between electronic circuits and the external environment. There are mainly four families in the kingdom of MEMS actuators: electrostatic, piezoelectric, thermal and magnetic. MEMS displacement sensors can be considered as capacitive, optical and electron tunneling [5] structures. Among them, the
Capacitive MEMS structures have relatively simple architectures with some added advantages.

1.2 Capacitive MEMS Structure

Capacitive MEMS sensors are commonly used to covert a mechanical quantity such as acoustic pressure or velocity acceleration into capacitance variation. The capacitance variations from its nominal value is conditioned, converted into digital format and processed in a controller for desired use. Capacitive MEMS structures have some notable advantages such as:

- They support better frequency performance compared to other counterparts, since the natural frequency of the Capacitive MEMS depends on its mass and material property.
- Due to their very small size, the use of energy and materials in manufacturing is minimized.

Figure 1: Combdrive resonator (Courtesy Discera)
• They have a very good reproducibility as they can be fabricated in batches.

• Capacitive MEMS can be fabricated within a chip. As a result, the signal delay between the mechanical and the electrical interfaces reduces.

• Capacitive MEMS devices can attain a very high resolution and operating range.

• The fabrication cost is very low due to the tiny size and as the well-developed batch fabrication technology.

1.3 Capacitive MEMS Readout Circuit

Capacitive MEMS devices are capable of operating at a very high frequency with a very high precision and accuracy. These qualities have made capacitive MEMS a very desirable component in sectors like biomedical, avionics and auto industry, etc. For most of these applications, a high precision and accurate detection is needed as the slightest error can prove to be very costly.

A readout circuit is an essential part of a capacitive MEMS sensor. Even though a capacitive MEMS sensor converts various mechanical parameters to electrical signals, the desired precision cannot be achieved without a precise readout circuit. A readout circuit must be able to detect very small and abrupt change of the electrical signal and respond almost instantaneously. In the operation of MEMS sensors, the design of readout circuit plays a critical role. While judging the performance of a MEMS sensor module, the performance of the readout circuit is of the same importance as the sensitivity and efficiency of the MEMS structure, if not more. To design a readout circuit, different types of nonlinearity effects, noise and interference have to be carefully handled to achieve the
desired accuracy and measurement resolution. The strict design requirements for readout circuits make the design of a robust circuit quite challenging.

Many design techniques have been proposed by various researchers in the literature for readout circuits. The most commonly used techniques are: charge sensitive amplifier (CSA) [6], correlated double sampling (CDS) [7], and chopper stabilization (CHS) [8]. These techniques can be incorporated in readout circuits in order to reduce the parasitic capacitance effect and offset as well as flicker noise which is dominant at low frequencies.

A charge sensitive amplifier (CSA) is a current integrator driven by an electrical source with capacitive nature. It transfers the input charge to another reference capacitor and produces an output voltage equal to the voltage across the reference capacitor. Thus the output voltage is proportional to the charge of both the reference capacitor. The input impedance of the circuit is almost zero because of the Miller effect. Hence all the stray capacitances are virtually grounded and they have no influence on the output signal.

In Correlated Double Sampling (CDS) electrical values such as voltages or currents are measured in such a way that allows removing an undesired offset. The main use of CDS is measuring sensor outputs. The output of the sensor is measured twice: once in a known condition and once in an unknown condition. The value measured from the known condition is then subtracted from the unknown condition to generate a value with a known relation to the physical quantity being measured. This is commonly used in switched capacitor operational amplifiers.

Chopper stabilization is better described as Offset Stabilization in OPAMPs by using a chopper circuit. It minimizes the input offset voltage and possibly any low-
frequency noise voltage in an OPAMP. The technique expressly chops or modulates the input signal using a square wave and eliminates or minimizes the offset voltage appearing at the output.

Various researchers used these techniques and integrated those in different types of readout circuits. Readout circuits can be divided into three basic groups, which are ac-bridge with voltage amplifier [8] – [11], trans-impedance amplifier [12], and switched-capacitor circuit [7], [13] – [15]. By combining both CDS amplitude modulation and demodulation in the switched-capacitor circuit, high sensitivity of 7.88 mV/aF has been reported [16]. Among these circuits, the switched-capacitor circuit is widely used [20].

Each of these readout circuits has its own merits and demerits. The overall performance of these circuits has been evaluated for different parasitic capacitances, amplifier gain bandwidths, and sampling frequencies using the above equations. It can be summarized that, the ac-bridge circuit works more efficiently when the parasitic capacitance is very low as it can detect minor capacitance variations, whereas when the parasitic capacitance is high, switched capacitor and transimpedance amplifier circuits are used to achieve high resolution readings. Readout circuits in general have to provide a very fine measurement resolution. Process, supply Voltage and Temperature (PVT) variations can affect the performance of readout circuits considerably.

1.4 Proposed Method

In this thesis, a new technique has been proposed to measure MEMS capacitance using a Phase Locked Loop (PLL). The readout circuit has been designed using a charge pump PLL. It can detect minor variations of MEMS capacitance from its nominal value. The proposed method has some advantages over the current solutions, such as (a) low
sensitivity to PVT variations due to the internal feedback of PLL systems (b) high measurement resolution and accuracy even in the presence of supply, process and temperature variations.

The rest of the thesis is organized as follows: chapter II presents some background study and literature review. The block diagram of the proposed readout circuit along with the principle of the proposed method with mathematical validation is discussed in chapter III. This chapter also elaborates the detailed functions of the building blocks. Chapter IV describes the test circuitry along with the schematic and post layout simulation results. The thesis is finally concluded in Chapter V with some discussion and future works.
CHAPTER II
REVIEW OF LITERATURE

The development of three-dimensional integrated circuits has enhanced the possibility of successful CMOS and MEMS integration. CMOS-MEMS integration [2] improves the performance of Microsystems substantially while reducing the fabrication cost. However, due to the multi dimensional nature [17] of such systems and the increasing popularity of MEMS for sensitive operations, more robust and precise readout solutions are needed to address the upcoming challenges. As the name suggests, Capacitive MEMS sensors operate based on the principal of capacitance variations. The parameters of interest such as acceleration, ultrasonic waves and pressure trigger a variation in the capacitance of the MEMS structure, which converts those parameters into electrical signals. The signals generated by MEMS structure are then measured by a readout circuit. The accuracy and resolution of readout circuits play an important role on the overall performance of MEMS sensors.

2.1 Readout Circuit for Capacitive MEMS

A readout circuit simply reads the value of the capacitance variations of a MEMS device. The performance of a MEMS sensor module depends both upon the sensitivity and efficiency of the MEMS structure as well as the performance of the readout circuit. As the capacitance of a MEMS device is in the Atto-farad \((10^{-18})\) range, a very precise readout circuit is a must to keep the error margin very low. MEMS devices have a great potential in almost every aspect of our world because of their added advantages. As a result, the importance of a precise readout circuit has increased day by day. Furthermore, MEMS devices are now fabricated on the same chip (SoC) with digital, analog, memory,
and FPGA circuit technologies [23]. Hence, an accurate and high precision readout circuit is needed for MEMS sensors to ensure measurement validity of the mechanical quantities. To design a readout circuit, nonlinearity effects, noise and interference have to be carefully handled to achieve the desired accuracy and measurement resolution.

Readout circuits have been studied comprehensively for a long time. Readout integrated circuits (ROIC) using capacitance-to-voltage (C-V) conversion method are widely employed. These circuits possess a high Signal-to-Noise Ratio (SNR), and high sensitivity [17] – [19]. The concept of this method is based on the conventional Analog-to-Digital Conversion (ADC). As the supply voltage scales down, the conventional ADC method presents some drawbacks such as high power consumption and circuit complexity [18] – [20]. New approaches have been presented based on the conventional Time-to-Digital Conversion (TDC) to overcome these negative effects and also to increase the resolution.

2.1.1 AC-bridge with voltage amplifier

![Simplified block diagram of ac-bridge with voltage amplifier](image)

**Figure 2: Simplified block diagram of ac-bridge with voltage amplifier [25]**

The sensing circuit of an ac-bridge with voltage amplifier readout circuit [8] – [11], [20] has a half bridge which contains a sensing capacitor \(C_s\) and a reference capacitor \(C_r\). The block diagram of the circuit is shown in Figure 2. The circuit is
driven by two pulses with 180° phase difference. The output of the bridge is proportional to the capacitive change ($\Delta C$), which is amplified by a voltage-mode amplifier. The final output is given by [20]:

$$V_{out} = V_p \frac{\Delta C}{2C_{S,0} + C_p} \times A_v$$

(2.1.1)

where $A_v$ is the amplifier gain, $C_p$ is the parasitic capacitance, $\Delta C = C_s - C_r$, $C_s$ is the sensing capacitor, $V_p$ is the amplitude of the pulse and $C_{S,0}$ is the MEMS capacitor at rest. The frequency of the input pulse is chosen to be higher than 1/f corner frequency of the amplifier in order to reduce the flicker noise. Moreover, increasing the amplitude of the pulse and reducing the parasitic effects improve the output voltage. The minimum detectable capacitance in this approach is given by [20]:

$$\Delta C_{\text{min}} = \frac{2C_{S,0} + C_p}{V_p} \times V_{n,rms} \times \sqrt{BW}$$

(2.1.2)

where $BW$ is the amplifier’s bandwidth and $V_{n,rms}$ is the input-referred thermal noise of the amplifier. From the equation it is evident that, the minimum detectable capacitance is determined by the thermal noise floor of the circuit and is still a function of parasitic capacitance.

2.1.2 Transimpedance amplifier

In the transimpedance amplifier readout circuit [12], [20], the half bridge is driven by two ac signals with 180° phase difference. The output of the bridge is virtually grounded by an op-amp with a resistive feedback $R_f$. The block diagram is shown in Figure 3.
When the input frequency \( f_{\text{drive}} \) is smaller than the overall readout circuit bandwidth, the output of the overall readout circuit is given by

\[
|V_{\text{out}}| = 2\pi f_{\text{drive}} V_m R_f \Delta C \quad (2.1.3)
\]

where, \( f_{\text{drive}} \) is the drive voltage frequency, \( \Delta C = C_s - C_r \) and \( V_m \) is the drive signal amplitude. However, the amplifier dominant pole creates an inductive effect and the bandwidth is limited by the poles associated with \( R_f \). The maximum output, which is attained at the resonance frequency, can be determined from [20]:

\[
f_{\text{drive-opt}} = \frac{\sqrt{GBW_{\text{amp}}}}{2\pi R_f (2C_s + C_p)} \quad (2.1.4)
\]

where \( GBW_{\text{amp}} \) is the amplifier gain bandwidth. In this case the thermal noise of the feedback resistor dominates other sources of noise in the circuit. The minimum detectable capacitance in this method is given by [20]:

\[
\Delta C_{\text{min-rms}} = \frac{\sqrt{BW}}{V_m} \sqrt{\frac{2k_B T (2C_s + C_p)}{\pi GBW_{\text{amp}}}} \quad (2.1.5)
\]

where \( k_B = 1.38066 \times 10^{-23} \text{ J/} \text{K} \) is the Boltzmann constant and \( GBW_{\text{amp}} \) is the amplifier gain bandwidth product.

Figure 3: Simplified block diagram of transimpedance amplifier [25]
2.1.3 Switched capacitor circuit

In the switched capacitor technique [7], [13] – [15], [20], an input capacitive feedback \( (C_{\text{int}}) \) has been introduced. In this method, the sense and reference capacitors are driven by signals with 180° phase shift and the capacitive difference is integrated into the feedback capacitor \( (C_{\text{int}}) \). The block diagram is shown in Figure 4. The output of the readout circuit is given by [20]:

\[
V_{\text{out}} = V_p \frac{\Delta C}{C_{\text{int}}}
\]  \hspace{1cm} (2.1.6)

![Figure 4: Simplified block diagram of switched capacitor circuit [25]](image)

The amplifier flicker noise can be cancelled by CDS technique [7]. The minimum detectable capacitance can be obtained from [20]:

\[
(\Delta C_{\text{min-rms}})^2 = \frac{1}{f} \left( \frac{16k_B T (2C_s + C_p) C_{\text{int}}}{C_{\text{out}}} + 2k_B T C_{\text{int}} \right) (BW) \]  \hspace{1cm} (2.1.7)

where \( C_{\text{out}} \) is the total amplifier output capacitance and \( f_s \) is the sampling frequency. If the sampled switch noise \( KT/C_{\text{int}} \) can be cancelled by sampling and removed from the output then the minimum detectable capacitance is given by
\[
\Delta C_{\text{min-rms}} = \sqrt{\frac{1}{f} \left( \frac{16k_B T (2C_s + C_p) C_{\text{int}}}{C_{\text{out}}} \right)} (\sqrt{BW})
\] 

(2.1.8)

2.2 Drawbacks of the current readout circuits

All of the above three methods have some common grounds, such as:

- All of them have two symmetrical inputs with 180° phase shift.
- These methods support high precision in an ideal condition, i.e. no PVT variation.
- Parasitic capacitance plays a big role in determining the MEMS capacitance.

The methods described in the previous sections are too sensitive to the variations of the phase shift and PVT variations. Moreover, the major dependency on the parasitic capacitance lowers the attainable resolution as the parasitic capacitance changes depending on the operating condition.
CHAPTER III
CAPACITIVE MEMS READOUT METHODOLOGY USING PHASE LOCKED LOOP (PLL) TECHNOLOGY

The block diagram and the working principle of the proposed method are discussed in this section. A Charge Pump Phase Locked Loop (CPPLL) is used to design the readout circuit. As the name suggests, a PLL locks both the output and input phase and frequency together. In other words, the output reflects the phase and frequency of the input signal. If a capacitive MEMS device is introduced in the feedback path of the PLL, it adds a certain amount of delay between the output and the input signal. The amount of delay is directly proportional to the change in capacitance.

3.1 Block Diagram of the Proposed PLL Technique

The block diagram of a typical CPPLL is shown in Figure 5. It incorporates a Phase-Frequency Detector (PFD) block, a Charge Pump (CP) – Low Pass Filter (LPF) block and a Voltage Controlled Oscillator (VCO) block.

![Figure 5: Block diagram of a typical charge pump phase locked loop](image)

Ideally, when lock is achieved, the phase and frequency difference between the input and output signals becomes zero. In the locked condition, process variations, temperature drifts and to some degree supply variations have little or no effect on the phase and frequency of the output signal. In fact, the PLL feedback loop negates the PVT
effects to achieve the lock. This fundamental characteristic of PLL systems has been exploited to design a robust readout circuit for MEMS sensors.

The block diagram of the proposed readout circuit is shown in Figure 6. It consists of the generic blocks of a charge pump PLL together with a MEMS detection block containing the MEMS sensor. When operating in the test mode, $V_1$ is connected to a variable supply voltage to apply different voltage levels to the MEMS sensor; whereas in the readout mode $V_1$ is connected to the PLL supply voltage.

![Block diagram of the PLL based MEMS readout circuit](image)

**Figure 6: Block diagram of the PLL based MEMS readout circuit**

3.2 Measurement Method

The introduction of the detection block between the VCO and PFD circuits creates a phase difference between the VCO output and the input signal. The resultant output and input wave-shapes are shown in Figure 7. When the MEMS capacitance varies from its nominal value, the signals applied to the PFD inputs become out of phase.
As a result, the PLL loses its lock. The PLL then adjusts the VCO output to reacquire the lock. When the lock is achieved again, the phase difference between the input $V_{in}$ and the feedback signal $V_f$ ideally reduces to zero and they become in-phase again. However, this results in a phase difference between the VCO output and the input signal. The variation in the phase difference is in accordance to the variation of the MEMS capacitance, which is also shown in Figure 10. In the next section a relation between the phase difference between the VCO output and the input signal in the locked condition and the variations of the MEMS capacitance has been established; which shows that they are directly proportional to one other.

### 3.3 Mathematical Analysis

In the architecture shown in Figure 6, when the PLL settles down $V_f$ and $V_{in}$ run at the same frequency without any phase difference. Therefore, the time difference between them ideally becomes zero. The time difference between the rising edges of $V_{in}$ and $V_{vco}$ varies with the time constant of the detection block. If $T_o$ is the time required for the

Figure 7: Input, output and feedback signals of the readout circuit (a) Before lock is achieved and (b) After acquiring the lock
MEMS capacitance to charge up and exceed the threshold voltage \(V_{th}\) of the PFD, which indicates the time difference between \(V_{in}\) and \(V_{vco}\), then we can write that:

\[
V_{DD} (1 - e^{-T_o/T_o}) = V_{th}
\]  
(3.3.1)

Rearranging, we get:

\[
T_o = \tau_o \ln \left( \frac{V_{DD}}{V_{DD} - V_{th}} \right)
\]  
(3.3.2)

where \(\tau_o = R(C_o + C_p)\) is the time constant and \(V_{DD}\) is the supply voltage. \(C_o\) is the MEMS capacitance in the steady state and \(C_p\) is the parasitic capacitance.

Similarly, under excited condition, when the MEMS capacitance changes from its nominal value \(C_o\) to \(C_1\), the charge up time \(T_1\) can be determined from:

\[
T_1 = \tau_1 \ln \left( \frac{V_{DD}}{V_{DD} - V_{th}} \right)
\]  
(3.3.3)

where \(\tau_1 = R(C_1 + C_p)\). From equation (3.3.2) and (3.3.3), the variation of the MEMS capacitance \(C_1 - C_o = \Delta C\) can be found as:

\[
\frac{T_1 - T_o}{T_o} = \frac{\tau_1 - \tau_o}{\tau_o}
\]  
(3.3.4)

Now, putting the values of \(T_1 - T_o = \Delta T\), \(\tau_o\) and \(\tau_1\), we can write:

\[
\frac{\Delta T}{T_o} = \frac{\Delta C}{C_o + C_p}
\]  
(3.3.5)

From this equation it is evident that the variation of the capacitance is independent of the supply voltage \(V_{DD}\) and threshold voltage \(V_{th}\) which varies considerably with temperature and process variations.
3.4 PLL Stability Issue

The PLL of the readout circuit has to be able to lock on the applied input signal in order operate properly. The linear model of a conventional charge pump PLL indicates that the relationship between the input and output can be characterized by a second order system [21].

\[
\begin{align*}
V_{in} & \rightarrow + \rightarrow K_p \left( \frac{1}{C_p s} + R_p \right) \rightarrow \frac{K_{vco}}{s} \rightarrow \frac{A_v}{1 + R_1 C_{MEMS} s} \rightarrow V_{vco}
\end{align*}
\]

Figure 8: Linear model of the proposed PLL based MEMS readout circuit

The linear model of the proposed design is shown in Figure 8. The addition of the detection block to the PLL system undermines the stability of the PLL loop. An extra pole is introduced to the system as a result of the inclusion of the detection block. This makes the system a third order one creating stability difficulties. To ensure the stability of the PLL loop, in the proposed scheme the time constant of \( R_1 C_{MEMS} \) is chosen to be much lower than the period of the PLL natural frequency. As a result, the frequency of the additional pole falls far above the natural frequency of the system. Thus the behavior of the scheme can still be approximated by a second order system.
CHAPTER IV
ANALYSIS OF RESULTS

The proposed design was implemented in TSMC CMOS 65nm technology using Cadence design tools. The MEMS combdrive [22] shown in Figure 9 was used as a Device Under Test (DUT).

4.1 Design of the PLL

As discussed above, a PLL consists of three main blocks: PFD, CP/LPF and VCO. The circuit diagram of each block is shown separately in Figure 10, 11 and 12. The whole system with the MEMS capacitor is shown in Figure 6. Here, a capacitor from the TSMC CMOS 65nm library, “moscap_rf”, is used as the MEMS capacitor.
Figure 10: Circuit Diagram of Phase Frequency Detector

Figure 11: Circuit Diagram of Charge Pump and Low Pass Filter
If the input frequency is higher than the VCO natural frequency, then the “Up” pin of the PFD gives a pulse. That pulse triggers the pMOS device of the CP/LPF block. As a result, the capacitors $C_1$ and $C_2$ charge up and cause a voltage build-up at the “OUT” pin. This output acts as the control voltage for the VCO and pushes the VCO output to a higher frequency. This process goes on until both the input and the feedback signals are in same phase and frequency. At that point, the control voltage stabilizes at a certain constant value. The MEMS capacitor introduces a phase difference between $V_{VCO}$ and $V_f$, signals and consequently between $V_{VCO}$ and $V_{IN}$ as it works as a delay element. The phase difference varies linearly with the change in MEMS capacitance.
4.2 Implementation and Simulation Results

An input signal of 40MHz has been used to conduct the tests. The implementation is done for both schematic level and post-layout level. Then both the levels are simulated and the results are compared to each other to find and eliminate any undesired effect.

4.2.1 Schematic Level

First, each block was created separately and tasted for their basic operation. A brief description of the implementation of each block is given below:

4.2.1.1 Schematic of Phase-Frequency Detector (PFD)

As shown in the basic circuit diagram in Figure 10, a PFD block has to contain two D-flip-flops (DFF) and one NAND gate. During the implementation, it has been determined that the Up and Down pulses are not given enough time to turn on the following charge pump circuit. To solve this problem, three buffers were added between
the NAND gate and the D-flip-flops. The schematic diagram implemented in cadence environment is shown in Figure 14.

The output of the PFD is shown in Figure 15. It shows a satisfactory result with a delay between the input and the output signals, which is due the D-flip-flop delay.

4.2.1.2 Schematic of Charge Pump and Low Pass Filter (CP/LPF)

Figure 15: Input and Output Waveforms of the PFD in Schematic Level

The output of the PFD is shown in Figure 15. It shows a satisfactory result with a delay between the input and the output signals, which is due the D-flip-flop delay.

4.2.1.2 Schematic of Charge Pump and Low Pass Filter (CP/LPF)

Figure 16: Schematic Diagram of the Charge Pump and Low Pass Filter
The block is designed exactly the same as is described in Figure 11. Capacitor $C_2$ is taken 5-10 times lower than $C_1$ to avoid any instability caused due to the introduction of the second pole associated with $C_2$. The schematic diagram is shown in Figure 16.

![Figure 16: Schematic Diagram of the Block](image)

**Figure 16: Schematic Diagram of the Block**

The output of the CP/LPF is shown in Figure 17. The result is acceptable with a slight spike at the start of each output pulse.

4.2.1.3 Schematic of Voltage Controlled Oscillator (VCO)

A ring oscillator is used as the oscillating circuit of the VCO. The capture range is chosen around 30MHz – 85MHz. The schematic diagram implemented in cadence environment is shown in Figure 18.

![Figure 17: Input and Output Waveforms of the CP/LPF in Schematic Level](image)

**Figure 17: Input and Output Waveforms of the CP/LPF in Schematic Level**

The output of the CP/LPF is shown in Figure 17. The result is acceptable with a slight spike at the start of each output pulse.
Figure 18: Schematic Diagram of the Voltage Controlled Oscillator
The output of the VCO is shown in Figure 19. It shows a linear frequency variation within 34MHz – 76MHz range as shown in Figure 20.

Figure 19: Input and Output Waveforms of the VCO in Schematic Level

Figure 20: Frequency Variation of the VCO with the Variation in Input Voltage
4.2.1.4 Schematic of MEMS Detection Block

As shown in Figure 6, a MEMS detection block consists of a unity gain amplifier and a MEMS sensor. So, an amplifier is designed to give unity gain. A CMOS capacitor, \textit{moscap}_{rf}, is used as the MEMS sensor. Here, \( R_1 \) is chosen in such a way that the time constant of \( R_1C_{\text{MEMS}} \) is much lower than the period of the PLL natural frequency. This ensures the PLL stability when all blocks are connected together.

4.2.1.5 Schematic of the Proposed Circuit

At first, the main three blocks of the PLL are connected together to ensure the operation of the PLL. Some parameters are due to be changed slightly to get the desired
output. The capture range of the PLL changed slightly from the original VCO capture range to 30.7MHz – 87.52MHz. The schematic diagram is shown in Figure 22. The charge pump is changed in such a way that at 40MHz input frequency, the control voltage, i.e. the output of the charge pump, remains at around 500 mV. This ensures maximum swing without any chopping. The output of the PLL is shown in Figure 23.

![Figure 23: Input, Output and Control Voltage Waveforms of the PLL in Schematic Level](image)

Then, the MEMS detection block is connected to the PLL. The circuit shows a linear frequency variation from 36MHz – 67MHz. The schematic diagram of the final circuit is shown in Figure 24.
The output shows promising result with a linear variation of the delay between the input and output signals with the variation of MEMS capacitance. The input and output waveforms are shown in Figure 25 in locked condition (constant control voltage) for a MEMS capacitance of 65fF, which is the nominal value.

Figure 24: Schematic Diagram of the Proposed Circuit

Figure 25: Schematic Level Waveforms of Simulated control voltage of the implemented readout circuit, Input and VCO output signals
In Figure 25 the output of the CP/LPF, i.e. the control voltage for the VCO, the PLL input and output waveforms are shown over the entire range of simulation. As seen in the Figure 25, the output $V_{vco}$ is in $180^\circ$ phase shift compared to $V_{in}$ and $V_f$. This is because of the use of a unity gain amplifier (Figure 6) to isolate $V_{vco}$ and $V_f$ nodes from one another. The introduction of that unity gain amplifier also gives the parasitic capacitance that was shown in the mathematical analysis. Apart from that $180^\circ$ phase shift, $V_{vco}$ also has some other delay as seen from the figure. That delay accounts for the total capacitance $C_1$, which is the combined value of the MEMS capacitance and the parasitic capacitance. In this case, $V_{in}$ and $V_f$ are in-phase and the time difference between $V_{vco}$ and $V_{in}$ is linearly proportional to the change in MEMS capacitance.

MEMS capacitors have to be effectively constant. If the capacitance varies too much from the nominal value, the MEMS device can be said to be damaged. So, the measurement of a variation of $\pm25\%$ is enough to determine the linearity of the readout circuit. The measured time delays with a $\pm25\%$ variation of the MEMS capacitance are shown in Table 1. The nominal value of the capacitance is $65\text{fF}$. The “% Error” in the rightmost cell of the table indicates a variation of less than $0.1\%$, which is very promising.
Table 1: Simulated results of the schematic level when DUT capacitance varies by ±25% from its nominal value of 65fF

<table>
<thead>
<tr>
<th>Reference MEMS Cap. (fF)</th>
<th>Delay (nS)</th>
<th>MEMS Cap. (fF) Determined via Simulation</th>
<th>% Error</th>
</tr>
</thead>
<tbody>
<tr>
<td>48.75</td>
<td>2.0386</td>
<td>48.7980</td>
<td>0.0985</td>
</tr>
<tr>
<td>52.00</td>
<td>2.1743</td>
<td>52.0465</td>
<td>0.0895</td>
</tr>
<tr>
<td>55.25</td>
<td>2.3100</td>
<td>55.2950</td>
<td>0.0815</td>
</tr>
<tr>
<td>58.50</td>
<td>2.4458</td>
<td>58.5454</td>
<td>0.0776</td>
</tr>
<tr>
<td>61.75</td>
<td>2.5815</td>
<td>61.7924</td>
<td>0.0687</td>
</tr>
<tr>
<td>65.00</td>
<td>2.7155</td>
<td>65.0000</td>
<td>0.0000</td>
</tr>
<tr>
<td>68.25</td>
<td>2.8494</td>
<td>68.2052</td>
<td>0.0657</td>
</tr>
<tr>
<td>71.50</td>
<td>2.9849</td>
<td>71.4505</td>
<td>0.0692</td>
</tr>
<tr>
<td>74.75</td>
<td>3.1206</td>
<td>74.6976</td>
<td>0.0701</td>
</tr>
<tr>
<td>78.00</td>
<td>3.2559</td>
<td>77.9374</td>
<td>0.0802</td>
</tr>
<tr>
<td>81.25</td>
<td>3.3910</td>
<td>81.1713</td>
<td>0.0968</td>
</tr>
</tbody>
</table>

To justify the linearity, a graph is plotted with the obtained values, which is shown in Figure 26. As seen from the figure, the relation between the Time delay and the measured capacitance is effectively linear.

![Figure 26: Relation between MEMS capacitance and time delay](image_url)
Any variation in the supply voltage can change the characteristics of a circuit. So, the circuit related to the supply voltage is designed in such a way that the supply voltage remains effectively constant regardless the operating condition and loading effect. So, the supply voltage is varied by ±5% to observe the effect in the measured capacitance.

Table 2: Simulated results of the schematic level when supply voltage varies by ±5%

<table>
<thead>
<tr>
<th>VDD (V)</th>
<th>MEMS Cap. (61 fF)</th>
<th>Simulated Cap. (fF)</th>
<th>% Error</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>Delay (nS)</td>
<td></td>
<td></td>
</tr>
<tr>
<td>0.95</td>
<td>1.1829</td>
<td>61.0652</td>
<td>0.1068</td>
</tr>
<tr>
<td>1.00</td>
<td>1.2064</td>
<td>61.0663</td>
<td>0.1088</td>
</tr>
<tr>
<td>1.05</td>
<td>1.2289</td>
<td>61.0672</td>
<td>0.1102</td>
</tr>
</tbody>
</table>

The obtained result is shown in Table 2. The %Error column shows that the variation between the reference and the simulated capacitance values is around 0.1%, which indicates the robustness of the proposed scheme against supply voltage variation.

Table 3: Simulated results of the schematic level as the temperature varies from -50°C to 60°C

<table>
<thead>
<tr>
<th>Temperature (°C)</th>
<th>MEMS Cap (61 fF)</th>
<th>Simulated Cap. (fF)</th>
<th>% Error</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>Delay (nS)</td>
<td></td>
<td></td>
</tr>
<tr>
<td>-50</td>
<td>2.1960</td>
<td>61.0116</td>
<td>0.019</td>
</tr>
<tr>
<td>-40</td>
<td>2.2600</td>
<td>61.0134</td>
<td>0.022</td>
</tr>
<tr>
<td>-30</td>
<td>2.3240</td>
<td>61.0159</td>
<td>0.026</td>
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<tr>
<td>-20</td>
<td>2.3881</td>
<td>61.0189</td>
<td>0.031</td>
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<tr>
<td>-10</td>
<td>2.4521</td>
<td>61.0220</td>
<td>0.036</td>
</tr>
<tr>
<td>0</td>
<td>2.5162</td>
<td>61.0256</td>
<td>0.042</td>
</tr>
<tr>
<td>10</td>
<td>2.5803</td>
<td>61.0299</td>
<td>0.049</td>
</tr>
<tr>
<td>20</td>
<td>2.6445</td>
<td>61.0342</td>
<td>0.056</td>
</tr>
<tr>
<td>30</td>
<td>2.7086</td>
<td>61.0384</td>
<td>0.063</td>
</tr>
<tr>
<td>40</td>
<td>2.7728</td>
<td>61.0433</td>
<td>0.071</td>
</tr>
<tr>
<td>50</td>
<td>2.8370</td>
<td>61.0482</td>
<td>0.079</td>
</tr>
<tr>
<td>60</td>
<td>2.9012</td>
<td>61.0537</td>
<td>0.088</td>
</tr>
</tbody>
</table>

To further study the efficacy of the method, the effects of temperature on the performance of the readout circuit are also investigated through simulation. Generally,
the operating temperature varies roughly from -50°C to 60°C. So, the simulation has been done within this range. The measured capacitances as indicated in Table 3 match the reference values with a maximum error of 0.088%.

### 4.2.2 Post-Layout Level

After proving the concept in schematic level, the layout of each block is generated. All the components are placed as close to each other as possible. This reduces the routing delay. The layout level design is explained further in the Appendix. The routing of each block is done using auto-routing option provided in the TSMC CMOS 65nm design tool. The layout diagram of each block is given below with the waveforms.
4.2.2.1 Layout of Phase-Frequency Detector

The layout diagram and the waveforms of the PFD block are shown below in Figure 27 and 28 respectively:

![Figure 27: Layout Diagram of the Phase Frequency Detector (PFD)](image)

![Figure 28: Input and Output Waveforms of the PFD in Post-Layout Level](image)
4.2.2.2 Layout of Charge Pump-Low Pass Filter (CP/LPF)

The layout of the CP/LPF block is given below in Figure 29:

![Figure 29: Layout Diagram of Charge Pump and Low Pass Filter](image)

The output waveforms of this block are shown in Figure 30:

![Figure 30: Input and Output Waveforms of the CP/LPF in Post-Layout Level](image)
4.2.2.3 Layout of Voltage Controlled Oscillator (VCO)

The layout of the VCO block is given below in Figure 31:

Figure 31: Layout Diagram of the Voltage Controlled Oscillator
The output waveforms of the layout of VCO are shown in Figure 32:

**Figure 32: Input and Output Waveforms of the VCO in Post-Layout Level**

4.2.2.4 Layout of MEMS Detection Block

The layout of the MEMS Detection block is given below in Figure 33:

**Figure 33: Layout Diagram of MEMS Detection Block**
4.2.2.5 Layout of the Proposed Circuit

The layout of the proposed MEMS readout circuit is given below in Figure 34:

Figure 34: Layout Diagram of the Proposed Circuit
The corresponding waveforms are shown in Figure 35:

![Waveforms of control voltage, VCO output and Input signals of the implemented readout circuit](image.png)

**Figure 35:** Post-Layout Level Waveforms of control voltage, VCO output and Input signals of the implemented readout circuit

**Table 4:** Simulated results of the post-layout level when DUT capacitance varies by ±25% from its nominal value of 65fF

<table>
<thead>
<tr>
<th>Reference MEMS Cap. (fF)</th>
<th>Delay (nS)</th>
<th>MEMS Cap. (fF) Determined via Simulation</th>
<th>% Error</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>48.75</td>
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</tr>
<tr>
<td>55.25</td>
<td>2.7728</td>
<td>55.3083</td>
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</tr>
<tr>
<td>58.50</td>
<td>2.9354</td>
<td>58.5514</td>
<td>0.0879</td>
</tr>
<tr>
<td>61.75</td>
<td>3.0980</td>
<td>61.7939</td>
<td>0.0711</td>
</tr>
<tr>
<td>65.00</td>
<td>3.2587</td>
<td>65.0000</td>
<td>0.0000</td>
</tr>
<tr>
<td>68.25</td>
<td>3.4191</td>
<td>68.1996</td>
<td>0.0738</td>
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<tr>
<td>71.50</td>
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</tr>
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<td>74.75</td>
<td>3.7434</td>
<td>74.6687</td>
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</tr>
<tr>
<td>78.00</td>
<td>3.9055</td>
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</tr>
<tr>
<td>81.25</td>
<td>4.0676</td>
<td>81.1350</td>
<td>0.1415</td>
</tr>
</tbody>
</table>
Table 4 shows the measured time delays in post-layout level for a ±25% variation of the MEMS capacitance. The “% Error” indicates a variation of less than 0.15%, which is very close to the result obtained from the schematic level.

Then the measurement variation of the capacitance is observed for the supply voltage is variation of ±5%. The obtained result is shown in Table 5. The %Error column shows a variation of capacitance of around 0.13%. This result is also effectively in agreement with the result obtained from schematic level.

Table 5: Simulated results of the post-layout level when supply voltage varies by ±5%

<table>
<thead>
<tr>
<th>VDD (V)</th>
<th>MEMS Cap. (61 fF)</th>
<th>% Error</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>Delay (nS)</td>
<td>Measured Cap. (fF)</td>
</tr>
<tr>
<td>0.95</td>
<td>3.0588</td>
<td>61.0728</td>
</tr>
<tr>
<td>1.00</td>
<td>3.0589</td>
<td>61.0751</td>
</tr>
<tr>
<td>1.05</td>
<td>3.0590</td>
<td>61.0774</td>
</tr>
</tbody>
</table>

Table 6: Simulated results of the post-layout level as the temperature varies from -50°C to 60°C

<table>
<thead>
<tr>
<th>Temperature (°C)</th>
<th>MEMS Cap (61 fF)</th>
<th>% Error</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>Delay (nS)</td>
<td>Measured Cap. (fF)</td>
</tr>
<tr>
<td>-50</td>
<td>2.6475</td>
<td>61.0189</td>
</tr>
<tr>
<td>-40</td>
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<td>20</td>
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<td>30</td>
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<tr>
<td>40</td>
<td>3.2652</td>
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<td>3.3340</td>
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</tr>
<tr>
<td>60</td>
<td>3.4028</td>
<td>61.0647</td>
</tr>
</tbody>
</table>
The effect of temperature variation on the performance of the readout circuit is also investigated through simulation for the same range of -50°C to 60°C. The measured capacitances as indicated in Table 6 match the reference values with a maximum error of around 0.11%. From Table 3 and Table 6, it is clear that the post-layout results match very closely with the schematic simulation results.
CHAPTER V
CONCLUSIONS AND FUTURE WORKS

A new readout technique for MEMS sensors has been proposed in this work. In the proposed scheme a single input is used instead of conventional two symmetrical inputs. A charge pump phase locked loop has been utilized to convert the variation of MEMS sensor capacitance to time domain signals. The proposed method exhibits a high measurement resolution due to the capability of a PLL to lock on the reference input signal. The proposed scheme also shows a robust performance against process, supply voltage and temperature variations due to the inherent feedback of the employed PLL. Post layout simulation results using TSMCE 65nm indicate that a measurement resolution of 73 aF for a MEMS capacitor can be achieved.

5.1 Contribution of the Proposed Method

The proposed readout scheme exhibits some major advantages compared to the conventional readout circuits. Due to the increased measurement resolution and robust nature against PVT variations, it can detect a very small variation of MEMS capacitance. The low sensitivity to PVT variations also increases the consistency of the measurement method. Furthermore, the simplicity of the circuit with the use of a very commonly used PLL circuit makes it less expensive.

5.2 Future Work

5.2.1 Inclusion of the BIST Technique

To further the effectiveness of the proposed method, a Built-In Self-Test (BIST) technique can be implemented. BIST allows testing the MEMS structure and detecting possible faults in the manufacturing stage or during the subsequent field applications.
BIST will make the circuit more cost-effective as it eradicates the necessity of costly external equipments to conduct operational tests on the device.

5.2.2 Extension to Other MEMS Devices

The main concept of this method is that the variation in MEMS capacitance is linearly proportional to the time delay. Any kind of capacitive MEMS sensor can be tested using this method. In this work, a combdrive [22] has been used as DUT. The same technique can be implemented for testing any other capacitive MEMS device such as Capacitive Micromachined Ultrasonic Transducer (CMUT).

5.2.3 Introduction to BISR Technique

The necessity of fault-tolerant or self-repairable MEMS devices is becoming more pressing. However, the very small size of a MEMS device and the introduction of on-chip MEMS device make the fulfillment of that kind of a promise very challenging. If one segment of the movable part is faulty, it is not feasible to physically remove the faulty part. On the other hand, if the fault can be detected with an on-chip testing device, the faulty MEMS sensor can be replaced with a good redundant module. Using this concept, a built-in self-repair (BISR) technique for any capacitive MEMS devices can be proposed. A control circuit can be integrated inside the chip to perform this task. If any module in the main device is found faulty by the BIST, the control circuit will separate out the faulty module and replace it with a good redundant module. Using this technique, the device can be self-repaired given the total number of faulty modules is less than the number of redundancy.
APPENDICES

Implementation Steps in TSMC 65nm Technology

The introduction of the basic usage of a TSMC’s PDK to the new users with less or no experience is the main intention of this appendix. In this section, we will design a PFD as an example and go through the whole design flow:

- **Schematic Capture:**
  - Creating library, design, symbol and test fixture

- **Pre-layout Simulation:**
  - Using Spectre simulator
  - TDC Performance

- **Layout Creation:**
  - Schematic-driven-layout
  - Component placement
  - Auto routing
Schematic Capture

Creating a Library:

- In the CIW, select “File>>New>>Library”
- Enter new library name into the Name field and press OK.
- Select “Attach to an existing techfile” and Press OK.
- Select “tsmcN65” and press OK

Creating a Cell view:

- In the CIW, select “File>>New>>Cell view”
- Select the desired library name into the Library Name field.
- Enter the new cell name into the name field.
- Select “Composer-Schematic” and press OK.
Creating a Design

Build the PFD schematic as stated below:

- In the PFD schematic window, click the instance fixed menu icon to display and Add Instance form.
- Click the “browse” button and select the required symbol from the specific library and cell.
- Then left click on the schematic window. It will place the symbol.
- The components required for this design:

<table>
<thead>
<tr>
<th>Component</th>
<th>Library Name</th>
<th>Cell Name</th>
<th>Required Number</th>
</tr>
</thead>
<tbody>
<tr>
<td>D-Flip-Flop</td>
<td>tcbn65gplus</td>
<td>DFCNQD1</td>
<td>2</td>
</tr>
<tr>
<td>NAND Gate</td>
<td>tcbn65gplus</td>
<td>ND2D0</td>
<td>1</td>
</tr>
<tr>
<td>Buffer</td>
<td>tcbn65gplus</td>
<td>BUFD0</td>
<td>3</td>
</tr>
</tbody>
</table>

- If you place a component with wrong parameter values, you can use the “Edit->Properties->Objects” command to change the properties.
- Now, add these pins by clicking “p”:

<table>
<thead>
<tr>
<th>Pin Name</th>
<th>Type</th>
</tr>
</thead>
<tbody>
<tr>
<td>A, B</td>
<td>input</td>
</tr>
<tr>
<td>Up, Down</td>
<td>output</td>
</tr>
<tr>
<td>VDD, VSS</td>
<td>inputOutput</td>
</tr>
</tbody>
</table>

- The final schematic should look as shown here:
Creating a Symbol

- In the PFD schematic window, select “Design > Create Cellview > From Cellview” and click OK.
- Assign the position of the pins as desired.
- Click “OK”. Then the symbol view will be created as shown in the figure.

Creating a Test Fixture

- The final step before starting the simulation is to create a test fixture. Generally the test fixture consists of the following components: a core design (the PFD in our case), voltage source, ground and other input values as shown in table.

<table>
<thead>
<tr>
<th>Library</th>
<th>Cell</th>
<th>Properties</th>
</tr>
</thead>
<tbody>
<tr>
<td>analogLib</td>
<td>vdc</td>
<td>For VDD=1V</td>
</tr>
<tr>
<td>analogLib</td>
<td>gnd</td>
<td>For VSS=0V</td>
</tr>
<tr>
<td>analogLib</td>
<td>vpulse</td>
<td>For A</td>
</tr>
<tr>
<td>analogLib</td>
<td>vpulse</td>
<td>For B</td>
</tr>
</tbody>
</table>
Parameter for Pin “VDD”

Parameter for Pin “A”

Parameter for Pin “B”

Circuit Diagram for the Test Fixture
Pre-Layout Simulation

- The design will be simulated with spectre simulator using Analog Design environment.
  For that, click “Tools->Analog environment”
- To set simulator to spectre, click “Setup>>Simulator/Directory/Host”
- Also set the project directory.
- Select analysis type and fill in parameters for simulation.
- Click “Ouputs>>To Be Plotted” to plot the desired outputs.
- Select “Simulation>>Netlist and Run” to run the simulation.
- The output log window will show the progress and status of the simulation.
Layout Creation

- From the PFD schematic menu select “Tools>>Design Synthesis>>Layout XL”.
- For new layout, select “Create New” and press OK.
- In the dialog box input the cell name and view name. Press OK.
- Two new windows will pop out. Those are the layout window and the LSW widow.
- From Virtuoso XL layout menu select “Design->Gen from source”.
- A layout generation options window appears and prompts to setup different parameters.
- Please refer to the figure beside for required input for basic layout generation.
- Click “Apply” and “Update”. Then Click OK to generate the initial layout diagram.
Component Placement:

- To place the components inside the cell boundary, click “Edit > Place As In Schematic”.
- Select and drag the devices/IO pins to proper location.
- Look for the lines representing the connections of selected object to other objects.

Configuring I/O Pins:

- In LSW window select layer to M1-pin.
- In the Virtuoso Layout window click “create>>label” and input the same name as the I/O pins.
Final Layout (Before Routing):

- The pins (colored white and blue) have to be inside the layout boundary (in violet). The pin names (in white) are zoomed big just for easy pickings.

Auto Routing

- Once the setup is complete, we send the design for auto routing.
- In the Virtuoso Layout window click “router>>export to router”.
- Fill up the required value as shown beside and click OK.
- A new window will pop up as shown in the next slide.
- Select “Use Rules File” and type “/CMC/kits/tsmc_65nm/CRN65GP/TN65CMSP018K1_V1.0C/icc.rules”
- Set the directory where to export.

Auto Routing Options:

- We can play with several options before sending for final routing.
- Click “Rules->Net->Width/Clearance”.
- We can change the path width and spacing between them, Noise, Crosstalk, Shielding, etc. as required.
Auto Routing (Final Step):

- Click “Autoroute>>Detail Route>>Detail Router”.
- Define the number of passes. Click OK.
- The auto-routed design will appear.
- You may click “Autoroute>>Clean” and this will fine tune the routing.
- Click “Quit and Save” and the routed design will appear on top of the un-routed layout window.

PFD Layout View:
REFERENCES


VITA AUCTORIS

NAME: Tareq Muhammad Supon

PLACE OF BIRTH: Barisal, Bangladesh

YEAR OF BIRTH: 1984

EDUCATION:

1. University of Windsor, Windsor, Ontario, Canada
   • Master of Applied Science (MASc) Sep 2010 – May 2012
     o Major: Electrical and Computer Engineering
     o CGPA: 11/13.00 (Letter Grade: A-)
     o Supervisor: Dr. Majid Ahmadi and Dr. Rashid Rashidzadeh
     o Thesis: A PLL based built-in self-test for MEMS sensors
     Work: I have proposed and implemented a novel BIST solution for capacitive MEMS sensors using phase locked loop (PLL).

2. University of Windsor, Windsor, Ontario, Canada
   • Master of Engineering (M.Eng.) Sep 2009 – Aug 2010
     o Major: Electrical and Computer Engineering
     o CGPA: 12/13.00 (Letter Grade: A)
     o Work: I have proposed a new technique to enhance the performance of Single Electron Junction (SET) 1-bit Full Adder during one of my course work. Later I published a conference paper with that work.

3. Ahsanullah University of Science and Technology, Dhaka, Bangladesh
   • Bachelor of Science (B.Sc.) May 2003 – Nov 2007
Major: Electrical and Electronic Engineering

Result: First Class First with honors in a class of 54.

CGPA: 3.77/ 4.00 (Letter Grade: A)

4. Amritalal Dey College, Barisal, Bangladesh
     - Major: Science
     - Marks: 79.1%

5. Barisal Zilla School, Barisal, Bangladesh
     - Major: Science
     - Marks: 85.1%

PUBLICATIONS:

- “A PLL Based Readout and Built-in Self-Test for MEMS Sensors”, Tareq Muhammad Supon, Krishnamohan Thangarajah, Rashid Rashidzadeh, Majid Ahmadi, IEEE MWSCAS 2011
  - This paper was short listed as one of the top eight articles among more than two hundred papers for the best paper award.
