A MEMS acoustical sensor array and associated micropackage.

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Abstract

This thesis develops the design methodology and fabrication procedures for a MEMS-based square planar acoustical sensor microarray for use in a hearing instrument to improve speech intelligibility in noisy and reverberant environments. The proposed microarray offers the potential of controlled directional sensitivity with a reasonably constant beamwidth over the audio frequency range when used in conjunction with an appropriate digital signal processor. The microarray consists of nine identical square-shaped capacitive-type acoustical sensors in a 3 x 3 planar layout and has a footprint area of 4.6 x 4.6 mm². Each sensor has a sensitivity of 10.3 mV/Pa when biased at 12 volts. A beamforming algorithm pertaining to MEMS realization of a square planar array of uniformly spaced identical acoustical sensors has been developed. A new analytical model has been developed that provides a better approximation to the pull-in voltage of capacitive type square diaphragm acoustical sensors as compared to existing models.

A MEMS-based three-dimensional modular package has been developed for the microarray where silicon has been used as the package material. The package realizes a complete microsystem by holding the microarray, necessary microelectronics dies and a power source in stacked submodules. Two different schemes have been developed to establish intermodular electrical connectivity. The first scheme uses pressure-dependent cantilevered bridge-type microspring
contacts that are fabricated as an integral part of a package submodule. The second scheme uses a MEMS-based microbus card to establish intermodular connectivity by using interconnection channels that are present in each package submodule.

The design methodology and fabrication process was developed through the extensive use of simulation tools. The actual fabrication processes have been simulated and the resulting microstructures have been analyzed using three-dimensional electromechanical finite element techniques (FEA). The FEA results closely match theoretical values predicted by the design methodology.

The design has been sent for analysis and prototype fabrication costing to the Corning-IntelliSense Corporation. The design was found to be robust and a price quotation for the microarray fabrication has been received. The physical implementation will take place when the collaborating private sector firm and a MEMS foundry have reached a confidentiality agreement.
To my wife, Shamima; and sons, Sakib and Shahir.
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<th>Description</th>
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<tbody>
<tr>
<td>$X, Y, Z$</td>
<td>Rectangular coordinates</td>
</tr>
<tr>
<td>$C_{Sensor}$</td>
<td>Sensor capacitance</td>
</tr>
<tr>
<td>$\varepsilon_0$</td>
<td>Permittivity of free space</td>
</tr>
<tr>
<td>$A$</td>
<td>Diaphragm area</td>
</tr>
<tr>
<td>$d_t$</td>
<td>Airgap thickness</td>
</tr>
<tr>
<td>$d_x, d_y$</td>
<td>Sensor element spacing</td>
</tr>
<tr>
<td>$c$</td>
<td>Velocity of sound in free space</td>
</tr>
<tr>
<td>$\theta, \phi$</td>
<td>Spatial angle</td>
</tr>
<tr>
<td>$\kappa$</td>
<td>Wave number</td>
</tr>
<tr>
<td>$\omega$</td>
<td>Radian frequency</td>
</tr>
<tr>
<td>$\psi_x, \psi_y$</td>
<td>Time delay</td>
</tr>
<tr>
<td>$\beta_x, \beta_y$</td>
<td>Progressive phase shift</td>
</tr>
<tr>
<td>$\lambda$</td>
<td>Wave length</td>
</tr>
<tr>
<td>$f$</td>
<td>Frequency</td>
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<tr>
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<td>Number of delay elements</td>
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<td>$d_{xx}, d_{yy}$</td>
<td>Physical array element spacing</td>
</tr>
<tr>
<td>$d_{xc}, d_{yc}$</td>
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</tr>
<tr>
<td>$D_x, D_y$</td>
<td>Electronic beam deflection angle to realize constant beamwidth</td>
</tr>
<tr>
<td>$Wf_x, Wf_y$</td>
<td>Weight factor to adjust beam height</td>
</tr>
<tr>
<td>$\psi_x, \psi_y$</td>
<td>Composite delay</td>
</tr>
<tr>
<td>$V$</td>
<td>Voltage</td>
</tr>
<tr>
<td>$M$</td>
<td>Mass</td>
</tr>
<tr>
<td>$F_E$</td>
<td>Electrostatic force due to bias voltage</td>
</tr>
<tr>
<td>$K$</td>
<td>Mechanical spring constant</td>
</tr>
<tr>
<td>$z$</td>
<td>Z-axis displacement</td>
</tr>
<tr>
<td>$F_M$</td>
<td>Mechanical elastic force</td>
</tr>
<tr>
<td>$d_0$</td>
<td>Initial airgap thickness</td>
</tr>
<tr>
<td>$V_{PI}$</td>
<td>Pull-in voltage</td>
</tr>
<tr>
<td>$z_{PI}$</td>
<td>Pull-in deflection</td>
</tr>
</tbody>
</table>
$d_{Pl}$  
Airgap at pull-in deflection

$\omega_{res}$  
Mechanical resonant frequency in radians/s

$C_{1M}, C_{2M}$  
Numerical fitting parameters

$t_d$  
Diaphragm thickness

$h_0$  
Deflection of the diaphragm midpoint

$h$  
Diaphragm deflection at different coordinate positions

$a$  
Square diaphragm side length

$b$  
Half of square diaphragm side length

$E$  
Young’s modulus

$\hat{E}$  
Fringe filed corrected effective Young’s modulus

$\nu$  
Poisson’s ratio

$P$  
Uniform pressure

$\sigma$  
Residual stress

$a_c$  
Circular diaphragm radius

$r_c$  
Radial position in a circular diaphragm

$D$  
Diaphragm rigidity

$K_1$  
Circular diaphragm tension parameter

$t$  
Time

$i(t)$  
Current due to flow of charge

$Q(t)$  
Charge

$\bar{v}(t)$  
Velocity of the diaphragm

$d_b$  
Airgap after diaphragm deflection due to bias voltage

$Z_m$  
Mechanical impedance of a sensor geometry

$Z_a$  
Acoustical impedance of air in contact with diaphragm

$Z_t$  
Total impedance of the sensor structure when subjected to external acoustical pressure

$S$  
Sensitivity

$V_o$  
Sensor output voltage

$M_r$  
Air mass

$M_m$  
Diaphragm mass

$R_r$  
Air radiative resistance

$C_m$  
Diaphragm compliance

$R_g$  
Airgap viscous resistance
\( R_h \)  Viscous resistance due to back vent holes
\( \alpha_{bh} \)  Surface fraction occupied by holes
\( C_a \)  Airgap compliance
\( \eta \)  Viscosity of air
\( \rho_0 \)  Density of air
\( T_D \)  Diaphragm tension
\( R_a \)  Total acoustical resistance due to airgap and the acoustical ports
\( K_B \)  Boltzman's constant
\( T \)  Absolute temperature
\( F_n \)  Spectral density of fluctuating force
\( p \)  Spectral density of the fluctuating pressure
\( L_A \)  A-weighted noise
\( A_i \)  A-weights following the A-curve
\( L_i \)  1/3 or 1/1 octave band level (dB SPL)
\( \dot{M} \)  Mass matrix
\( \dot{B} \)  Damping matrix
\( \dot{K} \)  Stiffness matrix
\( \alpha \)  Mass damping factor
\( \beta \)  Stiffness damping factor
\( \xi_i \)  Mode damping factor
\( Q_i, Q_M \)  Quality factor
\( \sigma_{UT} \)  Ultimate tensile strength
\( \sigma_{VM} \)  von Mises stress
\( \sigma_{P1}, \sigma_{P2}, \sigma_{P3} \)  Principal stresses
\( \alpha_S \)  Coefficient of thermal expansion
\( \delta_S \)  Tip deflection of a cantilever beam on the microbus card
\( A_{off} \)  Effective area to evaluate Hertzian contact resistance
\( R_c \)  Contact resistance
\( r_c \)  Radius of contact area used to evaluate Hertzian contact resistance
\( \rho \)  Electrical resistivity
\( T_r \)  Signal rise time
$v_p$  Propagation velocity
$C_1$  Oxide capacitance
$C_2$  Substrate capacitance
$G_S$  Substrate conductance
$R_{DC}$  DC resistance
$R_{AC}$  AC resistance
$L$  Self inductance
$w$  Width of an interconnect trace
$t_{ic}$  Thickness of an interconnect trace
$h_{ic}$  Height of an interconnect trace above ground plane
$f_{skin}$  Frequency at which skin depth equals conductor thickness
$\mu_0$  Permeability of free space
$L$  Inductance
$\delta$  Skin depth
$\varepsilon_r$  Average dielectric constant of a microstrip
$\varepsilon_{eff}$  Effective dielectric constant of a microstrip
$\gamma$  Propagation constant
$H(\omega)$  Frequency domain transfer function
Chapter 1

Introduction

1.1 Goals

For persons using hearing instruments, improving speech intelligibility in an acoustic environment associated with background noise and multipath distortion is a major technical challenge. The availability of a hearing instrument microphone with dynamically variable directional sensitivity can contribute to improving speech intelligibility for persons using hearing instruments. The technology associated with microelectromechanical systems (MEMS) offers the capability of fabricating a beamforming array of MEMS-based acoustical sensors with the potential to provide improved performance comparing to conventional microphone based speech acquisition systems. The overall goal of this research work is to design and develop a MEMS-based beamforming acoustical sensor microarray that can enable dynamic directional sensitivity. The resulting microarray dimensions must be sufficiently small so as to allow it to be mounted in the ear canal to provide enhanced speech intelligibility in a noisy reverberant environment. The acoustical array is to be used in conjunction with a special digital signal processor (beam steering engine) and associated algorithms to achieve dynamic directional sensitivity.
Omnidirectional acoustical sensors capture sound from all directions. The directional pattern of an omnidirectional microphone is shown in Figure 1-1a. A single directional microphone having a cardiode or a super cardiode type directional pattern cannot provide adequate improvement of the speech intelligibility. Instead of using a single omnidirectional or directional microphone, if a rectangular array of microphones is used, it is possible to form a highly directional beam with a sufficiently constant beamwidth for a desired frequency range using the techniques of spatial filtering (also known as beamforming) as is shown in Figure 1-1b. Signals coming from directions other than the beam pattern will be cancelled out automatically thereby reducing background noise and multipath distortion. If a beam can be formed, it is also possible to steer the beam within certain spatial limits as shown in Figure 1-1c to incorporate a speaker tracking capability.

The beamforming techniques range from conventional delay and sum beamforming, adaptive beamforming, and arrays with adaptive post-filtering [1]. Delay-and-sum based beamforming is robust and uses a less complex algorithm, but suffers from the limitations of a low spatial resolution that is dependent on the sampling frequency [2]. For the delay-and-sum beamforming, it is required that the sensor elements must be spaced at a distance of half the wave length of the desired frequency to satisfy Nyquist rate of spatial sampling to avoid spatial aliasing effects and to maximize power in the main beam [1]. The adaptive beamforming techniques have a limited functionality in an environment associated with multipath distortion and reverberation [3].
Figure 1-1. Beamforming and beam steering concept illustration. (a) Directional pattern of an omnidirectional acoustical sensor. (b) Directional pattern of a square planar array of acoustical sensors. (c) Steered beam pattern of a square planar array of acoustical sensors. Red color indicates highest intensity.
One crucial requirement for applying a beamforming technique is that all the acoustical sensor elements in the array must have matched sensitivity and frequency response [4]. This requirement cannot be fulfilled by an array of standalone acoustical sensors as the frequency response and sensitivity of each sensor element vary during standalone manufacturing and assembly process.

MEMS implemented capacitive-type voltage controlled acoustical sensors (microphones) has been demonstrated to have excellent performance metrics regarding size, power consumption, frequency response, low noise, and sensitivity [5]-[8]. Since MEMS technology offers the advantage of fabricating sensor elements that can be fabricated simultaneously as a single die, the matching of frequency response and sensitivity for each microphone is not a problem. The limitation of spatial resolution in such close proximity array elements can be overcome by controlling the sampling frequency in a manner such that the spatial resolution does no more depend on the physical array's element spacing. This is possible by electronically delaying the individual microphone signals to give the effect of larger array size and spacing. A planar symmetrical array of square shaped acoustical sensors may provide the best utilization of the available space while providing the desired functionality.

A MEMS capacitive-type acoustical sensor is basically an electrostatic transducer that depends on electrical energy, generally in terms of a constant bias voltage source to facilitate monitoring of capacitance change due to an
external acoustical pressure. A typical geometry of a MEMS-based capacitive-type acoustical sensor is given in Figure 1-2.

However, electrostatic force associated with the bias voltage is nonlinear due to its inverse square relationship with the airgap thickness between the capacitor electrodes. This gives rise to a phenomenon known as 'pull-in' that reduces the dynamic range of the diaphragm displacement to one-third of the airgap. If the

![Diagram of a capacitive-type acoustical sensor](image)

(a)

Figure 1-2. A capacitive-type acoustical sensor. (a) Cross-sectional view. (b) Functional concept.
bias voltage exceeds this pull-in limit, the diaphragm will collapse. In addition, the initial deformation of the diaphragm due to the electrostatic force causes an offset error in the readout circuit [9]. Applications, such as hearing aid instruments using this kind of microphone need additional electrical circuits to minimize this bias voltage dependent offset error. Furthermore, this initial diaphragm deformation reduces the airgap thickness that in turn reduces the dynamic range of the microphone.

Accurate determination of the pull-in, or the collapse voltage is critical in the design process. Unfortunately, the commonly used parallel-plate approximation method of pull-in voltage determination introduces significant errors (~20%) if the diaphragm is fully clamped [10]. Whereas 3-D finite element electromechanical analysis or finite difference methods are very much time consuming. In addition, for a clamped diaphragm, the small deflection model of diaphragm deformation does not account for nonlinearities associated with the presence of in-built residual stress in the diaphragm and predicts unrealistically high deformation values. Thus, it is necessary to formulate a method to determine the pull-in voltage that accounts for the nonlinear nature of the design parameters. In [10], an empirical method is provided to approximate pull-in voltage for cantilevers, fixed-fixed beams and circular diaphragms under electrostatic actuation. The method can evaluate pull-in voltage for the mentioned geometries within 1% agreement with finite element analysis results under certain limitations. However, there is no definitive analytical method to determine the pull-in voltage if a clamped diaphragm is square or rectangular. It is desirable to have a fast,
simple, and easy to use analytical or empirical method to determine the pull-in voltage of a microphone structure with a square diaphragm. Most of the other design parameters, such as the sensitivity, noise, frequency response, etc. depend crucially on the accurate determination of the pull-in voltage. Providing acoustical ports in the backplate help to reduce the air damping effect that in turn affects the sensor's frequency response and noise performance [5] [11] [12].

In order to have a viable working system the design of the acoustical sensor array must be developed in concert with the associated packaging design. MEMS technology still lacks the capability of fabricating an acoustically transparent protective thin film symmetrical dome over the array that will not interfere with beamforming or beamsteering. Thus, environmental contamination may damage or perturb the array's variable directional properties and overall sensitivity in course of time. It is thus necessary to develop a custom packaging solution to protect the sensor array and to provide interconnection between the sensor array and the necessary drive and control microelectronics circuitry that will allow for easy mounting and removal of the sensor array. The major design issues in this regard include the need for easy sensor array mounting and removal, high performance connectivity, minimized transmission line effects, proper frequency response and low insertion losses. Conventional packaging solutions including flip-chip bonding cannot resolve this issue. It is possible to exploit the capabilities of the MEMS technology to develop a custom micropackaging solution that can address the above packaging and connectivity issues. A modular MEMS-based micropackaging solution can be developed by
stacking required numbers of micropackage submodules secured together by longitudinal microbolts. Each package submodule basically is a socket type structure of desired geometry fabricated out of a silicon wafer. The sensor microarray can be accommodated in one of the micropackage submodule through special fixture or can be constructed to constitute one of the micropackage submodules. Control and drive electronics circuitry can be accommodated in other micropackage submodules in die level. A micropackage submodule can accommodate the required power supply battery. Non-permanent but reliable electrical connectivity between the package submodules can be established by using high performance microspring contacts or through the use of a custom designed removable and programmable microbus card. In this way a complete working system can be realized in a micropackage. As the identical micropackage submodules can be batch fabricated, this will speed up the entire packaging process. Whenever necessary, the sensor array can be removed form the micropackage submodule for cleaning or replacement purpose. The modular integration method also will facilitate easy integration of some additional functionality to the system in future.

In summary, this thesis investigates the development of a MEMS-based acoustical sensor microarray to provide enhanced speech intelligibility in a noisy reverberant environment. The specific design objectives are:

1. To develop a mathematical model of beamforming theory pertaining to very close proximity MEMS-based acoustical sensors that is to be fabricated as a single die.
2. Develop and verify an analytical model for more accurate determination of pull-in voltage related to a voltage controlled MEMS-based square diaphragm acoustical sensor.

3. Carry out the design of the MEMS-based acoustical sensor microarray based on the developed models. To verify the developed 3-D geometry of the sensor microarray by extensive 3-D electromechanical finite element analysis using IntelliSuite™ [13] MEMS design tools. Development and simulation of a fabrication process table using IntelliSuite™ for the sensor microarray fabrication with appropriate design rule check.

4. Development of a modular custom application specific micropackaging solution to integrate the microarray with required drive and control microelectronic circuitry. The packaging solution will incorporate MEMS-based interconnection schemes, such as microspring contacts and a microbus card to provide high performance interconnectivity between the sensor microarray and required drive and control microelectronic circuitry. Development and simulation of a fabrication process table for the micropackage and verification of the developed 3-D geometry including design rule check. Carry out 3-D electromechanical and thermomechanical finite element analysis to optimize the design requirements of the interconnectivity mechanisms.
1.2 Background

Background noise and multi-path distortion in an acoustic environment are major factors limiting speech intelligibility, especially for hearing instrument users [14] [15]. Several methods have been explored to eliminate background noise and improve speech intelligibility in noisy and reverberant environments [16] [17] [18]. A microphone array with directional sensitivity that can be steered electronically based on speaker tracking or other information-rich algorithms may provide increased speech intelligibility to hearing challenged persons. The steerable spatial response of the array should also be frequency invariant over the desired range of frequencies. Single cardiode or supercardiode type microphone [19], combination of one or more directional and omnidirectional microphone in the form of an array where individual microphones are arranged at different locations around the head sphere [4] or in the form of a wearable necklace where the signal from the microphones is being picked up by telecoils [20]. These have been found to be effective in eliminating background noise and improving speech intelligibility to some extent [21]. Single directional microphones cannot provide adequate directionality whereas external connectivity in the cases of wearable necklace is vulnerable to damage and inconvenience to the users. Furthermore, there's a mismatch in the frequency response and sensitivity of the standalone microphones used to construct an array. To achieve beamforming capability, the signal output of each microphone in an array type arrangement must be processed electronically to realize a beamforming algorithm as described in section 1.1.
There have also been attempts to build MEMS-based acoustical sensor arrays. The two most representative systems are described in [22] and [23]. In [22], 16 standalone MEMS-based piezoresistive microphones are mounted on a planar printed circuit board using a hybrid package. The overall package dimension is 9.88 centimeters. The package is considerably large, is not automated, and not suitable for space constraint applications, e.g. in a hearing instrument application. No detailed MEMS-based design methodology or fabrication methods for the microphones are given. The system is intended for use in aeronautical applications to measure aircraft noise.

In [23], three linear arrays of MEMS-based capacitive-type microphones having 4 (four), 8 (eight) and 8 (eight) numbers of different diameter microphones, respectively that span a baseline width of 7.75 mm are reported. The microphones have circular membranes suspended on support pillars. The largest microphones have a diameter of 0.82 mm and are spaced 1.3 mm. The smallest microphones have diameters of 0.2 mm and are spaced 0.65 mm. Linear arrays with circular type microphones cannot provide an optimal use of the available area whereas a complete investigation of the effect of air streaming out of the airgap between the backplate and a suspended membrane was nor carried out. Besides, very small microphone diaphragm (0.2 mm diameter) results in a lower sensitivity. The operating frequency range was not specified as for speech acquisition application, a constant beamwidth covering a desired audio frequency range is vital. This device was intended for use in ultrasonic applications for underwater source localization.
For space constraint speech acquisition applications, the obvious design requirements are (1) small size, (2) high sensitivity, (3) low-power, (4) low-noise, (5) matched frequency response and sensitivity for array elements, (6) speaker tracking capability, and (7) easy packaging and maintenance capability. The complexity of the beamforming algorithm must be considered in a practical implementation of the complete system. Less computationally expensive, reasonably constant beamwidth, and high-speed signal processing capability are some of the requirements.

MEMS-based microphones offer advantages due to their small size, relatively high sensitivity, batch fabrication capability, inherently low-power consumption and low-noise features. Piezoresistive, capacitive, and electret: - are the three major categories of microphones that have been fabricated successfully using MEMS technology. Capacitive-type microphones offer certain advantages over the piezoresistive or the electret ones in terms of relatively higher sensitivity, ease of fabrication, maintainability, etc. Thus capacitive-type microphones can be chosen as the elements of the proposed array.

Serious research efforts have been made to improve the design methodology and performance of MEMS-based capacitive-type microphones [5]-[8]. They have been fabricated using bulk micromachining with a silicon nitride backplate, combination of bulk and surface micromachining with a boron doping of the substrate to act as an etch stop for anisotropic backside etch of the substrate and a polysilicon diaphragm, bulk micromachining with a polyamide diaphragm and integrated CMOS circuitry, and differential diaphragm to minimize electrostatic
offset error. All these designs need high voltage anodic bonding to a glass substrate to facilitate surface mounting and the high voltage applied during the anodic bonding process can cause the diaphragm to collapse during the process [9]. Besides, Bulk micromachining of the silicon substrate using anisotropic etch through the wafer backside using KOH to facilitate release of the sacrificial layer between the diaphragm and the backplate creates a 54.7 degree slope as the anisotropic etch cuts through the <111> crystal plane. As a result, the area offset by the slope cannot be used as an active area for sensing thus reducing the available sensing area.

Instead of etching the substrate backside, if it is possible to remove the sacrificial layer (silicon dioxide, for example) through the topside of the die, it will be possible to have a flat die bottom, thus facilitating surface mounting without anodic bonding. Deep reactive ion etching through the wafer topside can be used to create the required inner cavity for air damping. In this way, a highly optimized array geometry can be realized. Use of a low-stress, low-resistivity, highly conformal polysilicon germanium (Poly-SiGe) layer as the diaphragm material will result in a higher sensitivity and some effects associated with fabrication can be minimized.

The temporary integration of the MEMS device (sensor microarray) and the microelectronic circuitry requires a highly optimized interconnection mechanism. Industry experience has revealed that the establishment of temporary connectivity to a pre-deposited solder ball on a die I/O pad is becoming increasingly difficult with decreasing feature size and gives rise to new technical
concerns [24] [25]. Connectivity based on prefabricated microsprings on the die I/O pad exposes the active circuitry on the die to thermal and mechanical energy used to form the microsprings [25]. In another currently available method, where the connectivity is based on depositing a sacrificial layer on the die I/O pad adds additional fabrication process steps, thus adds extra cost [24].

In this thesis, a new type of 3-D packaging solution is demonstrated where a temporary connectivity between a MEMS device and the CMOS microelectronic circuitry has been achieved without exposing the chip to any kind of external energy that may be harmful [25] to the dies or devices. The proposed packaging solution enables vertical integration using two different approaches. In the first approach, cantilevered bridge-type microspring contacts using wafer-through-hole aluminum-via-interconnects are used. In the second approach, a custom designed removable microbus card is used to achieve the desired connectivity. Both the systems enable vertical integration of dies or devices that helps to reduce number and average length of global wire by providing shorter "vertical" paths for connection in addition to establishing low contact resistance connectivity. This 3-D integration capability also helps to reduce overall chip area and enables new system architecture [26]. The 3-D packaging solution can be adopted for System-on-Chip (SoC) applications, where dies of different technological origin (0.18 μm or 0.08 μm) can be placed on different package submodule or dies of different functionality, such as digital, memory, analog, and RF, etc. can be located on different suitable layers. For example, digital circuits could be located on a bottom submodule, adjacent to the heat sink and lower-
power/higher-voltage analog circuits on a top package submodule close to the MEMS device.

1.3. Principal Results

The principal results of this thesis are summarized below:

1. The theory of a beamforming concept pertaining to MEMS realization of closely spaced square planar array of acoustical sensors has been developed. The sensor array can provide directional sensitivity to improve speech intelligibility in a noisy reverberant environment. The model, based on the classical delay-and-sum beamforming technique incorporates an electronic delay term in addition to the delay due to physical array element spacing to satisfy Nyquist rate of spatial sampling. The model also is capable of maintaining a reasonably constant beamwidth that covers a desired audio frequency spectrum. The beam is steerable and facilitates a speaker tracking capability.

2. An analytical model has been developed to evaluate the pull-in voltage of a MEMS-based capacitive-type acoustical sensor having a square-shaped diaphragm. The analytical model is able to determine the pull-in voltage within 2.5% error limit in comparison to finite element or experimental results. The model incorporates spring softening effect associated with electrostatic force and also spring hardening effect associated with a rigidly clamped diaphragm with built-in residual stress. The model was validated by comparing the results with finite element
methods and also with published experimental results of similar geometries. The model can be extended to determine pull-in voltage in case of fixed-fixed beams, cantilever beams and circular diaphragm cases.

3. The design of a MEMS-based square planar array of acoustical sensors has been carried out based on the developed beamforming theory and the pull-in voltage model. The array, consisting of nine acoustical sensors in a 3 x 3 planar layout has a footprint area of 4.6 x 4.6 mm². The geometry of the microarray has been optimized for a space-constraint application area. Using polysilicon-germanium (Poly-Sige) as the diaphragm material and specific fabrication process steps, it was possible to realize a sensitivity of 10.3 mV/Pa for each sensor element having a diaphragm side length of 1.2 mm. A fabrication process table has been developed to fabricate the array. The process table has been simulated using the IntelliSuite™ MEMS design tools to check for desired geometry and process compatibility. The 3-D model generated by the fabrication process simulation matches the design expectations. 3-D static and dynamic electromechanical finite element analysis results match closely with analytical values thereby validating the design process.

4. A 3-D MEMS-based modular micropackaging solution has been developed for temporary integration of the sensor array with the necessary drive and control electronics and power supply battery to
realize a complete working system in a micropackage. The interconnectivity among the package submodules is to be achieved, either by cantilevered bridge-type microspring contacts or by a microbus card. The microspring contacts have been simulated for desired behavior using 3-D electromechanical and therommechanical finite element analysis with satisfactory results. The process steps to fabricate the package submodule, the cantilevered bridge-type microspring contacts and the microbus card were developed and simulated using IntelliSuite™ design tools to generate 3-D models that satisfy the design requirements.

5. This research work has been financed by the Gennum Corporation of Burlington, Ontario. Currently, negotiations are underway to fabricate the sensor array and the micropackage in the foundry of the Corning-IntelliSense Corporation of Wilmington, MA. Corning-IntelliSense Corporation has validated the fabrication process table and quoted $275,000 USD for a prototype run. The devices can be fabricated when the funding is available.

1.4 Thesis Organization

This thesis has been organized in the following manner. Chapter 2 identifies the design requirements and constraints associated with the design and implementation of a MEMS-based acoustical sensor array for use in a hearing aid instrument. A beamforming theory compatible for an array having close-
proximity array elements is developed based on the conventional delay-and-sum beamforming method. Chapter 3 concentrates on identifying the relevant theoretical models to optimize the design parameters of a MEMS-based capacitive-type acoustical sensor. A new analytical method has been developed to determine the pull-in voltage for a MEMS-based capacitive-type acoustical sensor having square shaped diaphragms. Chapter 4 presents the design process of the proposed microarray based on the theory developed in chapter 2 and 3 along with constraints associated with the target application, viz. a hearing instrument that can be mounted in the ear canal. The developed array structure has been simulated using 3-D electromechanical finite element analysis for design verifications. A process table was developed that describes the MEMS fabrication process steps in details and has been simulated using the IntelliSuite™ MEMS design tool to verify the 3-D geometry and process check. Chapter 5 presents the design of a MEMS-based modular micropackaging solution. The design steps associated with the micropackage has been identified and carried out to optimize the electrical, mechanical and thermal parameter values for a micropackage submodule. A process table was developed by using the IntelliSuite™ MEMS design tools to fabricate a micropackage submodule and was simulated to verify the 3-D geometry. Chapter 6 presents the conclusions. Appendix I illustrates the idea of die testing using the developed modular packaging concept. Appendix II contains the IntelliSuite Report File generated from the process table developed to simulate the sensor microarray.
Chapter 2

Microarray Beamforming Theory

In this chapter, the design considerations for the proposed sensor microarray has been described with values and constraints that are associated with an acoustical sensor microarray that has the potential to be integrated with hearing instrument microelectronics and is sized for the ear canal. Specifically, relevant constraints associated with the MEMS implementation of the microarray and the physical constraints related to the kind of application have been identified. These constraints are then mapped into the classical delay-and-sum beamforming technique to develop a mathematical model for a microarray broadband beamforming theory.

2.1 Microarray Design Considerations

2.1.1 Fabrication Process Related Constraints

The MEMS technology offers the capability of fabricating three-dimensional microstructures, such as sensors or actuators using processes similar to VLSI technology. However, MEMS offers much higher number of material choices, exploits a wider set of physical properties for device functionality, and utilizes a diverse set of processes to meet the electrical, as well as mechanical design requirements of a particular design. Some fabrication process steps related to
the deposition and removal of the materials are expensive, equipment and foundry specific, and demands critical setup. To maximize the yield, to take the advantage of batch fabrication, and for best utilization of the wafer space, it is imperative to fabricate as many dies on a single wafer as supported by the fabrication process related constraints, such as, mask alignment, UV wavelength, minimum permissible feature size, layer overlap, allowable mask offset, etc. Additional lateral space may also be required for dicing, packaging, interconnection, and die handling purposes. For an array of MEMS-based acoustical sensors that can be fabricated as a single die, the spacing between the adjacent sensor elements is thus to be minimized based on the above fabrication process related constraints.

2.1.2 Maximum Die Size

Another constraint arises from the dimensions of the application area or type. For example, for a hearing instrument application intended for placement in the ear canal, the application area is limited by a diameter of approximately 8.0 mm, the average diameter for an adult ear canal. Some space is required to be left for ear mold and airflow purposes. Thus, the sensor array specifications must satisfy this physical constraint.

2.1.3 Sensor Type Selection

A capacitive-type acoustical sensor (microphone) has been chosen as the enabling microarray element as they offer high sensitivity to acoustical pressure variations; flat frequency response, are not affected greatly by temperatures
variations; have low-power requirements, and failure modes are easier to detect [5] [27].

Referring to Figure 1-2, assuming the space between the diaphragm and backplate filled with air and neglecting fringe field capacitance, the sensor capacitance, $C_{\text{sensor}}$, of the structure can be expressed as:

$$C_{\text{sensor}} = \frac{\varepsilon_0 A}{d_s}$$  \hspace{1cm} (2-1)

where $\varepsilon_0$ is the permittivity of the free space, $A$ is the effective sensing area and $d_s$ is the thickness of the airgap.

An important design parameter of a sensor is its sensitivity that reflects the sensor's capability in transducing the input signal (e.g., acoustical pressure) into an electrical output signal (e.g., a voltage or a current) [9]. For a capacitive-type acoustical sensor, the output voltage is dependent on the change of capacitance, $\Delta C$, due to an external acoustical pressure. It is evident from (2-1) that this change of capacitance is a direct function of the effective sensing area for a given airgap. Thus, a larger sensing area will result in a higher change of capacitance and will provide a higher sensitivity. For a space constraint application, the effective sensing area should thus be maximized while taking into account the fabrication constraints described above and the other design parameters must fit this requirement accordingly.
2.1.4 Sensitivity of the Readout Circuitry

For MEMS-based acoustical sensors, the zero acoustical pressure capacitance is typically of the order of a few picofarads and the change in capacitance due to an external acoustical pressure is of the order of a few femtofarads [27]. A change of one percent requires a reliable detection of capacitance change of the order of 0.1 femtofarad or less. At this very small scale of capacitance change, the parasitic capacitance associated with the readout circuitry and interconnection mechanism, itself may also contribute to a significant error in the readout of the sensor output. Thus, the performance of capacitive pressure sensors depends critically on the capability of the circuit used for signal readout. A low-power switched-capacitor readout circuitry, generally a charge integrator coupled with an amplifier is able to provide a readout resolution of 1.0 femtofarad [28]. If the capacitance change is smaller than the minimum detectable threshold of the readout circuitry, the noise associated with the readout circuitry itself will runoff the signal. Thus, the availability of an appropriate readout circuit offers a design constraint that limits the minimum sensor geometry.

2.1.5 DC Bias Voltage

The sensor capacitance increases with the DC bias voltage in an exponential-like manner in the range of operation of interest. The bias voltage is chosen to ensure that the sensor is operating in the middle of the linear range with the largest dynamic range available on the capacitance versus bias voltage curve to ensure maximum sensitivity (mV/Pa). The sensitivity of a capacitive-
type acoustical sensor increases as the DC bias potential between the plates increases. In a reported experiment [29], a MEMS capacitive-type acoustical sensor (microphone) with a bias of 10 Volts DC exhibited a sensitivity between −44 and −36 dB from DC to 10KHz and a decreased sensitivity by 5.0 to 8.0 dB with a bias voltage of 5.0 VDC (dB, ref. 1V/Pa). The sensor element had a capacitance value of 16.2 pF with zero bias voltage applied [29]. The electrostatic attraction force between the diaphragm and the backplate caused by the DC bias voltage may cause the diaphragm to collapse if the bias voltage exceeds the pull-in limit. DC-to-DC voltage converter [7] circuits can provide a suitable bias voltage from a commercial battery of 1.5 V. Battery technology has also advanced and mm-scale rechargeable batteries are available for this purpose [30]. The choice of an appropriate bias voltage is one of the most crucial design parameter. A detailed analysis on DC bias voltage selection is discussed in Chapter 3.

2.1.6 Operating Frequency Range

The sensor's frequency response is dependent on the acousto-mechanical impedance of the device geometry. For stable operation, the sensor's resonant frequency should be higher than the operating frequency range. The sensor's resonant frequency depends on the material properties and structural geometry of the sensor element. The nonlinearity of the electrostatic force associated with the bias voltage causes a downshift of the resonant frequency of the sensor structure, an effect known as spring softening [31]. Thus, the chosen bias voltage must not cause the mentioned downshift of the resonant frequency to a
level that interferes with the desired audio frequency range. Providing acoustical ports in the backplate will reduce the air damping effect thereby airgap resistance, and thus will contribute to increase the upper frequency limit. However, if the ratio of the area covered by the acoustical ports is greater than about one-third of the backplate area, an amplitude minimum, known as antiresonance will occur due to lower resonance frequency of the backplate and will cause a decrease in the operating frequency range [5].

2.1.7 Adjacent Sensor Element Spacing

Besides the fabrication constraints associated with the minimum feature size as described in section 2.1.1, the minimum adjacent element spacing depends also on the array element contact pad size, interconnect dimensions, and the width, spacing, and routing of the interconnect traces. Spatial aliasing problems associated with the microarray dimensions must be solved electronically.

2.1.8 Number of Array Elements and Diaphragm Area

The total number of sensors and the diaphragm area of each sensor can be determined from the array size constraints, fabrication process related constraints, and the minimum required adjacent sensor spacing criteria.

2.1.9 Airgap Thickness

The upper limit of the airgap thickness is influenced by the thickness of the sacrificial layer permitted by the available fabrication process (conformal deposition and etching) and choice of the sacrificial material. For a given diaphragm size, the airgap thickness specification must take into account the
magnitude of the diaphragm deflection due to both the acoustical and electrostatic forces. The nonlinear effect of the electrostatic attraction force causes the diaphragm to collapse on the backplate if the bias voltage exceeds the pull-in limit. For a parallel plate configuration, the deflection at pull-in is one-third of the airgap whereas for a clamped diaphragm case, the diaphragm can deflect little further before it collapses [10]. As the electrostatic attraction force is in inverse square relationship with the airgap thickness, the chosen airgap thickness must ensure failsafe operation in the non-collapse deflection zone, preferably less than one-third of the airgap, when the diaphragm is under combined effect of the electrostatic force and the external acoustical pressure. If the airgap is too thick, the change of capacitance will be small and will result in a lower sensitivity. The relative values of the bias voltage and the collapse voltage also influence airgap thickness, the sensor's dynamic range, as well as damping effects associated with air compression in the gap. If the airgap is too thin, the squeeze film damping will cause a higher acoustical resistance and that will contribute to an increase in the sensor's self noise.

2.1.10 Sensitivity

The capacitive-type acoustical sensor can be viewed as a mechano-electric transformer that transforms mechanical vibration of a rigid diaphragm due to an acoustical pressure to a flow of electrical charge that can be converted to a useful voltage signal using a suitable readout circuit. In the mechanical domain, the sensitivity of the acoustical sensor can be defined as the maximum deflection of the diaphragm per unit of acoustical pressure \( S_M \). In the electrical domain,
this transforms into maximum charge flow due to the capacitance change per unit deflection \((S_E)\). This charge flow can be described in terms of a fraction of the bias voltage. Thus, the total open loop sensitivity of the acoustical sensor is the product of both the electrical and mechanical sensitivity, i.e., \(S = S_E S_M\) \([32]\). Optimization of the sensitivity regarding bias voltage, airgap thickness, material, and fabrication process is the main design objective.

2.1.11 Sensor Self Noise

The source of noise for the sensor structure is mainly due to mechanical–thermal noise resulting from molecular agitation. Since the change of capacitance due to the external acoustical pressure generates a very low level signal (of the order of a few millivolts), the mechanical–thermal noise becomes the main limiting noise component. This mechanical-thermal noise is caused by the well-known Brownian motion of the molecules and is analogous to the Johnson noise in the CMOS electronic circuits \([12]\). The mechanical-thermal noise is directly proportional to the square root of the mechanical resistance formed by a series combination of the airgap and the backplate acoustical ports resistances. However, the mechanical resistance is in inverse square relationship with the sensor’s diaphragm area. Thus, a decrease in the diaphragm area will result in a higher mechanical-thermal noise. Typical A-weighted noise values for MEMS-based capacitive sensors are in the range of 22-36 dB(A) \([5]\) \([6]\).
2.1.12 Total Harmonic Distortion

Harmonic distortion in transducers is in general caused by the nonlinearities always present in the devices due to the choice of transduction principle, device operational mechanism and the uncertainty associated with the device fabrication processes [33]. For MEMS-based capacitive sensors, the total harmonic distortion is mainly caused by both the inverse relation between the sensor capacitance and the deflection of the diaphragm, as well as the nonlinear electrostatic forces generated by the applied DC bias voltage [33]. If the selected bias voltage is too close to the pull-in voltage, this becomes the main source of distortion. Secondly, the dynamic deflection of the diaphragm causes a dynamic change of the electric field between the diaphragm and the backplate leading to an asymmetric dynamic response. Thus, it is desirable to choose a DC bias voltage considerably lower than the pull-in voltage associated with the structure and to reduce the uncertainty associated with fabrication processes as much as possible.

2.1.13 Sensor Dynamic Range

The dynamic range of an acoustical sensor is defined as the acoustical pressure range bounded by the minimum detectable acoustical pressure level and the maximum level of acoustical pressure the sensor structure can withstand before the diaphragm collapses. The minimum detectable acoustical pressure is constrained by the sensor’s self-noise. Near pull-in, the total harmonic distortion increases due to an increase in the nonlinearities. Thus, the upper limit of
sensor's dynamic range is determined by the maximum pressure level up to which the sensor can produce a distortion less output signal.

2.1.14 Device Failure

The predominant failure mode for a thin clamped diaphragm is due to fracture from excessive dynamic and thermal stresses. The fracture is either from brittle failure or fatigue, with brittle failure causing ruptures being the more common for a silicon-based device while a metal structure would be more susceptible to fatigue [34]. These forces may also impart a permanent distortion to the shape of the membrane or bending if the distortion exceeds the elastic limits of the material. Another reason for minimizing the deflection is that the membrane would no longer behave linearly at large displacements. Fracturing is worse when internal residual stresses are high, causing it to separate or delaminate from the substrate material. Delamination also results from differences in thermal expansion coefficients between the membrane and substrate materials, particularly worse for multilayer multi-material membranes. The stress should be released in the fabrication process.

Particulate contamination of membranes from flaked materials is a serious concern, especially for an ear canal application, since they would affect the output characteristics of the device or even can puncture the membrane. Depending on the dielectric properties of the membrane material, it may also be affected by electromagnetic or electrostatic fields through its induced internal fields. The field forces may produce temporary distortions which inhibit device
performance. Non-magnetic materials should be used if the device is being used in the presence of stray fields. The device can be tested for electromagnetic compatibility to ensure proper operations [34].

For reliable operation, it is thus necessary to ensure that the deformation of the diaphragm under normal operating conditions due to the combined effect of the electrostatic force and the external acoustical pressure is always within the elastic limit of the diaphragm material. If the diaphragm is made of a ductile material, like aluminum, the von Mises failure criteria is to be used to ensure an elastic deformation. For a brittle material like, polysilicon, Coulomb-Mohr criteria should be used [35]. Wear of the vibrational characteristics of the sensor diaphragm while operating within the elastic limit is negligible as the vibrational amplitude is generally much smaller than the lateral dimensions of the diaphragm.

2.1.15 Power Consumption

A low-resistivity diaphragm material would result in a lower voltage drop and thus, desirable for an application like hearing instrument where the battery life is crucial. Recent research works has identified that the resistivity of a thin film material also depends on the residual stress [36]. A higher value of residual stress results in a higher value of resistivity. Thus, selection of a low residual stress diaphragm can lead to a lower resistivity. Besides, ion implantation by phosphorous or boron and high temperature annealing also help to reduce the resistivity [37].
2.2 Constraints Associated with Hearing Instrument Application

It is desirable to design the microarray for use in a completely-in-the-canal (CIC) hearing instrument. The average adult ear canal has an approximate diameter of about 8.0 mm. Allowing for a clearance space of 1.2 mm around for ear-mold packaging and airflow purposes, the maximum available area for a planar microarray is about 4.6x4.6 mm². A consideration of the microarray geometry must take into account, the operating environment, the type of sensors, inter-element spacing, maximizing the active sensor area, interfacing and interconnectivity concerns, together with MEMS fabrication process constraints. The array can be square, rectangular, logarithmic, ring or of some other suitable geometry depending on the type of application. A square planar array of identically sized sensor elements with uniform spacing appears to be a good choice for a hearing instrument application so that maximum utilization of the available space in the ear canal is ensured.

A capacitive-type acoustical sensor with a clamped square diaphragm can have a diaphragm area of approximately 1.2 mm by 1.2 mm. Following [29], a MEMS capacitive sensor having a square diaphragm of area 1.2 x 1.2 mm² can yield a sensitivity of about 11 mV/Pascal at 1 kHz when used in conjunction with a proper readout circuit. Contact pads for biasing and interconnection can have a dimension of 75 x 75 μm² following the International Technology Roadmap for Semiconductors (ITRS), 1999 edition [38], and typical dimensions of wafer-through-hole aluminum-via-interconnects are 25x25 μm². Thus, drawing the
contacts pads at the bottom of the array die, using the wafer-through-hole aluminum-via-interconnects can facilitate use of a larger sensing area. A space of 250 μm at the die edges and between the adjacent sensor elements is necessary to facilitate die handling and packaging, and to ensure electrical isolation of routing traces and fabrication requirements. These requirements and constraints lead to the adoption of a 3x3 planar array of capacitive-type sensors as the initial design target for the array structure.

It is now necessary to investigate if these physical constraints related to the MEMS implementation and the target array geometry can be successfully mapped into the requirements of a beamforming technique to provide the desired broadband dynamically variable directional sensitivity for a desired audio frequency range.

A speaker tracking capability can also be incorporated in the array functionality by realizing a scanning beam with appropriate delay specifications. The main beam can be focused to a particular direction to acquire speech while the scanning beam can scan the broadside region for other potential speech sources. It is necessary to have a real-time digital beamsteering engine and associated software in order to use a microarray for this purpose.

2.3 Microarray Beamforming Model Development

Beamforming is another name for spatial filtering where an array of transducers- linear, rectangular, and circular or of some other arbitrary geometry together with appropriate signal processing can either direct or block the
radiation or the reception of signals in specified directions [39]. Due to the reciprocity property, acoustical transducers constructed to have a thin diaphragm can be used, either to receive or radiate acoustical energy. The acoustical energy when arrive at an arrayed group of sensors in the form of a plane wave, the sensor outputs differ from sensor to sensor due to the different distances the wave front must propagate to reach an individual sensor. In the case of a narrowband signal, these differences are manifested in the phase variations of the carrier signal.

Figure 2-1. A linear array of acoustical sensors. The signal arriving at different sensor element differs by a phase angle. The arrow direction indicates the look angle

Figure 2-1 illustrates the effect of a linear equidistance sensor geometry on the phase of the sensor output. Signals received at the adjacent sensors travel a difference in distance of $d \cos \theta$ which corresponds to a phase difference of $\frac{\omega}{cd \cos \theta}$ where $\omega$ is signal angular frequency in radians/s and $c$ is the signal propagation velocity. The quantity $\frac{\omega}{c}$ equals the wave number $k$, expressed
as \(2\pi / \lambda\). Therefore, the phase difference between two elements is \(-nkd \cos \theta\) where \(nd\) is the distance between the two elements where \(n\) is an integer. The vector 
\[
d(\theta, \omega) = \begin{bmatrix}
1 & e^{i(1d \cos \theta)} & e^{i(2d \cos \theta)} & \cdots & e^{i(N-1)d \cos \theta}
\end{bmatrix}
\]
describes the complex phase difference of a common signal at each of the sensors in an \(N\) element array. The array response or the array factor for a linear array as shown in Figure 2-1 is expressed as [39]:

\[
AF(\theta) = \sum_{n=0}^{N-1} e^{jnd \cos \theta}
\]

which is simply the sum of the elements in \(d(\theta, \omega)\). The main idea is to add up the signals received by individual sensor elements in the array from some particular direction of interest by applying an appropriate time delay to the output of each sensor element so that the outputs can be added cophasically. The time delay factor alters the phase of the received signal of each sensor element in the array so that their phases coincide with that of the output of the reference sensor element. This technique is known as the classical delay-and-sum beamforming. Another method of beamforming is called adaptive post filtering [2] where a beam of the required spatial dimension focused to a particular direction is formed by adaptively canceling the signals arriving from other directions by applying the techniques of constraint optimization [39]. It was reported that adaptive filtering technique isn’t much effective if the environment is associated with background noise and multipath distortion [3].
The array factor for a two-dimensional planar rectangular array can be expressed using a similar manner as described above. The normalized array factor, \( AF(\theta, \phi) \), of such an array incident to a plane wave at an angle \((\theta, \phi)\) can be approximated as [40]:

\[
AF(\theta, \phi) = \frac{\sin \left( \frac{M}{2} \psi_x \right)}{\frac{M}{2} \psi_x} \frac{\sin \left( \frac{N}{2} \psi_y \right)}{\frac{N}{2} \psi_y}
\]  
(2-3)

where \(M\) and \(N\) are the number of array elements along the \(x\)-axis and the \(y\)-axis, respectively, as shown in Figure 2-1. It is assumed that the array elements are equally spaced apart and all the sensor elements have identical characteristics. The parameters:

\[
\psi_x = \kappa d_x \sin \theta \cos \phi + \beta_x \]  
(2-4a)

\[
\psi_y = \kappa d_y \sin \theta \sin \phi + \beta_y \]  
(2-4b)

represent the amount of time delay applied to the output of each array element along the \(x\)-axis and \(y\)-axis respectively so that the outputs from all the array elements sum cophasically. The quantities \(d_x\) and \(d_y\) refer to the inter-element spacing along the \(x\)-axis and \(y\)-axis, respectively. The values \(\beta_x\) and \(\beta_y\) are the progressive phase shifts that must be applied to the output of each array element to steer the beam to a particular direction as specified by an angle \((\theta = \theta_0)\) and \((\phi = \phi_0)\). They are computed according to:
Figure 2-2. A rectangular array of acoustical sensors. An acoustical wave is incident to the array at an angle \((\theta, \phi)\)

\[
\beta_x = -kd_x \sin \theta_0 \cos \phi_0 \tag{2-5a}
\]

\[
\beta_y = -kd_y \sin \theta_0 \sin \phi_0 \tag{2-5b}
\]

To avoid spatial aliasing at all steering angles, the inter-element spacing \(d_x\) or \(d_y\) is required to be:

\[
d_x \leq \frac{\pi c}{\omega} = \frac{\pi c}{2\pi f} = \frac{\lambda}{2} \tag{2-6a}
\]

\[
d_y \leq \frac{\pi c}{\omega} = \frac{\pi c}{2\pi f} = \frac{\lambda}{2} \tag{2-6b}
\]
where \( \lambda \) is the wavelength and \( f \) is the frequency of the incident acoustical signal. Equation (2-6) specifies the Nyquist rate equivalent for spatial sampling [41].

Using equation (2-6), a sensor array requires an inter-element spacing of about 17 cm to form a beam at a signal frequency of 1000 Hz. Due to the constraints outlined in section 2.1 and 2.2, the inter-element spacing in a MEMS-realized array will be much smaller than what is required to avoid spatial aliasing. This means that a MEMS-based implementation of acoustical sensor microarray will have to be used in conjunction with an external digital realization of a beamsteering engine.

As \( d_x \) or \( d_y \) contributes to a time delay for the output of each element in the sensor array, equation (2-4) can be modified to incorporate a time delay that compensates for the difference in the time delay due to the physical array element spacing and what is required to avoid spatial aliasing. This compensatory time delay can be realized electronically, as if the array elements are being separated electronically to a distance that satisfies the Nyquist rate equivalent of spatial sampling. Equations (2-4) and (2-5), can thus be rewritten as:

\[
\psi_x = k d_{x} \sin \theta \cos \phi + k d_{xc} \sin \theta \cos \phi + \beta_x \tag{2-7a}
\]

\[
\psi_y = k d_{y} \sin \theta \sin \phi + k d_{yc} \sin \theta \sin \phi + \beta_y \tag{2-7b}
\]

and
\[ \beta_s = -(kd_{xs} \sin \theta_0 \cos \phi_0 + kd_{xc} \sin \theta_0 \cos \phi_0) \]  

\[ \beta_y = -(kd_{ys} \sin \theta_0 \sin \phi_0 + kd_{yc} \sin \theta_0 \sin \phi_0) \]  

where the expressions containing the \( d_{xs} \) and \( d_{ys} \) terms represent the delay due to physical array element spacing and the expressions containing the \( d_{xc} \) and \( d_{yc} \) terms represent the additional delay necessary to prevent spatial aliasing that will be realized in terms of an electronic time delay using an external processor and digital signal processing algorithms.

The half-power beamwidth of the sensor array is inversely proportional to the frequency of the incident signal. For a hearing instrument application, a constant beamwidth is desirable over the specified audio frequency range. Several constant beamwidth methods have been proposed in the literature [41]–[44]. An approach proposed in [42] has been adopted for this MEMS acoustical sensor array design, with a modification that incorporates the compensatory time delay factor. The method consists of utilizing \( 2r+1 \) delay elements in parallel to provide the overall delay for each sensor element.

One of the delay elements can be considered to define the direction of the main axis of the desired beam. The remaining \( 2r \) delay elements are used in pairs to provide positive and negative delays with respect to the main axis delay element to symmetrically broaden the beam width about the main axis. As each of the parallel delays can be adjusted to correspond to a slightly different spatial positioning of the beam, it is possible to effectively superimpose all the spatial
shifted beams to form one composite beam with the desired beam geometry. In
the resulting method, the beamwidth is kept constant over a frequency range with
a high frequency to low-frequency ratio quantized to equal to \(2r+1\). Since the
beam width at lower frequencies is wider, the symmetrical delays about the main
axis do not reshape the beam significantly. Thus in practice a number of high
frequency beams will be deflected to form a composite beam shape similar to
that obtained at the low frequencies. Applying this technique, the composite
beam pattern can be deflected from its main axis by an angle \(D_x\) or \(D_y\) as
expressed in the following equation (2-9):

\[
D_x = \left( \frac{2(d_{xr} + d_{xc})}{\lambda} - 1 \right) \frac{\pi}{2r} \tag{2-9a}
\]

\[
D_y = \left( \frac{2(d_{yr} + d_{yc})}{\lambda} - 1 \right) \frac{\pi}{2r} \tag{2-9b}
\]

The effect of beam superimposing is shown in Figure 2-3. Weighting gain
factors \(Wf_x\) and \(Wf_y\), are used to control the signal amplitude at the output of the
\(2r\) delay elements to adjust the beam length at the corresponding spatial
direction as given in equation (2-10).

\[
Wf_x = \frac{1}{\sqrt{2}} \frac{\sin \left( \frac{D_x}{2r} \right)}{\pi} \tag{2-10a}
\]

\[
Wf_y = \frac{1}{\sqrt{2}} \frac{\sin \left( \frac{D_y}{2r} \right)}{\pi} \tag{2-10b}
\]
By defining

\[ \Psi_x = \psi_x + \beta_x \]  \hspace{1cm} (2-11a)

\[ \Psi_y = \psi_y + \beta_y \]  \hspace{1cm} (2-11b)

the array factor of the MEMS acoustical beamforming sensor array can now be expressed in its final form as:

\[ AF(\theta, \phi) = \sum_{m=-\infty}^{\infty} \left( 1 - mWf_x \right) \sum_{n=-\infty}^{\infty} \left( 1 - mWf_y \right) \sin\left( \frac{M}{2} \Psi_x - mD_x \right) \sin\left( \frac{N}{2} \Psi_y - mD_y \right) \]  \hspace{1cm} (2-12)

A beam can thus be formed with the microarray using digital signal processing algorithms that are implemented in real-time using the available digital hardware in the hearing instrument. A symmetrical microarray layout consisting of an odd number of sensor elements, such as 3x3, 5x5, etc. contributes to a simplified beamforming algorithm. An inter-element spacing of \( \lambda / 2 \) results in reduced power in the grating beams and it maximizes the main axis beam power. Figures 2-4 to 2-9 show such beams formed by using an array of 3x3 sensors in a planar arrangement for different steered angles.
Figure 2-3. Superimposed beam patterns showing broadband constant beamwidth beamforming.
Figure 2-4. Beam pattern of a 350 Hz beam, $r=4$, $\theta=0^\circ$, $\phi=90^\circ$
Figure 2-5. Beam pattern of a 3150 Hz beam, $r=4$, $\theta=0^\circ$, $\phi=90^\circ$
Figure 2-6. Beam pattern of a 50 Hz beam, $r=4$, $\theta=30^\circ$, $\phi=45^\circ$
Figure 2-7. Beam pattern of a 3150 Hz beam, \( r=4, \theta=30^\circ, \phi=45^\circ \)
Figure 2-8. Beam pattern of a 18020 Hz beam, $r=450$, $\theta=0^0$, $\phi=90^0$
Figure 2-9. Beam pattern of a 18020 Hz beam, $r=450$, $\theta=30^0$, $\phi=45^0$

2.4 System Block Diagram

A block diagram of the proposed system is shown in Figure 2-10. Highly efficient SoC IP cores are available for signal conditioning, $\Sigma-\Delta$ A/D converter, DSP processor and other microelectronics circuitry. A microcontroller can be programmed to realize the proposed beamforming engine.
Figure 2-10. Block diagram of the proposed beamforming acoustical sensor microarray showing the necessary MEMS and CMOS functional blocks. In the figure, color coding has been used to group blocks those are in a same functional domain.

2.5 Summary

In summary, a beamforming method has been developed for use in a MEMS realization of a square, planar acoustical sensor microarray. The method, based on the conventional delay-and-sum beamforming incorporates an electronically realizable time delay factor to satisfy the Nyquist rate of spatial sampling. Using the method, a reasonably constant beamwidth for a frequency range that very well covers the audio frequency range can be obtained while the constraints associated with the MEMS implementation and the target application, i.e., hearing instrument application are being satisfied. A block diaphragm of the overall system concept has been provided.
Chapter 3

Acoustical Sensor Element Design

In this chapter, the design methodology of an acoustical sensor element of the proposed microarray has been described. The sensitivity, harmonic distortion and the dynamic range of a voltage controlled MEMS-based capacitive-type acoustical sensor depend directly on the bias voltage. The chosen bias voltage must be well below the pull-in voltage related to the sensor structure. There is no definitive analytical model available in existing literature to accurately evaluate the pull-in voltage related to a voltage controlled MEMS-based capacitive-type acoustical sensor having a clamped square diaphragm. In this chapter, a simple, easy to use analytical model to evaluate the pull-in voltage associated with a clamped square diaphragm under electrostatic load has been developed. The approach is based on a linearized uniform approximate model of the electrostatic pressure and a 2-D load-deflection model of a square diaphragm under uniform pressure. The model has been verified by three-dimensional electromechanical finite element analysis and also by comparing the results with published experimental results of similar structures. Relevant mathematical models governing sensitivity, bias voltage, capacitance, load-deflection characteristics, mechanical impedance, stress, and noise performance of a capacitive-type acoustical sensor are presented. The models lead to an
integrated design strategy to optimize the electrical and mechanical design variables to satisfy the design requirements.

3.1 Operating Principle

The basic structure of a MEMS-based capacitive-type acoustical sensor is shown in Figure 3-1. The structure can be viewed as a parallel plate capacitor consisting of a top diaphragm and a bottom backplate separated by a small airgap acting as the dielectric material. When an acoustical wave is incident on the diaphragm, it causes the diaphragm to deflect and the airgap between the diaphragm and the backplate decreases, causing an increase in the capacitance between them. As the diaphragm vibrates in accordance with the frequency of the acoustical wave, the capacitance between the electrodes keep changing accordingly due to a variable airgap. If a battery is connected across the diaphragm and the backplate, following the principle of energy conservation, electrical charge will flow to and away from the battery in accordance with the diaphragm vibration. By connecting to a suitable charge flow (current) sensing electrical circuit to the system a usable voltage signal representation of the incident acoustical wave can be obtained [28].

However, while the supply, or the bias voltage provides a means for readout of the change in capacitance due to diaphragm deflection, the electrostatic attraction force associated with the bias voltage pulls the capacitor electrodes towards each other and causes the diaphragm to deflect, even in the absence of an external mechanical pressure. This electrostatic attraction force is nonlinear
Figure 3-1. A conceptual cross-section of a MEMS-based capacitive-type acoustical sensor

and increases with the decreasing airgap between the electrodes for a given bias voltage. Furthermore, since the diaphragm is clamped, the deflection at the central region of the diaphragm is greater than that at the diaphragm edges. Thus, a non-uniform pressure profile is developed. In addition, the nonlinearity of the electrostatic attraction force causes a shift of the fundamental resonant frequency of the structure, an effect known as spring softening [31] [45].

During operation, the capacitor structure is subjected to four different kinds of forces: the mechanical input (acoustical pressure), the elastic force generated in the vibrating diaphragm in response to the deformation, the damping force generated by the airgap, and the electrostatic attraction force due to the bias voltage. In equilibrium, the damping force can be neglected. Thus, the perturbing force acting on the diaphragm is the sum of the electrostatic and the external mechanical pressure and is counterbalanced by the elastic force developed in the diaphragm due to its deformation.

While having no external pressure, the electrostatic attraction force associated with the bias voltage causes a deformation of the diaphragm resulting
in a change of the device capacitance. Consequently, charges flow in the external electrical circuit, and an offset error occurs [9]. Furthermore, this initial diaphragm deformation reduces the airgap thickness that in turn reduces the sensor’s dynamic range.

Therefore, it is desirable to minimize the effect of the electrostatic force as much as possible. Careful determination of an optimum operating point for the supply (bias) voltage is necessary so that:

1. The device does not collapse due to pull-in,
2. Sufficient charge flow can be established for the chosen readout circuitry,
3. The spring softening effect does not modify the fundamental resonant frequency of the structure below the desired upper cut-off frequency, and
4. The maximum allowable deformation due to combined electrostatic and mechanical forces is within the elastic limit of the diaphragm material.

As the sensitivity, frequency response, load-deflection characteristics, noise performance, and harmonic distortion of a capacitive-type acoustical sensor depend critically on the bias voltage, it is necessary to optimize the bias voltage, considering the available geometry and fabrication materials, to ensure safe operation.

The nonlinear and non-uniform nature of the electrostatic force makes it difficult to determine the pull-in voltage for a square diaphragm case and the
exact analytical solution is still unknown [46]. The commonly used parallel-plate approximation method of pull-in voltage determination introduces significant errors (~20%) if the diaphragm is fully clamped [10]. 3-D finite element electromechanical analysis or finite difference methods are computationally highly expensive. In [10], simple and fast empirical solutions are provided to determine the pull-in voltage for cantilever beams, fixed-fixed beams and circular diaphragms with excellent accuracies. However, published analytical models to determine the pull-in voltage for a square diaphragm case, predict pull-in voltages that show significant error when compared with finite element analysis results or experimentally measured values [29], [47]. In the following sections, an analytical method is developed to determine the pull-in voltage for a clamped square diaphragm case.

3.2 First-order Analysis (Parallel Plate Approximation)

A parallel plate approximation is considered first to highlight the major aspects of the analysis. In this analysis, any fringe field capacitance associated with the capacitor electrodes is neglected and the capacitor electrodes and contacts are assumed to be perfect. It is assumed that the capacitor structure is situated in a vacuum environment to ensure zero external mechanical loading of the top electrode. It is also assumed that the diaphragm's restoring force (spring force) is a linear function of its displacement. A lumped element model of a movable plate capacitor is shown in Figure 3–2a and an equivalent circuit of the lumped element model is shown in Figure 3–2b. Neglecting any damping within
the system (as the structure is assumed to be in vacuum), the equation of motion of the movable plate due to an electrostatic attraction force \( F_E \) caused by a constant supply voltage \( V \) can be expressed as:

\[
M \frac{d^2 z}{dt^2} + Kz = F_E
\]

(3-1)

where \( M, K \), and \( z \) represents the mass, spring constant, and the displacement, respectively. The mechanical elastic force \( F_M \) can be expressed as

\[
F_M = Kz
\]

(3-2)

where the variation of \( K \) is assumed to be linear.

The electrostatic attraction force \( F_E \) between the plates due to the charges on the plates can be found by differentiating the stored energy of the capacitor with respect to the position of the movable plate and is expressed as:

\[
F_E = -\frac{d}{dz} \left( \frac{1}{2} CV^2 \right) = \frac{\varepsilon_0 AV^2}{2(d_0 - z)^2}
\]

(3-3)

where \( \varepsilon_0 \) is the permittivity of the free space, \( C \) is the capacitance, \( A \) is the area of a capacitor plate and \( d_0 \) is the initial thickness of the airgap. Since at static equilibrium, \( F_M = F_E \), we have:

\[
Kz = \frac{\varepsilon_0 AV^2}{2(d_0 - z)^2}
\]

(3-4)
Figure 3-2. (a) Lumped parameter model of a parallel plate capacitive transducer, (b) Equivalent circuit of the lumped parameter model

The equation (3-4) can be rearranged into a third-order polynomial in $z$. After solving for $z$ and choosing the stable root, the pull-in voltage can be expressed as [48]:

$$V_{pl} = \frac{\sqrt{8Kd_0^3}}{27\varepsilon_0A} \quad (3-5)$$

The distance where the pull-in occurs is:

$$z_{pl} = \frac{d_0}{3} \quad (3-6)$$

and the pull-in airgap is:
\[ d_{pi} = \frac{2d_0}{3} \]  

(3-7)

The spring constant of the diaphragm is given by:

\[ K = \frac{27\varepsilon_0 AV_{pi}^2}{8d_0^3} \]  

(3-8)

If the voltage is increased beyond this pull-in voltage, the resulting electrostatic force will overcome the elastic restoring force, and will cause the movable plate to collapse on the fixed plate and the capacitor will be short-circuited.

By expanding (3-3) using a Taylor series approximation about a nominal distance \( z_0 \) [31], one obtains:

\[ F_E = \frac{\varepsilon_0 AV^2}{2(d_0 - z)^2} = \frac{\varepsilon_0 AV^2}{2(d_0 - z)^2} \bigg|_{z=z_0} + \frac{\varepsilon_0 AV^2(-2)(-1)}{2(d_0 - z)^3} \bigg|_{z=z_0} (z - z_0) + ... \]  

(3-9)

After rearranging the terms:

\[ F_E = \frac{\varepsilon_0 AV^2}{2(d_0 - z_0)^2} \left[ 1 + 2 \frac{z - z_0}{d_0 - z_0} + ... \right] \]  

(3-10)

Substituting \( F_E \) from (3-1) in (3-10), one obtains:

\[ M \frac{d^2 z}{dt^2} + Kz = \frac{\varepsilon_0 AV^2}{2(d_0 - z_0)^2} \left[ 1 + 2 \frac{z - z_0}{d_0 - z_0} + ... \right] \]  

(3-11)

After rearrangement:
\[ M \frac{d^2 z}{dt^2} + \left( K - \frac{\varepsilon_0 AV^2}{(d_0 - z_0)^3} \right) z = \frac{\varepsilon_0 AV^2}{2(d_0 - z_0)^2} \left[ 1 - 2 \frac{z_0}{d_0 - z_0} + \ldots \right] \] \hspace{1cm} (3-12)

Thus, the electrostatic attraction force effectively modifies the spring constant of the movable plate and the term within parenthesis in the left hand side of (3-12) represents the effective spring constant at a specified voltage. The amount of modification is termed as spring softening and can be expressed as:

\[ K_{\text{soft}} = \frac{\varepsilon_0 AV^2}{(d_0 - z_0)^3} \] \hspace{1cm} (3-13)

Consequently, the resonant frequency of the structure is shifted from:

\[ \omega_{\text{res}} = \sqrt{\frac{K}{M}} \] \hspace{1cm} (3-14)

to:

\[ \omega_{\text{res}} = \sqrt{\frac{1}{M} \left( K - K_{\text{soft}} \right)} \] \hspace{1cm} (3-15)

For an acoustical sensor, the resonant frequency of the sensor structure must be well above the upper cut-off frequency of the desired acoustical frequency range.

Thus, for an acoustical sensor with a clamped diaphragm, the chosen bias voltage must not soften the spring constant of the diaphragm so much that the altered resonant frequency of the structure falls below the upper cut-off frequency of the desired frequency range.
3.3 Square Diaphragm Load-Deflection Characteristics

Due to the presence of residual stress and a significantly large deflection of the diaphragm compared to its thickness, the developed strain energy in the middle of the diaphragm causes a stretch of the diaphragm middle surface. Consequently, the deflection of the diaphragm middle surface no longer depends solely on the external forces and the rigidity of the diaphragm increases with the deflection [49]. This deflection dependent nonlinear behavior of a rigidly clamped diaphragm is known as spring hardening and a large deflection model of analysis must be applied to determine the deflection. Following the large deflection model, for a rigidly clamped square diaphragm with built in residual stress, the deflection of the midpoint of the diaphragm under a uniform pressure load $P$ can be expressed as [50]:

$$P(h_0) = C_{1M} \frac{t_d \sigma}{b^2} h_0 + C_{2M} (\nu) \frac{t_d E}{b^4} h_0^3$$

(3-16)

where $P$ is the applied uniform pressure, $t_d$, the diaphragm thickness, $E$, Young's modulus of the diaphragm material, $\nu$, the in-plane Poisson's ratio, $\sigma$, the residual stress, $b$, half of the diaphragm side length and $h_0$, represents the deflection of the diaphragm midpoint. The quantities, $C_{1M}$ and $C_{2M}$ are numerical fitting parameters and their values are given by:

$$C_{1M} = 3.45, \quad \text{and}$$

$$C_{2M} = 1.994(1-0.271\nu)/(1-\nu)$$

(3-17)
The deflection of the diaphragm from mid-side to mid-side can be calculated from the midpoint deflection as:

$$h(x, 0) = h_0 \left(1 + 0.401 \frac{x^2}{b^2}\right) \cos \left(\frac{\pi x}{2b}\right) \tag{3-18}$$

and diagonal deflection can be calculated similarly as:

$$h(x = y) = h_0 \left(1 + 0.401 \left(\frac{2x^2}{b^2} + 1.1611 \frac{x^4}{b^4}\right) \cos^2 \left(\frac{\pi x}{2b}\right)\right) \tag{3-19}$$

In [10], it was shown that for clamped diaphragms, a fringe field correction is necessary for the Young's modulus as given by:

$$\hat{E} = E (1 - v^2) \tag{3-20}$$

where $\hat{E}$ is the effective Young's modulus. This fringe field corrected Young's modulus thus, is necessary to incorporate in the load-deflection equation (3-16) to yield:

$$P(h_0) = C_{1M} \frac{t_d \sigma}{b^2} h_0 + C_{2M} (v) \frac{t_d \hat{E}}{b^4} h_0^2 \tag{3-21}$$

The nonlinear spring constant can be extracted from (3-21) as

$$K_{\text{nonlinear}} = \frac{P(h_0)}{h_0} = C_{1M} \frac{t_d \sigma}{b^2} + C_{2M} (v) \frac{t_d \hat{E}}{b^4} h_0^2 \tag{3-22}$$

The first term in the right hand side of (3-22) has the same form as the lumped element spring constant except a slightly different value for the numerical
constant $C_{1M}$ and the second term in the right hand side of (3-22) captures the deflection dependent nonlinearity due to spring hardening as it contains the square of the midpoint deflection variable $h_0$. A plot of $K_{\text{nonlinear}}$ vs. $h_0$ is shown in Figure 3-3 for different test device parameter values as are listed in Table 1.

### Table 3-1. Test device parameters

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Diaphragm thickness, $t_d$</td>
<td>0.8</td>
<td>μm</td>
</tr>
<tr>
<td>Diaphragm side length, $a$</td>
<td>1.2</td>
<td>mm</td>
</tr>
<tr>
<td>Airgap thickness, $d_0$</td>
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<td>μm</td>
</tr>
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<td>Young's modulus, $E$</td>
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<td>GPa</td>
</tr>
<tr>
<td>Poisson's ratio, $\nu$</td>
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<td>-</td>
</tr>
<tr>
<td>Residual stress, $\sigma$</td>
<td>20</td>
<td>MPa</td>
</tr>
</tbody>
</table>
Figure 3-3. Spring hardening resulting from deflection of a square diaphragm due to an applied uniform pressure
3.4 Square Diaphragm Pull-in Voltage: A New Analytical Model

The analysis carried out in Section 3.2 for a parallel plate capacitor structure can now be extended to the case of a rigidly clamped square diaphragm separated from a rigid backplate by a small airgap as shown in Figure 3-1. The deflection of the diaphragm is due to the resultant effect of the electrostatic, external acoustical, restoring elastic and air damping forces acting simultaneously.

At equilibrium, the air damping force can be neglected. For a parallel plate configuration, the nonlinear electrostatic force is always uniform. However, for a rigidly clamped diaphragm case, the electrostatic force becomes non-uniform due to a cosine like deformation profile of the diaphragm as is shown in Figure 3-4. This non-uniformity results in a lower deflection of the midpoint of the diaphragm. Thus, to evaluate the deflection of a rigidly clamped diaphragm under electrostatic force, it is necessary to obtain a uniform, linear model of the electrostatic force that can be applied in the load-deflection equation (3-21). A uniform, linearized model of the electrostatic force can be obtained from equation (3-12) by linearizing the electrostatic force about the zero deflection point, i.e. \( z_0 = 0 \), as shown in Figure 3-5.

Since, prior to any deflection the diaphragm is flat \( (z_0 = 0) \), the parallel plate approximation can then easily be applied without any significant error if the airgap thickness is very small compared to the lateral dimensions of the diaphragm.
Figure 3-4. Non-uniformity of the electrostatic pressure for a clamped diaphragm under electrostatic load. (a) Top view of a rigidly clamped diaphragm. (b) Non-uniformity of the electrostatic force arises due to clamped nature of the diaphragm.
Figure 3-5. Linearization of the electrostatic force about zero displacement

Linearizing (3-12) about the point, \( z_0 = 0 \), one obtains:

\[
M \frac{d^2 z}{dt^2} + \left( K - \frac{\varepsilon_0 AV^2}{d_0^3} \right) z = \frac{\varepsilon_0 AV^2}{2d_0^2} \tag{3-23}
\]

Rearranging (3-23) and neglecting the time dependent term, one obtains:

\[
\frac{\varepsilon_0 AV^2}{2d_0^2} + \frac{\varepsilon_0 AV^2}{d_0^3} z = Kz \tag{3-24}
\]

Left hand side of (3-24) equals to an approximate, uniform, and linear electrostatic force and the effective linearized uniform electrostatic pressure on the diaphragm can be evaluated from (3-24) as:

\[
P_{\text{eff}} = \varepsilon_0 V^2 \left( \frac{1}{2d_0^2} + \frac{z}{d_0^3} \right) \tag{3-25}
\]

Substituting \( z \) in (3-25) by the pull-in deflection from (3-6), the effective pull-in pressure \( P_{\text{eff, PI}} \) can be evaluated as:
\[ P_{\text{eff-PI}} = \frac{5}{6} \frac{\varepsilon_0 V_{pl}^2}{d_0^2} \]  

(3-26)

where \( V_{pl} \) represents the pull-in voltage. Next, by substituting the pull-in deflection \( \frac{1}{3} d_0 \) for \( h_0 \), and replacing \( P(h_0) \) by \( P_{\text{eff-PI}} \), in (3-26), we obtain:

\[ \frac{5}{6} \frac{\varepsilon_0 V_{pl}^2}{d_0^2} = C_{1M} \frac{t_d \sigma}{b^2} \left( \frac{d_0}{3} \right) + C_{2M} (\nu) \frac{t_d \hat{E}}{b^4} \left( \frac{d_0}{3} \right)^3 \]  

(3-27)

The above equation can now be solved for the pull-in voltage, \( V_{pl} \), as:

\[ V_{pl} = \left[ \frac{6d_0^2}{5\varepsilon_0} \left[ C_{1M} \frac{t_d \sigma}{b^2} \left( \frac{d_0}{3} \right) + C_{2M} (\nu) \frac{t_d \hat{E}}{b^4} \left( \frac{d_0}{3} \right)^3 \right] \right]^{\frac{1}{2}} \]  

(3-28)

Expression (3-28) provides the desired approximation of the pull-in voltage for a clamped square diaphragm under electrostatic pressure.

### 3.5 Model Validation

#### 3.5.1 Illustrative Example

To illustrate the above model of pull-in voltage evaluation, an acoustical sensor structure having device parameters as given in Table 3-1 has been used.

The left hand side of (3-24) is plotted in Figure 3-6 for a voltage range of 11 to 17.45 volts. Superimposed in the Figure 3-6 is a plot of the right hand side of (3-24) using the nonlinear spring constant \( K_{\text{nonlinear}} \) as expressed in (3-22). At a
distance of one-third of the airgap (1.167 \mu m), the $K_z$ graph intersects the 17.45 volts constant voltage curve and thus gives the voltage where the pull-in occurs.

The intersection of the $K_z$ graph with the 12 volts constant voltage curve shows the stable equilibrium point at that voltage. The diaphragm deflection at that point is about 0.41 \mu m. The pull-in voltage calculated using (3-28) is 17.453 volts and this is in close agreement with Figure 3-6. The value of pull-in voltage calculated using equation (3-28) is about 2.45 volts higher than that is calculated using (3-5).

The mid-side to mid-side deflection profiles of the diaphragm for different bias voltages is calculated using (3-18) and (3-21), and are plotted in Figure 3-7.

Results from 3-D electromechanical finite element analysis and the developed analytical model for the diaphragm deflection for different bias voltages are plotted in Figure 3-8. The FEA results show that the pull-in occurs at 17.85 volts and this is in close agreement with the analytical value. Figure 3-9 shows the 3-D electromechanical finite element analysis result of the diaphragm collapse and the Figure 3-10 shows a 3-D deflection profile of a square diaphragm calculated using the analytical models.
Figure 3-6. Electrostatic and elastic forces versus displacement using parameters given in Table 3-1
Figure 3-7. Mid-side to mid-side deflection profiles of a clamped diaphragm for different bias voltages
Figure 3-8. Comparison of diaphragm deflection calculated using the analytical model and FEA analysis for different bias voltages.
Figure 3-9. Finite element analysis results showing diaphragm collapse when the bias voltage exceeds the pull-in limit

Figure 3-10. Calculated diaphragm deflection following the equations (3-18), (3-19) and (3-21) for a bias voltage of 12 volts
3.5.2 Comparison with Other Reported Designs

In Table 3-2, a comparative result is provided of reported pull-in voltages for square diaphragms under electrostatic load with the results obtained using the developed analytical model. The maximum difference between the experimental value and the developed analytical model is 2.52%.

Table 3-2: Comparison of square diaphragm pull-in voltages

<table>
<thead>
<tr>
<th>Reference</th>
<th>Reported Pull-in Voltage (V)</th>
<th>Pull-in Voltage Evaluated Using the Developed Analytical Method (V)</th>
<th>Difference (%)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Osterberg [46] (Polymeric diaphragm)</td>
<td>45.25 (Experimental)</td>
<td>46.39</td>
<td>-2.52</td>
</tr>
<tr>
<td>Mastranengelo [29] (Polysilicon diaphragm)</td>
<td>19.90 (FEA)</td>
<td>19.46</td>
<td>2.25</td>
</tr>
<tr>
<td>Bergqvist [5] (Monocrystalline silicon diaphragm)</td>
<td>10.5 (Experimental)</td>
<td>10.75</td>
<td>-2.38</td>
</tr>
</tbody>
</table>

3.6 Circular Diaphragm Pull-in Voltage Evaluation

The analytical method developed in the preceding section to determine the pull-in voltage for a rigidly clamped square diaphragm can be adopted to evaluate the pull-in voltage for a circular diaphragm under electrostatic load.

Following [51], the deflection of a rigidly clamped circular diaphragm under uniform load can be expressed as:
\[ h(r_c) = \frac{P(h)a_c^4}{K_1^2 D} \left[ \frac{I_0(K_1 r_c/a_c) - I_0(K_1)}{2K_1 I_1(k)} + \frac{a_c^2 - r_c^2}{4a_c^2} \right] \]  

(3-29)

where, \( a_c \) is the diaphragm radius, \( r_c \) is the radial position, \( h(r_c) \) is the deflection at a radial position \( r_c \). \( I_0 \) and \( I_1 \) are the modified Bessel functions of first kind of zeroth and first order, respectively. \( P \) is the uniform pressure, \( t_d \) is the thickness of the diaphragm and the diaphragm rigidity \( D \) is expressed as:

\[ D = \frac{E t_d^2}{12(1-v^2)} \]  

(3-30)

The tension parameter \( K_1 \) is expressed as:

\[ K_1 = \frac{a_c}{t_d} \sqrt{\frac{12(1-v)^2 \sigma}{E}} \]  

(3-31)

At the center of the diaphragm, \( r_c = 0 \). Thus, the deflection of the center of the diaphragm can be obtained from equation (3-29) by substituting zero for the radial position \( r \) and a simplified expression can be given as:

\[ h_0 = \frac{P(h_0)a_c^4}{K_1^2 D} \left[ \frac{-I_0(K_1)}{2kI_1(K_1)} + 0.25 \right] \]  

(3-32)

where \( h_0 \) represents the deflection of the center of the diaphragm. Expression (3-32) can now be rearranged in the format of expression (3-16) to express the deflection of the center of the diaphragm as a function of applied pressure, \( P(h_0) \) as:
\[ P(h_0) = \frac{h_0 K_1^2 D}{a_c^4 \left[ -I_0(K_1) \right] + 0.25} \]  \hspace{1cm} (3-33)

Next, using the same method as for the square diaphragm case, we replace \( E \) in equations (3-30) and (3-31) by \( \hat{E} \) from (3-20), \( h_0 \) in (3-33) by the pull-in deflection \( \frac{1}{3} d_0 \), and substitute \( P_{eff-pl} \) from (3-26) for \( P(h_0) \) in (3-33), rearrange, and obtain the expression for the pull-in voltage as:

\[ V_{pl} = \sqrt{\frac{2d_0^4}{5\varepsilon_0} \frac{K_1^2 D}{a_c^4 \left[ -I_0(K_1) \right] + 0.25}} \]  \hspace{1cm} (3-34)

A comparison of pull-in voltages evaluated using expression (3-34) with the pull-in voltages obtained using the method provided in [10] is presented graphically in Figure 3-11 for a range (0.5 mm–2.5 mm) of diaphragm radius. For the diaphragm and the airgap thickness, Young’s modulus, Poisson’s ratio, and residual stress, the values that are listed in Table 3-1 are used. From Figure 3-11, it is evident that there is negligible difference (less than 1%) between the pull-in voltages evaluated using the new analytical method and those obtained using the method provided in [10]. As this comparison provided in Figure 3-11 validates the new method of pull-in voltage evaluation for a circular diaphragm, it also further validates the new method of pull-in voltage evaluation for square diaphragms as both the methods are derived using the same principle.
Figure 3-11. Comparison of pull-in voltage evaluated using new analytical method and the empirical method provided by Osterberg and Senturia for different diaphragm radii.
3.7 Model Limitations

It is evident that the new analytical method can provide very good approximation of pull-in voltage for the following limited cases:

1. Both the electrodes are required to be parallel prior to any electrostatic actuation.

2. The gap between the clamped diaphragm and the backplate should be small enough so that the Taylor series expansion about the zero deflection point doesn’t introduce any significant error.

3. The lateral dimensions of the diaphragm are required to be very large compared to the diaphragm’s thickness and the airgap.

3.8 Diaphragm Stress Calculation

Following [52], the maximum stress developed in the diaphragm under deflected condition is tensile and occurs at the middle of the edges. This tensile stress is the sum of the constant tensile stress due to stretching and bending stress at the middle of the edges and can be expressed as:

\[
\sigma_{\text{total}} = 0.29 \times \sqrt{\frac{P^2 a^2 \hat{E}}{t_d^2}} + 1.47 \times \sqrt{\frac{P^2 a^2 \hat{E}}{t_d^2}}
\]

where \( P \) is applied uniform pressure and \( a \) represents square diaphragm side length. The first term in the right hand side of (3-35) represents the tensile
stress in the middle of the diaphragm due to stretching and the second term represents the bending stress at the middle of the edges.

3.9 Sensitivity Analysis

A voltage controlled capacitive-type acoustical sensor can be viewed as a mechano-electric transformer that transforms mechanical vibration of a rigid diaphragm due to an acoustical pressure to a flow of electrical charge. In the mechanical domain, the sensor’s sensitivity can be defined as the maximum deflection of the diaphragm per unit of acoustical pressure \( S_M \) while in the electrical domain, this transforms into maximum charge flow due to capacitance change per unit deflection \( S_E \). Thus, the total open loop sensitivity, \( S \) is the product of both electrical and mechanical sensitivity, i.e., \( S = S_E S_M \).

Since it is desirable to evaluate the sensitivity of the sensor structure in terms of frequency, a method is described below that expresses sensitivity in terms of frequency.

The current, \( i(t) \), due to the flow of charge, \( Q(t) \), caused by capacitance change due to an external acoustical pressure can be expressed as:

\[
i(t) = \frac{dQ(t)}{dt} = \frac{d}{dt} (C(t)V) = C(t)\frac{dV}{dt} + V \frac{dC(t)}{dt}
\]  

(3-36)

Since, in a voltage controlled capacitive transducer \( V \) is constant, equation (3-36) reduces to:
\[ i(t) = V \frac{dC(t)}{dt} = V \frac{d}{dt} \left( \frac{\varepsilon_0 A}{d_0 - z(t)} \right) \]

\[ = V \varepsilon_0 A \left( \frac{d}{dz} \left( \frac{1}{d_0 - z(t)} \right) \right) \frac{dz(t)}{dt} \]

\[ = - \frac{V \varepsilon_0 A}{(d_0 - z(t))^2} \frac{dz(t)}{dt} = - \frac{V \varepsilon_0 A}{d_b^2} \ddot{v}(t) \]

or

\[ i(t) = - \frac{V \varepsilon_0 A}{d_b^2} \ddot{v}(t) \quad (3-38) \]

where \( d_b \) is the value of the airgap after applying the bias voltage \( V \) and \( \ddot{v}(t) \) is the velocity of the diaphragm due to acoustical pressure. The equation (3-38) establishes the important relationship between the mechanical domain velocity of the diaphragm to the electrical domain current. The quantity \( \varepsilon_0 AV_2 / d_b^2 \) can be expressed in terms of a transformation ratio \( n \). Thus:

\[ i(t) = -n \ddot{v}(t) \quad (3-39) \]

Based on this concept, a lumped element electromechanical equivalent model of the sensor structure is shown in Figure 3-12. In the Figure 3-12, \( Z_m \) is the mechanical impedance of the sensor structure, and \( Z_a \) represents
Figure 3-12. A lumped element Electro-mechanical equivalent model of the sensor structure

the acoustical impedance of the air in contact with the diaphragm. The derivations of the parameters $Z_m$ and $Z_a$ are available in [29]. The total impedance of the sensor while subjected to an acoustical pressure is then:

$$Z_i = Z_m + Z_a$$

(3-40)

Referring to Figure 3-12, expression (3-39) can be expanded as:

$$i(t) = -n\ddot{v}(t) = -\frac{nF(t)}{Z_t} = -\frac{nAP(t)}{Z_t}$$

(3-41)

or

$$\frac{i(t)}{P(t)} = \frac{VA^2e_0}{d_b^2Z_t} = -\frac{CAV}{d_bZ_t}$$

(3-42)

where $C$ is the sensor capacitance after applying the bias voltage. Expressing the radian frequency of the acoustical wave by $\omega$ and multiplying both sides of (3-42) by $1/j\omega$ one obtains:

$$\frac{i(t)}{j\omega CP(t)} = \frac{i(t)Z_C}{P(t)} = \frac{VA}{j\omega d_bZ_t}$$

(3-43)
\[ i(t)Z_C, \text{is the open circuit output voltage } V_0(t). \text{ Thus the sensitivity, } S, \text{ can}
\]

finally be expressed in the form:

\[ S = \frac{|V_0(t)|}{|P(t)|} = \frac{VA}{|j\omega d_z Z_t|} \quad (3-44) \]

Using (3-44) frequency response of the sensor can be obtained in terms of mechanical vibration of the diaphragm.

3.10 Sensor Mechanical Impedance

The dynamic behavior of the sensor can be calculated using an equivalent analog electrical circuit model [39] as given in Figure 3-13. The air radiative resistance is defined as \( R_r \), and the air mass is defined as \( M_r \), the diaphragm mass is \( M_m \) and its compliance is \( C_m \). The airgap and back-vent losses are represented by viscous resistances \( R_g \) and \( R_h \), respectively. The airgap compliance is given by \( C_a \). The mathematical models of the above parameters can be obtained from [29] and are listed in equations (3-45)-(3-54) in Table 3-4. Table 3-3 provides the list of symbols used in Table 3-4.
### Figure 3.13  Equivalent analog electrical circuit of a capacitive-type acoustical sensor

![Equivalent analog electrical circuit of a capacitive-type acoustical sensor](image)

### Table 3.3  Acoustical sensor element design variables [29]

<table>
<thead>
<tr>
<th>Physical Parameters</th>
<th>Symbol</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Diaphragm angular vibrational frequency</td>
<td>$\omega$</td>
<td>Rad/s</td>
</tr>
<tr>
<td>Square diaphragm side length</td>
<td>$a$</td>
<td>m</td>
</tr>
<tr>
<td>Diaphragm thickness</td>
<td>$t_d$</td>
<td>m</td>
</tr>
<tr>
<td>Airgap thickness</td>
<td>$d_g$</td>
<td>m</td>
</tr>
<tr>
<td>Backplate thickness</td>
<td>$t_b$</td>
<td>m</td>
</tr>
<tr>
<td>Hole density in the backplate</td>
<td>$n$</td>
<td></td>
</tr>
<tr>
<td>Surface fraction occupied by the holes</td>
<td>$\alpha_{bh}$</td>
<td>%</td>
</tr>
<tr>
<td>Poisson's ratio of the diaphragm material</td>
<td>$v$</td>
<td></td>
</tr>
<tr>
<td>Viscosity of air</td>
<td>$\eta$</td>
<td>kg/m-s</td>
</tr>
<tr>
<td>Air density</td>
<td>$\rho_o$</td>
<td>kg/m$^3$</td>
</tr>
<tr>
<td>Young's modulus of the diaphragm material</td>
<td>$E$</td>
<td>GPa</td>
</tr>
<tr>
<td>Velocity of sound in free space</td>
<td>$c$</td>
<td>m/s</td>
</tr>
<tr>
<td>Radius of a backplate acoustical port</td>
<td>$r_{bh}$</td>
<td>m</td>
</tr>
</tbody>
</table>
Table 3-4. Acoustical sensor element design parameter expressions [29]

<table>
<thead>
<tr>
<th>Design parameter</th>
<th>Expression</th>
<th>Unit</th>
<th>Equation Number</th>
</tr>
</thead>
<tbody>
<tr>
<td>Diaphragm rigidity</td>
<td>( D = \frac{E t_d^3}{12(1-\nu^2)} )</td>
<td>Pa.m^3</td>
<td>(3-45)</td>
</tr>
<tr>
<td>Diaphragm tension</td>
<td>( T_D = \sigma_d )</td>
<td>MPa.m</td>
<td>(3-46)</td>
</tr>
<tr>
<td>Resonant frequency</td>
<td>( f_{\text{res}} = \sqrt{\frac{1}{\rho} \left( \frac{D \pi^2}{a^4} + \frac{T_D}{2a^2} \right)} )</td>
<td>Hz</td>
<td>(3-47)</td>
</tr>
<tr>
<td>Air radiative resistance</td>
<td>( R_r = \frac{\rho_0 a^4 \omega^2}{2 \pi c} )</td>
<td>N·s/m^5</td>
<td>(3-48)</td>
</tr>
<tr>
<td>Air radiative mass</td>
<td>( M_r = \frac{8 \rho_0 a^3}{3 \pi \sqrt{\pi}} )</td>
<td>kg</td>
<td>(3-49)</td>
</tr>
<tr>
<td>Diaphragm compliance</td>
<td>( C_m = \frac{32a^2}{\pi^6 (2\pi^2 D + a^2 T_D)} )</td>
<td>m/N</td>
<td>(3-50)</td>
</tr>
<tr>
<td>Equivalent acoustical mass</td>
<td>( M_m = \frac{\pi^4 \rho (2\pi^2 D + a^2 T_D)}{64 T_D} )</td>
<td>kg</td>
<td>(3-51)</td>
</tr>
<tr>
<td>Airgap viscosity loss</td>
<td>( R_s = \frac{12 \eta a^2}{nd^3 \pi} \left( \frac{\alpha_{bh}}{2} - \frac{\alpha_{bh}^2}{8} - \frac{\ln \alpha_{bh}}{4} - \frac{3}{8} \right) )</td>
<td>N·s/m</td>
<td>(3-52)</td>
</tr>
<tr>
<td>Viscosity loss of the backplate holes</td>
<td>( R_h \approx \frac{8 \eta_h a^2}{\pi m_{bh}^4} )</td>
<td>N·s/m</td>
<td>(3-53)</td>
</tr>
<tr>
<td>Airgap compliance</td>
<td>( C_a = \frac{d_s}{\rho_0 c^2 \alpha_{bh}^2 a^2} )</td>
<td>m/N</td>
<td>(3-54)</td>
</tr>
</tbody>
</table>

Total equivalent impedance, \( Z_e \), of the circuit shown in Figure 3-13, thus can be expressed as:
\[ Z_i = Z_a + Z_m = R_r + j \omega (M_r + M_m) + \frac{1}{j \omega C_m} + \frac{R_g + R_h}{1 + j \omega (R_g + R_h) C_a} \]  

(3-55)

The principal design variables are thus, the diaphragm side length, the diaphragm thickness, the backplate thickness, the airgap thickness, the backplate hole radius, and the surface area fraction occupied by the holes.

In [3-8], it is shown that the cutoff frequency of a capacitive-type acoustical sensor is a function of the stiffness of the diaphragm and is inversely proportional to the total acoustical resistance offered by the sensor geometry. Thus, either by increasing the stiffness of the diaphragm or decreasing the total acoustical resistance, the cutoff frequency can be increased. Since an increase in stiffness of the diaphragm will affect the sensitivity, a good method to increase the cut-off frequency is to decrease the acoustical resistance by increasing the acoustic hole density to a limit so that anti-resonance occurring due to lower backplate stiffness doesn’t occur.

### 3.11 Noise Analysis

The equation of motion considering thermal effects is expressed as [12]:

\[ M \ddot{z} + R \dot{z} + Kz = f_n(R, t) \]  

(3-56)

where \( f_n(R, t) \) represents the fluctuating force due to random thermal agitation from the environment and \( R \) represents air resistance due to damping. The spectral density of the fluctuating force following Nyquist relation is given as:
\[ F_n = \sqrt{4K_bTR} \text{ N/Hz} \]  
\[(3-57)\]

where \( K_b \) is Boltzmann’s constant \((1.38 \times 10^{-23} \text{ Joules/Kelvin})\) and \( T \) is the absolute temperature. Spectral density of the fluctuating pressure related to acoustical resistance is expressed as:

\[ p = \sqrt{4K_bTR_{\text{acoustical}}} \]  
\[(3-58)\]

where the acoustical resistance is given by:

\[ R_{\text{acoustical}} = \frac{R}{A^2} \text{ N s/m}^5 \]  
\[(3-59)\]

Equation (3-58) is analogous to Johnson noise related to an electrical resistance [12]. This analogy implies that power spectral density of the fluctuating pressure is uniform over the entire frequency range. The noise bandwidth is expressed as:

\[ \Delta f = \frac{\pi}{2} f_c \]  
\[(3-60)\]

Thus, the fluctuating pressure over a desired frequency band can be given as:

\[ p = \sqrt{4K_bTR_{\text{acoustical}}\Delta f_c} \]  
\[(3-61)\]

The air resistance \( R \) due to damping can be derived from the expressions for the airgap and the backplate hole resistance as was given by (3-52) and (3-53) as:
\[ R = R_e + R_h \quad (3-62) \]

and can be substituted in equation (3-59) to evaluate \( R_{\text{acoustical}} \).

The sound pressure level (SPL) associated with fluctuating pressure is expressed as:

\[ SPL = 20 \log_{10} \left( \frac{p}{20e^{-6}} \right) \text{ dB} \quad (3-63) \]

and the A-weighted noise level can be expressed as [3-17]:

\[ L_A = 10 \log_{10} \sum_{j=1}^{N} 10^{(L_j+A_j)/10} \text{ dB(A)} \quad (3-64) \]

where \( L_j \) are the 1/3 or 1/1 octave band level (dB SPL) and \( A_j \) are the A-weights following the A-curve [53].

3.12 Summary

In this chapter, the mathematical models related to the design of a MEMS-based acoustical sensor element are presented that leads to an integrated design methodology. A new analytical model has been developed to determine the pull-in voltage related to voltage controlled MEMS-based capacitive-type acoustical sensors with square diaphragms. The model has been validated by comparing with FEA and published experimental results. The developed model is simple, easy to use, fast, and can approximate the pull-in voltage for a square diaphragm case with a maximum difference of 2.5 % with FEA or experimental
results within some limitations. The method, followed to develop the model is a
generalized one and was also applied to develop a new model to determine the
pull-in voltage for a circular diaphragm case. The evaluated pull-in voltage differs
less than 2% with the definitive empirical models provided in [10]. This further
validates the method and the models. This generalized approach can be used to
determine the pull-in voltage for other microstructures, such as cantilever beams,
or fixed-fixed beams under electrostatic excitation. Mathematical models related
to mechanical impedance, sensitivity analysis, noise analysis, and various design
parameters are presented based on which a step-by-step design procedure can
be implemented.
Chapter 4

Microarray Design and Fabrication

In this chapter, the beamforming concept developed in the chapter 2 for an acoustical sensor microarray has been used as a basis to design the target microarray for use in a hearing aid instrument. Due to space constraints of the target application, every effort was made to best utilize the available application area considering packaging, materials and fabrication process capabilities. These considerations contributed to a new innovative geometry for the sensor microarray. These design considerations coupled with the relevant theory of a MEMS capacitive acoustical sensor design presented in chapter 3 has been used to optimize the array performance while satisfying the design constraints. Three-dimensional electromechanical finite element analysis has been carried out to verify the analytical models. Finally, a step-by-step process table has been developed to fabricate the microarray.

4.1 Design Requirements

The preliminary design considerations include:

1. Array geometry

2. Array layout
3. Type of acoustical sensors (microphones)

4. Inter-element spacing requirements for beamforming

5. Maximizing the active sensor area

6. Interfacing and interconnectivity concerns

7. Sensor self-noise

8. Fabrication process considerations

9. Operating environment

10. Dynamic range

The average adult ear canal has an approximate diameter of about 8.0 mm. Allowing for a clearance space of 1.0 mm around for custom ear-mold fitting purposes, the available area for a planar square array is about 4.0 x 4.0 mm² as shown in Figure 4-1a. The area can be further increased to 4.6 x 4.6 mm² by modifying the four corners of the square array as shown in Figure 4-1b.

A square planar array of identical size sensor elements (microphones) with uniform spacing and symmetrical distribution appears to be a good choice for a hearing aid instrument to ensure maximum utilization of available space in the ear canal.

Since the contact pads for biasing and readout circuitry takes a considerable amount of lateral space, they can be drawn at the bottom side of the array
Figure 4-1. Microarray array target geometry
structure using 25 μm square wafer-through-hole aluminum-via-interconnects.

A dimension of 75x75 μm² then can be chosen for a contact pad to be in compliance with the International Technology Roadmap for Semiconductors (ITRS), 1999 edition [38]. A spacing of 250 μm between adjacent microphone elements has been chosen to meet the electrical isolation and fabrication requirements. Another 250 μm spacing from the die edge is required for routing of interconnect traces, fabrication and also for die handling purposes. The remaining lateral area can thus be used for sensing purposes. Since the change in capacitance of a microphone structure due to an external acoustical pressure is very small (of the order of a few femtoFarad), it is desirable to maximize the sensing area of each microphone. These requirements and constraints lead to the adoption of a 3 x 3 planar array geometry. Each element has an active sensor area (diaphragm size) of 1.2 x 1.2 mm².

4.2 Packaging Considerations

With the contact pads drawn at the bottom side of the array structure to maximize the available space for sensing purposes, a surface mounting capability is desirable for the array structure for packaging and connectivity purposes. Common geometries of MEMS based capacitive type microphones have a backside cavity created by either wet or dry etching of the silicon wafer as shown in Figure 4-2a and Figure 4-2b. The cavity is also being used to release the sacrificial layer between the diaphragm and the backplate by pouring a wet etchant through the backplate holes. These geometries further require anodic
bonding with another substrate, usually PSG (Phosphosilicate glass) to facilitate packaging or surface mounting. A high voltage, usually of the order of 700-1200 volts [54], is necessary to perform the anodic bonding process. As a result of this high voltage, an electrostatic force much higher than the pull-in limit of the structure is developed. This electrostatic force can cause unwanted sticking, diaphragm damage, and even bonding of the diaphragm onto the backplate [9]. To avoid this situation, a conceptually new geometry is being proposed. The sacrificial layer is to be removed through small windows (air outlet port) created on the topside of the array structure in the spaces around the sensor elements as is shown in Figure 4-2c. Air cavities under the backplate of each microphone structure has been created for damping purposes using deep reactive ion etching of the wafer while keeping the bottom surface intact. Air streaming out of the inside cavities will pass through these air outlet ports, and thereby will provide the necessary damping. In this way the structure will be robust, provide surface mounting without additional anodic bonding and will have higher strength comparing to conventional geometries.
Figure 4-2. (a) Bulk micromachined, backside etched MEMS capacitive microphone proposed by Mastrangelo in 1998 [29]. (b) Bulk micromachined, backside etched, dual diaphragm MEMS capacitive microphone proposed by Rombach in 2002 [8]. (c) This work proposes a bulk micromachined concealed cavity, flat bottom architecture that enables surface mounting without anodic bonding.
4.3 Material Selection

Polysilicon, silicon nitride, polyamide and monocrystaline silicon are the most common materials used to fabricate a diaphragm. During the fabrication process, residual stresses are accumulated in the diaphragm equal to the sum of the thermal and intrinsic stresses [36]. Thermal stress is caused by a difference in the expansion coefficient of the substrate and that of the thin film. Intrinsic stress has two components, the first originates from the volume contraction associated with crystallization and is tensile, the second is compressive and is due to the existence of a preferred growth orientation, disorder at the grain boundary, and effects related to different deposition rates or the incorporation of impurity atoms. The dominant component of stress is the intrinsic value and the stress gradient along the direction of growth of a thin film contributes to the residual stress [55].

This residual stress changes the vibrational characteristics of the microphone diaphragm by causing it to buckle up or down based on the type of the stress (tensile or compressive) and consequently influences the microphone's first resonant frequency mode, cutoff frequency, pull-in characteristic, and sensitivity. The residual stress can also lead to degradation of electrical characteristics of a thin film and yield loss through defect generation.

There are some methods available to control the residual stress. One method is to anneal the thin film at a high temperature between 900 °C and 1100 °C in a nitrogen atmosphere after ion implantation by Boron, Phosphorous or
Arsenic. High temperature annealing of a low-pressure chemical vapor deposition (LPCVD) of polysilicon thin film that is ion implanted with phosphorous, can confine the residual stress to as low as 20 MPa [29]. Thus, low-stress polysilicon is a common choice for the diaphragm material.

However, an alloy of polycrystalline silicon-germanium (poly-SiGe) offers some advantages over low-stress polysilicon. Poly-SiGe has properties similar to polysilicon, but can be conformally deposited and doped at much lower temperatures (less than 500°C) than polysilicon [55] [56] [57]. This simplifies the integration with CMOS devices and allows surface passivation to reduce stiction effects. Poly-SiGe with a high Ge content can be etched in solutions of NH₄OH and H₂O₂ (RCA). Poly-SiGe structural and sacrificial layers can be deposited in the same chamber by changing the percentage of Ge content [57].

In addition, poly-SiGe has a lower strain and strain gradient in comparison to polysilicon. High temperature annealing is therefore not necessary in all cases. The Poly-Ge sacrificial layer is highly conformal and this allows the structure to be an accurate reproduction of the mold wafer. Instead of a poly-Ge sacrificial layer, a conventional SiO₂ sacrificial layer can be used as well. It is reported [55] that poly-SiGe shows almost flat surface planes due to the uniformity of stress (low stress gradient) along the direction of growth. The stress induced decrease in the airgap thickness associated with a microphone having a polyamide diaphragm (resulting in a decreased sensitivity) [7] will not occur for a microphone with a poly-SiGe diaphragm.
LPCVD silicon nitride ($\text{Si}_3\text{N}_4$) has uniform film thickness, a Young's modulus higher than silicon, high dielectric strength, hard, and can has a residual stress within a range of 450-1000 MPa [36] [48]. To avoid anti-resonance, a thin perforated backplate is required to have a high level of residual stress. For these reasons LPCVD silicon nitride is chosen to fabricate the capacitive microphone's backplate. The backplate can be made to serve as an electrode of the capacitor by depositing an electrically conducting gold layer over the nitride layer. The high dielectric strength of the nitride layer will provide the necessary electrical isolation from the underlying silicon wafer. In this way, a backplate with sufficient strength can be realized from a lower thickness thin film. This simplifies the fabrication process, compared to the process where boron doped etch stops are used to create the microphone backplate while performing bulk micromachining of the silicon wafer [29].

PECVD deposited silicon nitride layer (SiN) has been chosen as insulation barrier between the diaphragm and the backplate. The physical properties of poly-SiGe (60% Ge content), LPCVD silicon nitride and PECVD silicon nitride are listed in Table 4–1 [36][56].
Table 4-1. Properties of materials selected for microarray fabrication

<table>
<thead>
<tr>
<th>Properties</th>
<th>Poly-SiGe</th>
<th>Si₃N₄</th>
<th>SiN</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Density</td>
<td>3.2</td>
<td>2.9-3.2</td>
<td>2.4-2.8</td>
<td>(gm/cm³)</td>
</tr>
<tr>
<td>Young’s Modulus</td>
<td>155</td>
<td>275</td>
<td>240</td>
<td>GPa</td>
</tr>
<tr>
<td>Poisson’s Ratio</td>
<td>.28</td>
<td>.27</td>
<td>.25</td>
<td></td>
</tr>
<tr>
<td>Residual stress</td>
<td>20</td>
<td>454-1100</td>
<td>60.7</td>
<td>MPa</td>
</tr>
<tr>
<td>Coefficient of thermal</td>
<td>3.8</td>
<td>2.8</td>
<td>1.6</td>
<td>10⁻⁶/°C</td>
</tr>
<tr>
<td>expansion</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Thermal conductivity</td>
<td>8.3</td>
<td>36</td>
<td>2.23</td>
<td>W/m-K</td>
</tr>
<tr>
<td>Dielectric strength</td>
<td>13.13</td>
<td>10</td>
<td>7.5</td>
<td></td>
</tr>
<tr>
<td>Resistivity</td>
<td>Depends on doping</td>
<td>10¹⁶</td>
<td>10⁶-10¹⁵</td>
<td>Ω-cm</td>
</tr>
</tbody>
</table>

4.4 Microarray Design

Following the equation sets listed in Table 3-4, the thickness of the diaphragm, airgap thickness, diaphragm residual stress, the number of backplate acoustical ports and other parameter values are determined. For the chosen parameter values, the pull-in voltage was calculated using equation (3-28) as 17.45 Volts. A 3-D electromechanical finite element analysis was then carried out to determine the pull-in voltage as 17.85 volts. Detailed design specifications are given in Table 4-2.

Conventional hearing aid instruments use a battery ranging from 1.4-3 volts to provide the required power supply for the hearing aid instrument. It is assumed that a DC-DC voltage converter as described in [7] can be used to
**Table 4-2. Microarray final design specifications**

<table>
<thead>
<tr>
<th>Design parameter</th>
<th>Value</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Array physical dimensions</td>
<td>4.6 x 4.6</td>
<td>mm²</td>
</tr>
<tr>
<td>Physical microphone spacing, $d_{xr} = d_{yr}$</td>
<td>250</td>
<td>µm</td>
</tr>
<tr>
<td>Number of microphones in the array ($M \times N$)</td>
<td>9 (3 x 3)</td>
<td>-</td>
</tr>
<tr>
<td>Diaphragm side length and width (each microphone), $a$</td>
<td>1200</td>
<td>µm</td>
</tr>
<tr>
<td>Diaphragm thickness, $t_d$</td>
<td>0.8</td>
<td>µm</td>
</tr>
<tr>
<td>Airgap thickness, $d_g$</td>
<td>3.5</td>
<td>µm</td>
</tr>
<tr>
<td>Number of acoustical ports (holes)</td>
<td>288</td>
<td>Number</td>
</tr>
<tr>
<td>Backplate hole size (each microphone), $bh$</td>
<td>30 x 30</td>
<td>µm²</td>
</tr>
<tr>
<td>Surface fraction occupied by holes, (each microphone), $\alpha_{bh}$</td>
<td>18.0%</td>
<td>%</td>
</tr>
<tr>
<td>Backplate thickness, $t_b$</td>
<td>1.0</td>
<td>µm</td>
</tr>
<tr>
<td>Diaphragm material</td>
<td>Poly-SiGe (60% Ge)</td>
<td></td>
</tr>
<tr>
<td>Poly-SiGe residual stress, $\sigma$</td>
<td>20</td>
<td>MPa</td>
</tr>
<tr>
<td>Bias voltage, $V$</td>
<td>12</td>
<td>Volts</td>
</tr>
<tr>
<td>Sensitivity at 1 kHz (Depends on readout circuitry), $S$</td>
<td>10.3</td>
<td>mV/Pa</td>
</tr>
<tr>
<td>Cut-off frequency (each microphone), $f_c$</td>
<td>18</td>
<td>KHz</td>
</tr>
<tr>
<td>Zero pressure capacitance (each microphone), $C$</td>
<td>3.64</td>
<td>pF</td>
</tr>
<tr>
<td>Pull-in voltage (each microphone), $V_{pi}$</td>
<td>17.85</td>
<td>Volts</td>
</tr>
</tbody>
</table>

*boost the power supply to 12 volts without any difficulty. An operating supply volts of 12 volts seems to be adequate as it is reasonably lower than the determined the pull-in voltage considering also the uncertainties and non-*
idealities associated with the fabrication process. For a bias voltage of 12 volts, the determined parameters values yield a sensitivity of 10.3 mV/Pa (-39.82 dB, reference to 1V/Pa) at 1.0 KHz for each of the acoustical sensor elements of the microarray. Figure 4-3 shows the frequency response of a sensor element in the microarray. The upper cutoff frequency of a sensor element is about 18 KHz.

Figure 4-3. Frequency response of an acoustical sensor element in the microarray
4.5 3-D Static Electromechanical Finite Element Analysis

The detailed simulation setup instructions and rules to carry out 3-D electromechanical finite element analysis using IntelliSuite™ design tools are available in [58]. The basic simulation procedures are: (1) Import a 3-D model of the structure in the electromechanical simulation window. The 3-D model can be generated either by simulating the fabrication process steps or by using the manual builder module. If the model is symmetrical, a quarter model simulation will reduce the analysis time substantially, (2) assign material properties as necessary, (3) select a part of the device to receive a load, e.g. voltage, pressure or temperature, etc. The load may be static or dynamic. In dynamic case it is possible to apply a step, ramp or sinusoidal excitation of a desired frequency, time frame and magnitude, (4) set boundary conditions, (5) mesh creation, (6) choose analysis type, for example linear or nonlinear (large deflection), (7) run the analysis, and finally, (8) view the analysis results.

Meshing Considerations

IntelliSuite™ uses 20-node brick elements because of the high quality and accuracy of these elements [58]. After extensive numerical testing, linear elements (such as 8-node brick elements) were found to be inefficient for MEMS simulations. These linear elements usually require a prohibitively fine discretization (especially through the thickness) that leads to large numerical models. Tests on a tetrahedral family of elements also showed that a larger number of nodes and elements are required to achieve the same accuracy as a
mesh consisting of 20-node brick elements. In MEMS applications especially, the tetrahedral elements in a mesh comprised solely of tetrahedrons can become highly distorted leading to numerical inaccuracies. In summary, the 20-node brick elements achieve a balance between its numerical costs and its predictive capabilities and accuracy [58].

In IntelliSuite™ it is possible to refine both the mechanical mesh and the electrical mesh. The refinement of the mechanical mesh is limited by the available memory. The Mech_mesh option allows the user to locally refine the mesh on certain faces of the structure. In IntelliSuite™, the maximum mesh panel size is recommended to be of a value of 2-10% of the XY dimension of the device. A mesh convergence study must be carried out to obtain high accuracy results. Reducing a mesh panel size beyond the mesh convergence limit results in inaccurate results due to truncation error. Since the electromechanical simulation is highly time consuming, to keep the problem size small and reach a fairly good mesh convergence rapidly, a natural frequency analysis of the structure in the mechanical domain for successively decreasing mesh sizes is highly useful. When for a particular mesh size, the FEA results and the calculated fundamental frequency of the structure are within an acceptable value of accuracy, it can be concluded that the mesh convergence has been achieved and the desired electromechanical simulation can be carried out.

The Elec_mesh option is used to activate the new Exposed Face Mesh algorithm (EFM) to execute three-dimensional coupled electromechanical
analysis. When compared to the commonly used volume refining mesh method, the EFM algorithm shows substantial improvement in increasing accuracy of results and reducing computational time and memory expenses. In the design of microelectromechanical systems, the accurate calculation of electrostatic pressure (or force) on the structure surface is essential in determining the structural deformation. Many of these devices have specific faces on which the electrostatic pressure is critical for determining the device electromechanical behavior. Examples of such planes include the deformable face of capacitive pressure sensors and the movable finger tips of surface micromachined accelerometers. These faces are referred to as Exposed Faces due to their exposure to other electric field sources. In order to calculate the electrostatic pressure on these Exposed Faces, the commonly used method is to refine the three-dimensional domain. Unfortunately, the modeling of typical electrostatically activated MEMS using the volume mesh method results in large problem sizes.

Instead of refining the volume mesh, *Elec_mesh* can be used to refine only the electrostatic surface mesh on chosen Exposed Faces. The advantage of this novel method is that the surface mesh used in the electrostatic analysis is separated from the mechanical volume mesh while assuring full compatibility between the two. The EFM method results in smaller computational models while improving the numerical accuracy in MEMS simulation. The *Elec_mesh* option is activated by providing a value for a refinement factor $N$. Selecting a refinement factor of 4 refines the mesh $2N^2$ or 32 times [58].
Applying the above procedure, the 3-D static electromechanical finite element analysis of the microphone structure was carried out without applying any external pressure load. To keep the problem size small, only a quarter model of the square diaphragm and the back plate was simulated. A mechanical mesh size of 10 µm and a value of 8 was used for the refinement factor $N$ to refine the electrical mesh. That refines the mechanical mesh by $2N^2$ times resulting in a refinement of $128$ times of the mechanical mesh. Thus a very fine mesh resolution was utilized. A bias voltage of 12 volts was used as specified in Table 4-2. Figure 4-4 shows a deformation of 0.404 µm for the diaphragm midpoint after performing a 3-D electromechanical finite element analysis for an applied bias voltage of 12 volts. The analytical result following the method described in chapter 3 predicts a deformation of 0.415 µm for the diaphragm midpoint when a bias voltage of 12 volts is applied. This shows excellent agreement between the analytical and 3-D FEA results. Figure 4-5 shows the electrostatic pressure distribution when 12 volts of bias voltage is applied. Figure 4-6 shows the change of capacitance due to applied bias voltages ranging from 0-18 volts. The figure shows the static capacitance of a sensor element (zero bias voltage) as 3.72 pF. The calculated analytical value is 3.64 pF, also in excellent agreement with theoretical findings. Finite element analysis results also shows that the maximum magnitude of the developed stress is much small compared to the yield strength of polysilicon Germanium (<10%). This ensures desired elastic deformation of the diaphragm.
Figure 4-4. Z-axis displacement of the diaphragm at a bias voltage of 12 volts
Figure 4-5. Electrostatic pressure profile at a bias voltage of 12 volts
Figure 4-6. 3-D electromechanical finite element analysis result showing the change of capacitance at different bias voltages ranging from 0-18 Volts
4.6 3-D Dynamic Electromechanical Finite Element Analysis

4.6.1 Direct Integration Transient Analysis

IntelliSuite™ uses one of the implicit methods based on the Hilber-Hughes-Taylor operator for the direct integration based transient analysis. Implicit methods use implicit time integration to calculate the transient dynamics of a system [58]. The advantage implicit integration offers is that it is unconditionally stable for linear systems. There is no limit on the size of time increment that can be used to integrate a linear system. IntelliSuite™ uses another advanced method of carrying out transient and steady-state analysis. The method uses Rayleigh proportional damping. Mass damping factor defines the mass proportional damping, which has units of (1/time) and the damping ratio is inversely proportional to the frequency, therefore contributes mostly to the low frequency domain. Stiffness damping factor is proportional to the elastic material stiffness, which has units of (1/time), the damping ratio is directly in proportion with the frequency, and contributes mostly the high frequency domain.

For this method, the equation of motion can be described as:

\[ \hat{M}\ddot{z} + \hat{B}\dot{z} + \hat{K}z = F \]  \hspace{1cm} (4-1)

where \( \hat{M} \), \( \hat{B} \), and \( \hat{K} \) are matrices representing, mass, damping and stiffness, respectively and \( F \) is the applied external force. The damping matrix \( \hat{B} \) can be expressed as:
\[ \hat{B} = \alpha \hat{M} + \beta \hat{K} \]  

(4-2)

where \( \alpha \) and \( \beta \) represent the mass damping factor and the stiffness damping factor, respectively.

4.6.2 Mode Based Transient Analysis

Mode based transient analysis is used to analyze linear dynamic problems using modal superposition [58]. This scheme assumes the structure's dynamic response is based on a subset of the eigenmodes of the system. The subset of the eigenmodes, or the number of modes must be sufficient to model the dynamic response of the system. As the number of modes is increased, the solution will converge to the same stable solution achieved using direct integration method provided the same type of damping is specified.

The two mode damping factors or ratios (\( \xi_1 \) and \( \xi_2 \)) associated with two specific natural frequencies (\( \omega_1 \) and \( \omega_2 \)) or modes have the following relationship with the mass damping factor (\( \alpha \)) and stiffness damping factor (\( \beta \)):

\[ \xi_1 = \frac{\alpha \omega_1}{2} + \frac{\beta}{2 \omega_1} \]

(4-3)

and

\[ \xi_2 = \frac{\alpha \omega_2}{2} + \frac{\beta}{2 \omega_2} \]

(4-4)
where $\omega_1$ and $\omega_2$ are the natural frequencies. The rest of the modal damping factors, $\xi_i$, can be extracted from:

$$\xi_i = \frac{\alpha}{2\omega_i} + \frac{\beta \omega_i}{2} \tag{4-5}$$

The equation of motion for the mode based transient analysis is expressed as:

$$\ddot{z}_i + 2\xi_i \omega_i \dot{z}_i + \omega_i^2 z_i = p_i(t), \quad i = 1, 2, 3, \ldots, m \tag{4-6}$$

### 4.6.3 Mode Based Steady-State Analysis

Steady-state analysis provides the steady state amplitude and phase response of a system due to harmonic excitation at a given frequency. Usually such analysis is done as a frequency sweep by loading at a series of different frequencies and recording the response. In the mode based steady state dynamic analysis, the response is calculated on the basis of the system's eigenfrequencies and eigenmodes.

The modal equation of motion for harmonic excitation can be expressed as:

$$\ddot{z}_i + 2\xi_i \omega_i \dot{z}_i + \omega_i^2 z_i = p_i \sin(\omega t), \quad i = 1, 2, 3, \ldots, m \tag{4-7}$$

The mass damping factor, $\alpha$, and the stiffness damping factor, $\beta$, can be obtained from a knowledge of the quality factor of the diaphragm. The quality factor associated with mode damping factors can be expressed as:
\[ Q_i = \frac{1}{2\xi_i} \]  \hspace{1cm} (4-8)

However, assuming squeeze film damping in the airgap between the diaphragm and the backplate, the quality factor of a square diaphragm can be expressed as:

\[ Q_M = \frac{d}{\eta a^2 \sqrt{MK}} \]  \hspace{1cm} (4-9)

where \( \eta \) is the viscosity of air, \( M \) and \( K \) are the lumped element mass and spring constant of the diaphragm, respectively. For the first or the fundamental mode, assuming a stiffness proportional damping \( \beta = 0 \), we have:

\[ \xi_i = 1/2Q_M, \alpha = 2\omega_i\xi_i \]  \hspace{1cm} (4-10).

Using (4-9) and (4-10), the mass damping factor \( \alpha \) can be evaluated and used to carry out necessary steady state analysis.

Assuming the stiffness proportional damping \( \beta = 0 \), the values of \( \alpha \), and \( Q_M \) associated with a sensor structure are evaluated as \( 7.7 \times 10^4/\text{sec} \) and 3.8, respectively.

The first six natural frequencies of the microphone structure were evaluated using IntelliSuite™ mechanical analysis module. The natural frequencies and associated mode damping factors are listed in Table 4-3.
Table 4-3. Natural frequencies and damping factor for the first six modes

<table>
<thead>
<tr>
<th>Mode number</th>
<th>Mode frequency (Hz)</th>
<th>$\xi_i$</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>4.858e4</td>
<td>0.1259</td>
</tr>
<tr>
<td>2</td>
<td>7.719e4</td>
<td>0.0792</td>
</tr>
<tr>
<td>3</td>
<td>7.719e4</td>
<td>0.0792</td>
</tr>
<tr>
<td>4</td>
<td>9.81e4</td>
<td>0.0623</td>
</tr>
<tr>
<td>5</td>
<td>1.105e5</td>
<td>0.0555</td>
</tr>
<tr>
<td>6</td>
<td>1.105e5</td>
<td>0.0555</td>
</tr>
</tbody>
</table>

4.6.4 Dynamic Analysis Results

Following the procedures described in the previous sections, the direct integration based transient analysis and mode based steady state analyses were carried out for one of the sensor element. The load application window used to enter a step load for the direct integration based transient analysis is shown in Figure 4-7. The result of the direct integration based transient analysis is shown in figure 4-8. The mode-based steady-state analysis result for a frequency range of 100-70,000 Hz is shown in Figures 4-9 and 4-10. Mode based harmonic excitation result is shown in Figure 4-11. The calculated first natural frequency value matches closely with the FEA analysis result marked by a resonance as shown in Figure 4-9.
Figure 4-7. (a) Load application window for direct integration based transient analysis for a sensor element. (b) A plot of the applied load.
Figure 4-8. Result of direct integration based transient analysis
Figure 4-9. Mode based steady state analysis (Magnitude response)
Figure 4-10. Mode based steady state analysis (Phase response)
Figure 4-11. Mode based steady state analysis for harmonic excitation at a maximum acoustical pressure ($P_{max}$) of 1.0 Pascal (94 dB SPL).
4.7 Microarray Noise Performance

Following the method outlined in the section 3-11, the noise performance of a microphone element in the array was evaluated. The results are summarized in Table 4-4.

Table 4-4. Noise Analysis Results

<table>
<thead>
<tr>
<th>Noise variables</th>
<th>Design value</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Acoustical resistance due to airgap</td>
<td>$7.8190 \times 10^8$</td>
<td>N·s/m$^5$</td>
</tr>
<tr>
<td>Acoustical resistance due to backplate hole</td>
<td>$.9758 \times 10^5$</td>
<td>N·s/m$^5$</td>
</tr>
<tr>
<td>Total acoustical resistance</td>
<td>$7.82 \times 10^8$</td>
<td>N·s/m$^5$</td>
</tr>
<tr>
<td>Noise pressure</td>
<td>$3.56 \times 10^{-6}$</td>
<td>Pa</td>
</tr>
<tr>
<td>Noise in SPL</td>
<td>29.97</td>
<td>DB (SPL)</td>
</tr>
<tr>
<td>A-weighted noise</td>
<td>26.56</td>
<td>dB(A)</td>
</tr>
</tbody>
</table>
4.8 Microarray Fabrication

In this section, the fabrication process steps associated with the fabrication of the sensor microarray using state-of-the-art MEMS fabrication techniques has been described. For better visualization and understanding, only one microphone structure is shown in a respective figure. To highlight certain features, the thickness and widths of some layers have been exaggerated. Some common but necessary steps like Piranha or RCA cleaning [58], photoresist curing, solvent removing, promoter layers, etc. have been omitted while major fabrication steps are highlighted. Detailed fabrication process table developed to simulate the fabrication of the sensor microarray using IntelliSuite™ is annexed as Appendix II. The whole fabrication process sequences of the microarray have been grouped into eight steps and are described below.

Step 1

The process starts with the deposition of a 75 nm thick silicon nitride layer by LPCVD process on the backside of a 400 μm thick <100> oriented n-type Czochralski silicon substrate. The substrate topside is then patterned using a 200 nm thick layer of aluminum. Wafer through-holes (25 x 25 μm²) and designated volumes for inside air chambers and air outlet ports are etched using an inductively coupled plasma–reactive ion etching (ICP-RIE) process. A 75 nm thick silicon nitride layer is next deposited in the wafer through-holes by a LPCVD process. A 70 nm thick layer of chromium is then deposited in the wafer through-holes by E-Beam evaporation. This process is followed by the sputtering

115
of a 30 nm thick layer of titanium as a seed layer. Aluminum is then electrodeposited in the wafer-through-holes using a solution of aluminum chloride and lithium aluminum hydride-ethereal [59]. Silicon dioxide is deposited in the designated volumes (20 μm thick) by a PECVD process and densified at 1100 °C in N₂ at ambient pressure [60]. Figure 4-12a shows a drawing of the result of this
Figure 4-13. Wafer-through-hole aluminum via interconnect fabrication details. (a) DRIE etched wafer-through-hole. (b) Electroplated aluminum with chromium adhesion layer and titanium seed layer deposited on silicon nitride insulation. (c) Topview of the wafer-through-hole after etching.
process step while Figure 4-12b shows the result of the simulation of this process step using IntelliSuite™. Figure 4-13 highlights the wafer-through-hole aluminum-via-interconnect mechanism.

**Step 2**

A 1.0 μm thick layer of silicon nitride is deposited on the wafer topside by a LPCVD process. The nitride layer is patterned and plasma etched using CF₄/O₂. Over the nitride layer a 30 nm thick layer of titanium is magnetron sputtered. This step is followed by the E-Beam evaporation of a 30 nm thick layer of gold. The titanium layer acts as an adhesion base for the gold layer that is used as the backplate electrode. Figure 4-14a shows a drawing of the result of this process step while Figure 4-14b shows the result of the simulation of this process step using IntelliSuite™.

**Step 3**

The gold and titanium layers are then patterned and dry etched using a Cl₂ plasma process. Next, the silicon nitride layer is dry etched using CF₄/O₂ plasma to form the acoustical ports. Figure 4-15 shows the mask layout used to etch the acoustical ports. Figure 4-16a shows a drawing of the result of this process step while Figure 4-16b shows the result of the simulation of this process step using IntelliSuite™.
Figure 4-14. Microarray fabrication step 2. (a) 2-D cross-sectional view. (b) 3-D cross-sectional view of a single microphone after simulating the mentioned fabrication process.

**Step 4**

A 3.5 \( \mu \text{m} \) thick layer of silicon dioxide is then deposited by a LPCVD process for airgap definition. The top surface of the silicon dioxide layer is polished to have a planar surface. The oxide layer is then patterned and etched dry using CHF\(_3\)/O\(_2\). A 1.0 \( \mu \text{m} \) thick low stress silicon nitride (SiN) layer is then deposited by a PECVD process. The PECVD nitride layer is then patterned and dry etched using CHF\(_3\)/O\(_2\). Figure 4-17a shows a drawing of the result of this process step.
Figure 4-15. Etch mask to fabricate backplate acoustical ports

while Figure 4-17b shows the result of the simulation of this process step using
IntelliSuite™.

Step 5

A 40 nm thick layer of polysilicon and a 760 nm thick layer of poly-SiGe (60% Ge) are deposited by a LPCVD process using SiH₄ and GeH₄ as gas sources. These two layers are In-situ boron doped using B₂H₆ with an implant dose of 4x10¹⁵ cm⁻² (Boron) using an implant energy of 20 KeV [61]. Both the layers are
Figure 4-16. Microarray fabrication step 3. (a) 2-D cross-sectional view. (b) 3-D cross-sectional view of a single microphone after simulating the mentioned fabrication process.

then annealed at 900 °C for 40 minutes to reduce the residual stress and resistivity. These two layers are then patterned and etched with $\text{SF}_6/\text{CH}_4$ plasma. Figure 4-18a shows a drawing of the result of this process step while Figure 4-18b shows the result of the simulation of this process step using IntelliSuite™.
Figure 4-17. Microarray fabrication step 4. (a) 2-D cross-sectional view. (b) 3-D cross-sectional view of a single microphone after simulating the mentioned fabrication process.

**Step 6**

The wafer topside is then protected with a thick layer of low temperature oxide (LTO). The wafer backside nitride layer is patterned and etched over the aluminum-via-interconnect region. Figure 4-19a shows a drawing of the result of this process step while Figure 4-19b shows the result of the simulation of this process step using IntelliSuite™.
Step 7

A 1.0 μm thick layer of aluminum is then deposited on the wafer backside using a DC magnetron sputtering method, patterned and etched to form 75 x 75 μm² contact pads. A 75 nm thick PSG is then deposited, patterned and etched
Figure 4-19. Microarray fabrication step 6. (a) 2-D cross-sectional view. (b) 3-D cross-sectional view of a single microphone after simulating the mentioned fabrication process.

on the wafer backside. Figure 4-20a shows a drawing of the result of this process step while Figure 4-20b shows a zoomed view of one of the aluminum contact pads after simulating this process step using IntelliSuite™.
Figure 4-20. Microarray fabrication Step 7. (a) 2-D cross-sectional view. (b) Zoomed view of a bottom side contact pad after simulating the mentioned fabrication process.

**Step 8**

The topside protective LTO layer is then stripped. A buffered oxide etch (BOE) is then performed to sacrificially etch the silicon dioxide through the air outlet ports in between the adjacent microphones to release the diaphragm and
Figure 4-21. Microarray fabrication Step 8. (a) 2-D cross-sectional view. (b) 3-D cross-sectional view of a single microphone after simulating the mentioned fabrication process.
the structure is then freeze-dried using cyclohexane at atmospheric pressure, under a continuous flow of nitrogen, to avoid stiction. Figure 4-21a shows a drawing of the result of this process step while Figure 4-21b shows the result of the simulation of this process step using IntelliSuite™.

Figure 4-22 shows a perspective view of the sensor microarray in the IntelliSuite™ design environment after completion of the fabrication process steps simulation. The corners of the array die will be shaped as was shown in Figure 4-1 during dicing. Figures 4-23 and 4-24 show the topview and the bottom view of the array die, respectively. Figure 4-25 shows a cross sectional view of the array die generated using IntelliSuite™ by simulating the process steps.

Figure 4-22. A perspective view of the sensor microarray in the IntelliSuite™ design environment after simulating the fabrication process steps
Figure 4-23. A bottom view of the sensor microarray in the IntelliSuite™ design environment after simulating the fabrication process steps

Figure 4-24. A topview of the sensor microarray in the IntelliSuite™ design environment after simulating the fabrication process steps
Figure 4-25. A cross-sectional view of the sensor microarray in the IntelliSuite™ design environment after simulating the fabrication process steps
4.9 Summary

In summary, the design and simulation of a MEMS based acoustical sensor microarray that can be mounted in the ear canal has been carried out. The square shaped microarray, consisting of nine sensor elements in a 3 x 3 planar layout occupies a footprint area of 4.6 mm x 4.6 mm. Each sensor element of the microarray has an active sensing area of 1.2 mm x 1.2 mm and exhibits a calculated sensitivity of 10.3 mV/Pa. The 3-D static and dynamic electromechanical finite element analysis results are in close agreement with the analytical values. A fabrication process table has been developed to fabricate the device. The fabrication process table has been simulated using IntelliSuite™ to generate a 3-D model of the sensor microarray. The generated 3-D model of the sensor microarray satisfies design requirements.
Chapter 5

MEMS Micropackaging Solution

In this chapter the design of a MEMS-based modular micropackaging solution for the sensor microarray is described. A very low change of the sensor capacitance due to an external acoustical pressure demands for a highly optimized electrical connectivity mechanism between the MEMS sensor microarray and the microelectronics circuitry. On the other hand, as the array is intended for use in a hearing aid instrument that can be mounted in the ear canal, surface contamination may occur. Thus, the packaging of the array must provide easy removal and replacement capability for cleaning or replacement purposes. Conventional packaging solutions are not adequate for this kind of application. The major challenge here is the design of a low impedance, high pitch, and short length contact mechanism that can provide a reliable but non-permanent electrical interconnectivity. In conventional temporary interconnect mechanisms, the package and the contacts are fabricated separately and are then assembled together, either manually or by an automated process. A new approach can be made to fabricate the package and the contacts simultaneously taking the advantage of the MEMS fabrication technology. Vertical integration of the MEMS and microelectronics dies in a three-dimensional fashion will provide tremendous advantage for applications where lateral space is a constraint, such
as the case of ear canal mountable hearing instruments. A new kind of packaging solution can be developed to provide these functionalities if silicon is used for the package material instead of conventional epoxy. MEMS technology then can be used to fabricate the microspring contacts on a silicon wafer that is etched DRIE to create fixtures to hold the dies and provide routing of the interconnects from one module to the other. This kind of silicon based, MEMS implemented, modular micropackaging solution can enable highly efficient, reliable, and non-permanent electrical interconnectivity of the sensor microarray to the microelectronics circuitry and power supply while providing a robust mechanical protection and excellent thermal management. In the following sections, complete design procedure, simulation, fabrication, and electrical characterization of the proposed micropackaging solution are presented.

5.1 Concept Illustration

Integration of diverse technological origin dies or devices, to realize a complete working system in a micropackage is a major technical challenge. Application specific packaging and interconnectivity scheme is necessary to suite the specific requirements demanded by the type of application and operating environment. The developed acoustical sensor microarray must be packaged in such a manner that it can operate in the ear canal and can be interconnected to the associated signal conditioning electronics and digital signal processing elements and output amplifiers. The resulting mixed-signal environment requires a sophisticated packaging solution. In addition, MEMS technology still lacks the capability of fabricating acoustically transparent thin films that can be used to
protect the array from environmental contamination while not interfering with beamforming. Consequently, when the array is required to be deployed in the contaminative environment of the ear canal, there is potential for surface contamination and the array may lose its functional characteristics in course of time. Thus, in addition to establishing electrical connectivity and providing mechanical protection, the packaging of the microarray die should also facilitate easy insertion and removal capability for cleaning and replacement purposes. Conventional packaging, as it provides a permanent bond between a MEMS device and the drive and control electronics, is not adequate for this application.

The connectivity among the micropackage submodules demands for a highly optimized interconnection mechanism that should feature low contact resistance, and reduced inductance and parasitic capacitance associated with transmission line effects. The interconnection techniques employed in conventional packaging often feature higher inductance or parasitic capacitance due to higher length of the bonding wires or IC pins. As a result, at high clock or operational frequencies, inductive or capacitive reactance can become significant and result in considerable signal degradation. In a large SoC, the routing distance of different signal components from one IP core to another IP core often become considerably large due to a longer global wire and may deteriorate the signal integrity considerably [26].

MEMS technology can be used to develop a micropackaging solution with highly efficient interconnection, signal integrity, mechanical protection, and thermal management features. The proposed packaging solution has a complex
design methodology due to the diverse requirements and constraints imposed on the package geometry and material composition.

The proposed packaging solution has been developed on a modular concept. A package submodule is to be fabricated out of a silicon wafer of required thickness. Using deep reactive ion etching technique, the wafer thickness is to be etched selectively to form a socket like cavity that can be used to hold one of the enabling subsystems of the overall design, e.g. a CMOS die, or the MEMS sensor microarray. Required numbers of package submodules are to be stacked vertically or horizontally. Precision alignment of the socket submodules has been ensured using precision alignment keys that are present in each of the submodules. After stacking, the package submodules are secured together by longitudinal microbolts.

Two different connectivity schemes have been developed to provide electrical interconnection among the package submodules. One is based on a pressure dependent MEMS-based cantilevered bridge-type microspring contacts utilizing with wafer-through-hole aluminum-via-interconnects and the other is by using a MEMS-based microbus card connectivity system. The details of both the schemes are described in the following sections.
5.2 Microspring Contact Based Connectivity

5.2.1 Connectivity Concept

A conceptual layout of the microspring contact based connectivity system is shown in Figure 5-1. In this scheme, a MEMS or a CMOS die is surface mounted on a package submodule. The number of other micropackage submodules is determined by the number of individual CMOS dies that are necessary to provide a mixed signal CMOS implementation of both the required analog processing of each of the sensor elements outputs, together with the associated hardware for real-time digital signal processing beamforming algorithms. One of the micropackage submodules is to hold a power supply battery. Battery technology is continually advancing and 4.0 mm or less diameter manganese lithium dioxide batteries are becoming available. All the required micropackage submodules are stacked vertically or horizontally and secured by using two longitudinal microbolts. To facilitate mounting of the sensor microarray, a slight modification of the microarray geometry is required to add two side flanges as shown in the Figure 5-1b.
Figure 5-1. Microspring contact based connectivity. (a) A cross-section of the modular micropackage. (b) Top view of the package submodule containing the surface mounted sensor microarray. (c) Top view of a package submodule containing a surface mounted CMOS die.
Each micropackage submodule has aluminum contact pads and deformable microspring contacts fabricated either on the top or on the bottom side or on both sides based on connectivity requirements. The microspring contacts provide temporary-type connectivity between dies contained in individual package submodules, whereas conventional gold wire bonding is used to establish connectivity between the contact pads on a CMOS die and the contact pads on a package submodule where the die is mounted as shown in Figure 5-1c. Wafer-through-hole aluminum via-interconnects [62] [63] provide the routing of contact paths from a submodule topside to the bottom side as can be viewed in the cross-sectional diagram shown in the Figure 5-1a. Precision alignment keys incorporated in each of the package submodules ensure proper orientation of the package submodules and allows for precision alignment of the microspring contact pads with the I/O pads on the dies in question. When the package submodules are stacked, for example vertically and secured by tightening the microbolts, developed downward pressure causes the microsprings to deform and generate necessary contact force to establish a temporary but reliable connectivity between a die pad and a microspring contact. Figure 5-2 illustrates this concept.

In this system, due to vertical integration using wafer-through-hole aluminum-via-interconnect, the length of an interconnection path between two dies is much less compared to conventional packaging systems. This significantly reduces the inductance and capacitances associated with the interconnection path and
increases signal integrity. In this manner, a complete working system can be realized in a MEMS-based micropackage.

![Diagram of MEMS die, Microspring contact, Package submodule, Aluminum via interconnect, CMOS die, Die metal pad, Passivation, Before contact, After contact](image)

**Figure 5-2. Illustration of the proposed pressure dependent microspring contact mechanism**

### 5.2.2 Microspring Contact Design Considerations

The most critical part of the proposed modular integration scheme is the design of a suitable geometry, high performance microspring contact. The design objective of the microspring contact mechanism is to develop a low-contact force, low-contact resistance, short length, high pitch, and a reliable contact mechanism that would provide temporary connectivity between the I/O pads on the dies under question. The microsprings also have to ensure elastic deformation while establishing pressure dependent connectivity among the die I/O pads. Another important requirement is to maintain a contact surface that will remain reasonably flat even under possible torsional deformation to realize a higher contact area.

Major categories of industry practiced temporary type contact mechanisms are listed in Table 5-1 [64]. Industry experience has revealed that the
establishment of temporary connectivity to a pre-deposited solder ball on a die I/O pad is becoming increasingly difficult with decreasing feature size and gives rise to new technical concerns [25] [65]. Connectivity based on using

<table>
<thead>
<tr>
<th>Contact Mechanism</th>
<th>Vendor</th>
<th>Pitch (mm)</th>
<th>Contact Force (mN)</th>
<th>Contact Resistance (mΩ)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Solder ball and spring or pogo pin</td>
<td>YAMAICHI, Synergetix, Johnstech, TI, Everett</td>
<td>0.22-1.27</td>
<td>98-686</td>
<td>5-50</td>
</tr>
<tr>
<td>Microtouch™ Conductive adhesive</td>
<td>3M</td>
<td>0.5-1.27</td>
<td>98-196</td>
<td>50</td>
</tr>
<tr>
<td>Microspring on die I/O pad</td>
<td>FormFactor</td>
<td>0.22-1.27</td>
<td>98</td>
<td>30</td>
</tr>
<tr>
<td>GoreMate™ Sacrificial layer on die I/O pad</td>
<td>Motorola</td>
<td>0.1</td>
<td>&lt;98</td>
<td>N/A</td>
</tr>
</tbody>
</table>

Microsprings on the die I/O pad exposes the active circuitry on the die to thermal and mechanical energy used to form the microsprings. Connectivity based on sacrificial layer removal, while maintaining the integrity of the aluminum I/O pad, is a critical design issue and the sacrificial layer of TiW and/or Cu must be removed completely after testing, thus adding additional manufacturing costs [65]. Due to these limitations and as none of these contact mechanisms can be integrated in MEMS-based batch fabrication process; the design of a new contact spring mechanism was explored for the proposed micropackaging solution.
Initial exploration was based on a cantilever beam with a built-in contact pad or a contact pad supported by a fixed-fixed beam type geometries due to their easy MEMS-based fabrication capabilities. However, both the geometries appeared to fall in short to meet the design requirements. A contact pad on a cantilever beam type contact spring deforms due to an applied load where the top surface of the contact pad undergoes a shear that results in a curved surface. A 3-D finite element analysis result of such a deformed cantilever beam with a conceptual die pad superimposed is shown in Figure 5-3. The Figure is zoomed 25 times in the direction of deformation for visual clarity.

Form the Figure 5-3, it is clear that while in contact, the whole pad area doesn't provide connectivity; instead a thin line contact is made resulting in a much higher contact resistance. Similar finite element analysis result shows that for a contact pad supported by a fixed-fixed beam, the top surface of the contact pad on the spring deforms into a concave surface where the contact area is limited only to the circumferential edge.
Another consideration is to determine the Z-axis displacement range for a specified elastic deformation while achieving the required contact force. The developed stress in a deformable microstructure increases with deformation due to an applied load. For a ductile material the stress in the structure at a deformed state must be less than the von Mises stress expressed as:

$$\sigma_{VM} = \left\{ \frac{1}{2} \left[ (\sigma_{p_1} - \sigma_{p_2})^2 + (\sigma_{p_2} - \sigma_{p_3})^2 + (\sigma_{p_3} - \sigma_{p_1})^2 \right] \right\}^{1/2}$$  \hspace{1cm} (5-1)

so as to ensure an elastic deformation [5-8]. In (5-1) \(\sigma_{p_1}, \sigma_{p_2}\) and \(\sigma_{p_3}\) represent the principal stresses. For a brittle material, like polysilicon, Coulomb-Mohr criterion is to be followed [35]. Polysilicon, a common MEMS structural material, due to its lower ultimate tensile strength \(\sigma_{UT}\) of 1.2 GPa [66], is unsuitable for this application. Also, the use of polysilicon requires a copper or aluminum conductive trace over it, thus adding additional fabrication steps and concerns about thermal shear stress due to different coefficients of thermal expansion of the materials. Copper has a higher ultimate tensile strength and very good electromigration and conductivity properties and appears to be the best choice. Oxidation of the exposed contacting surface of the pad can be avoided by applying a protective deposition of sputtered platinum.

5.2.3 Square-Shaped Microspring Contact

Based on these considerations, a new microspring contact geometry where a square thin copper plate with a cylindrical contact pad on the top is connected to
two vertical support pillars by four U-shaped beams has been chosen as shown in Figure 5-4.

![Support Post](image)

![Support Arm](image)

![Contact Pad](image)

**Figure 5-4. Square-shaped microspring 3-D geometry**

Due to the symmetrical long support arms holding the square thin plate supporting the contact pad, the stress developed due to an external pressure will cause a deformation of the support arms leaving a negligible or zero deformation of the contact pad itself. Thus, it will be possible to ensure an area contact under sufficient contact force. This square-shaped cantilevered bridge-type structure can be viewed as a thin isotropic square plate of side length $a$, loaded by a uniform pressure load on a circular area around the center of the contact pad, and is elastically supported by four beams of width $b$ at the edges parallel to the x-axis as shown in Figure 5-5. To simplify the analysis, the solid cylindrical contact pad on the plate can be assumed as a load mass and the total load on the plate is then the combination of the load due to the pad and the laterally applied uniform pressure on the top surface of the contact pad. Following [49], the deflection, $h$ of a thin plate due to an applied uniform load $P$ is expressed as:
Figure 5-5. Square-shaped microspring contact assumptions for analysis

\[
\frac{\partial^4 h}{\partial x^4} + 2 \frac{\partial^4 h}{\partial x^2 \partial y^2} + \frac{\partial^4 h}{\partial y^4} = \frac{P}{D}
\]  \hspace{1cm} (5-2)

where \( D \) is the flexural rigidity of the plate expressed as:

\[
D = \frac{Et_d^3}{12(1-\nu^2)}
\]  \hspace{1cm} (5-3)

where \( E \) is the modulus of elasticity of the plate material, \( \nu \) is the Poisson’s ratio and \( t_d \) is the plate thickness. The deflection profile of such a partially loaded square diaphragm supported by four elastic beams at the corners can be carried out using analytical methods described in [5-10] by applying necessary boundary conditions.

The International Technology Roadmap for Semiconductors (ITRS), 1999 edition, indicated a requirement for a 75x75 \( \mu m^2 \) pad size and a pad pitch of 150 \( \mu m \) as a near-term (year 2005) goal [38]. To satisfy this requirement, a foot print
area of 100x100 \( \mu \text{m}^2 \) is chosen for the microspring contact. The side length of the square plate is chosen as 60 \( \mu \text{m} \) to facilitate a width of 10 \( \mu \text{m} \) for the support beams and a radius of 20 \( \mu \text{m} \) is chosen for the cylindrical contact pad to provide a good tolerance while aligned with a 75x75 \( \mu \text{m}^2 \) pad. Copper is chosen for its higher ultimate tensile strength, excellent electrical conductivity and electromigration properties. With the material chosen and dimensions fixed, the load deflection characteristic of the structure is now dependent on the thickness of the square plate and the beams and the height of the contact pad. A few micrometers thick copper layers are now possible to deposit using sputtering process and electrodeposition of copper is the preferred method to realize higher thickness copper structures. A thickness of two micrometers for the support beams and the square diaphragm and a five micrometers thick contact pad was chosen as initial thickness.

For an externally applied load of 1.35 mN, the IntelliSuite™ 3-D finite element analysis result shows that the maximum Z-axis displacement of the contact pad is 5.0 \( \mu \text{m} \) (Figure 5-6a). At maximum displacement, the von Mises stress is 1.47 GPa, which is approximately half of the yield strength of copper (2.80 GPa) [25] (Figure 5-6b). This ensures that the deflection of microspring geometry under the specified force is within the elastic limit of copper and allows for a reasonable safety margin. From the result of the FEA analysis shown in Figure 5-6a, it is also evident that the shear deformation of the contact pad is negligible and the top surface of the contact pad remains reasonably flat to ensure an area as opposed to a line contact, thus satisfying the required design criteria.
Figure 5-6. FEA simulation results of the square-shaped microspring contact. (a) Z-axis displacement. (b) von Mises stress.
5.2.4 Z-Shaped Microspring Contact

A higher contact force supporting Z-shaped microspring contact is shown in Figure 5-7. The Z-shaped microspring contact has the same footprint area and contact pad size as the square-shaped one, however, the contact pad height and the support beam thickness are increased. In addition to realizing a higher contact force, the complex curved cantilever support beams allows for torsional stability within a tolerance limit while establishing an area based die pad-spring connectivity. An analysis similar to the one for the square-shaped microspring contact can be carried out for the Z-shaped contact spring structure assuming a circular thin plate is uniformly loaded and is supported elastically on two sides for a small distance along the circumference by a complex curved cantilever beam [67]. The FEA simulation results of the Z-shaped microspring contact are shown in Figure 5-8. At an applied load of 5.0 mN, the maximum displacement of the contact pad is 4.79 μm and maximum von Mises stress is about 1.46 GPA.

Figure 5-7. Z-shaped microspring contact 3-D geometry
Figure 5-8. FEA simulation results of the Z-shaped microspring contact. (a) Z-axis displacement. (b) von Mises stress.
Table 5-2. Cantilevered bridge-type microsprings design specifications

<table>
<thead>
<tr>
<th>Design Parameter</th>
<th>Microspring specifications</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>Square-shaped</td>
<td>Z-shaped</td>
</tr>
<tr>
<td>Spring footprint area</td>
<td>100 x 100</td>
<td>100 x 100</td>
</tr>
<tr>
<td>Square thin plate area</td>
<td>60 x 60</td>
<td>-</td>
</tr>
<tr>
<td>Contact pad radius</td>
<td>20</td>
<td>20</td>
</tr>
<tr>
<td>Contact pad height</td>
<td>5</td>
<td>10</td>
</tr>
<tr>
<td>Support arm length</td>
<td>70</td>
<td>164</td>
</tr>
<tr>
<td>Curved beam radius</td>
<td>-</td>
<td>30</td>
</tr>
<tr>
<td>Support arm thickness</td>
<td>2</td>
<td>5</td>
</tr>
<tr>
<td>Support arm width</td>
<td>10</td>
<td>20</td>
</tr>
<tr>
<td>Contact force</td>
<td>1.35</td>
<td>5</td>
</tr>
<tr>
<td>Contact resistance</td>
<td>18.8</td>
<td>12.1</td>
</tr>
<tr>
<td>Max. Z-axis displacement</td>
<td>5</td>
<td>4.79</td>
</tr>
<tr>
<td>Max. von Mises stress</td>
<td>1.47</td>
<td>1.46</td>
</tr>
<tr>
<td>Platinum coating</td>
<td>100</td>
<td>100</td>
</tr>
</tbody>
</table>

Detailed design specifications of both the microspring contacts are given in Table 5-2. Figure 5-9 shows the deformed Z-shaped microspring contact after simulation with a conceptual die pad superimposed that shows that the microspring and the die pad connectivity results in an area type contact due to the reasonably flat top surface of the contact pad on the microspring.
5.3 Microbus Card Connectivity System

5.3.1 System Description

In this connectivity scheme, individual die-holding package submodules are fabricated out of silicon wafers of required thickness and the connectivity between the micropackage submodules, including the sensor microarray die is achieved by using a MEMS-based microbus card. The developed microbus card is basically a removable insert carved out of a silicon wafer having cantilevered microspring contacts fabricated on it using MEMS technology.

In this scheme, the MEMS sensor microarray itself constitutes a package submodule. To accommodate this capability, the microarray fabrication processes as described in Chapter 4 is slightly modified. A top view of the modified MEMS sensor microarray die is shown in Figure 5-10a. All the required micropackage submodules are stacked vertically or horizontally and secured by using two longitudinal microbolts as described in the previous section. A cross-section of the micropackage through the plane A-A’ is shown in Figure 5-10b.
Figure 5-10. The geometry of the MEMS sensor microarray is modified to facilitate microbus-based connectivity. The sensor microarray itself now constitutes a package submodule. (a) Topview of the modified sensor microarray die. (b) Cross section through the plane A-A' as defined in Figure 5-10a.
All of the micropackage submodules, including the sensor microarray, have prefabricated interconnection channel(s). When the submodules are stacked, for example vertically, the interconnection channels in each of the submodules align up and fit to form a long contiguous channel. The interconnection channel(s) in a package submodule have electrical contacts in the form of long vertical microrails coated with a durable conductive material, e.g., platinum. Each microrail contact is connected to an aluminum contact pad in the micropackage submodule through insulated buried copper trace. Gold bonding wires provide connectivity among die I/O pads and the micropackage submodule metal pads.

A top view of a CMOS die container package submodule is shown in Figure 5-11a. Different CMOS die container submodules may contain dies fabricated out of different technologies, thus adding flexibility in using existing SoC IP cores that are available in different technology layouts.

After securing the package submodules in a stack, the microbus card has to be inserted in the interconnection channel to establish connectivity among the package submodules. A cross-section through the plane B-B' in Figure 5-11a is shown in Figure 5-11b to illustrate inter-modular connectivity. The connectivity mechanism using cantilevered microspring contacts formed on one or both sides of the microbus card is illustrated in Figure 5-12. When inserted in the interconnection channel, the bent microsprings will push against the microrail inside the interconnection channel to cause further deformation to generate the required contact force that is required to establish the necessary connectivity. Gold-coated polysilicon cantilever microspring contacts on a microbus card are
Figure 5-11. Microbus based connectivity system. Connectivity between a CMOS die pad and a micropackage pad is achieved by using a gold bonding wire. Platinum coated microrails inside an interconnection channel are connected to pads on a micropackage submodule through copper traces. (a) Top view of a CMOS die container micropackage submodule. (b) Cross-sectional view through the plane B-B' as defined in Figure 5-11a.
Figure 5-12. Illustration of cantilevered microspring connectivity inside an interconnection channel

arranged in a matrix form where an element (microspring) of each row connects to a corresponding microrail contact in a package submodule while the elements of each column are connected to an aluminum bus that runs along the whole length of the microbus card. The aluminum bus can be configured during fabrication process to establish selective connectivity among the submodules. Gold-coated polysilicon microspring contacts are heat-treated to introduce more stress in addition to residual stress accumulated during the fabrication process to bend further, thereby to generate a higher contact force.

5.3.2 Package Submodule Design

The substrate thickness of a conventional CMOS die is generally reduced by polishing before packaging. It is possible to have CMOS dies with a substrate thickness in between 50-100 μm. Thus, the CMOS die housing pit depth in a package submodule should be at least 100 μm. About 100 μm gap above a
CMOS die and package contact pad is necessary to provide sufficient space for gold bonding wire and air ventilation. Assuming a 400 μm thick commercially available silicon substrate is used to fabricate a micropackage submodule, the bottom deck thickness of 100 μm is chosen for a submodule so that at least 100 μm space can be used for overlapping when the submodules are stacked. In the interconnection channel, 25 μm wide, 50 μm pitch microrails are to be formed by DRIE process. The width of the microrail matches the width of the cantilevered microspring contacts on the microbus card. A spacing of 25 μm results from the consideration of accommodating higher number of contacts while minimizing the possibility of cross talk due to inductive and capacitive coupling between the microrails. Silicon dioxide insulated buried copper traces connecting the microrails and the package pads reduce the inductive and capacitive coupling between the copper traces to a minimum. A height of 1.0 μm for the copper lines was chosen to reduce resistivity.

A precision alignment key for the micropackage submodules is vital for stacking the submodules in the desired orientation. A triangular alignment key is chosen for this purpose. To ensure, proper orientation of the microbus card inside the interconnection channel, two asymmetrical vertical notches are included in each interconnection channel that conforms to two alignment keys fabricated in each microbus card. Detailed dimensions of a CMOS die container package submodule are given in Table 5-3.
Table 5-3. Micropackage submodule design specifications

<table>
<thead>
<tr>
<th>Design Parameter</th>
<th>Value</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Thickness of a package submodule:</td>
<td>400</td>
<td>μm</td>
</tr>
<tr>
<td>Depth of CMOS die housing pit:</td>
<td>100</td>
<td>μm</td>
</tr>
<tr>
<td>Thickness of bottom deck:</td>
<td>100</td>
<td>μm</td>
</tr>
<tr>
<td>Microrail contact height:</td>
<td>300</td>
<td>μm</td>
</tr>
<tr>
<td>Aluminum contact pad area:</td>
<td>75 x 75</td>
<td>μm²</td>
</tr>
<tr>
<td>Microbolt diameter:</td>
<td>400</td>
<td>μm</td>
</tr>
<tr>
<td>Interconnection channel width</td>
<td>2</td>
<td>mm</td>
</tr>
<tr>
<td>Interconnection channel thickness</td>
<td>400</td>
<td>μm</td>
</tr>
</tbody>
</table>

5.2.3 Package Submodule Fabrication

In this section, the process steps associated with the fabrication of a single micropackage submodule with the interconnection channels have been described. For better visualization and understanding the thickness and widths of some layers have been exaggerated. Some common but necessary steps like Piranha or RCA cleaning, photoresist curing, solvent removing, promoter layers, etc. have been omitted while major fabrication steps are highlighted. The complete fabrication process sequences have been grouped into eight steps and are described below. Due to symmetry, only a section of the package geometry is used to illustrate the fabrication process.
**Step 1**

![Diagram of Micropackage Submodule Fabrication: Step 1](image)

**Figure 5-13. Micropackage submodule fabrication: Step 1**

A 70 nm thick silicon nitride layer is deposited on the top of a 400 μm thick Czochralski silicon wafer by a plasma enhanced chemical vapor deposition (PECVD) method. The nitride layer is then patterned and dry etched. Three layers of aluminum-negative photoresist laminations are deposited, patterned and etched on the front side of the wafer.

**Step 2**

![Diagram of Micropackage Submodule Fabrication: Step 2](image)

**Figure 5-14. Micropackage submodule fabrication: Step 2**

$O_2$ ashing of the negative photoresist is carried out by inductively coupled plasma-reactive ion etching (ICP-RIE) method. The wafer is then successively ICP-RIE etched using aluminum and negative resist laminations as delayed mask [68]. Figure 5-14 shows the result of ICP-RIE etch using the top aluminum mask.
Step 3

Figure 5-15. Micropackage submodule fabrication: Step 3

After the 3rd ICP-RIE process using aluminum and negative photoresist as a delayed etch mask, the wafer patterning is completed. The 3rd aluminum mask is then stripped. The figure shows the wafer after completion of the 3rd ICP-RIE process.

Step 4

Figure 5-16. Micropackage submodule fabrication: Step 4

A 70 nm thick Silicon nitride layer is then deposited on the wafer backside by PECVD method and patterned. Thermal oxide is grown on both sides of the wafer and patterned.
Step 5

Figure 5-17. Micropackage submodule fabrication: Step 5

The PECVD silicon nitride on the wafer topside is then removed. The wafer is then wet etched using tetramethyl ammonium hydroxide (TMAH) to form the slant edge on the top. The wafer front side is then RIE etched to from 1.2 μm deep by 35 μm wide trenches. A 70 nm thick low temperature oxide is then grown on the wafer topside including the deep trench. The LTO layer is then patterned and etched dry using SF6/O2 plasma.

Step 6

Figure 5-18. Micropackage submodule fabrication: Step 6

A 70 nm thick tantalum layer is then deposited on the wafer topside by a DC magnetron sputtering process and patterned in the shallow trenches. Afterwards, 1.0 μm thick copper is sputtered and patterned over the tantalum layer. Finally a 0.2 μm thick silicon dioxide is PECVD deposited over the copper trace to protect the copper traces from oxidation.
Step 7

Figure 5-19. Micropackage submodule fabrication: Step 7

75x75 μm² aluminum contact pads are then formed by e-beam evaporation of 1.0 μm thick aluminum and wet etching. 200 nm thick platinum is next sputter deposited in the interconnection channel and patterned using an electrodeposited photoresist.

Step 8

Figure 5-20. Micropackage submodule fabrication: Step 8

Wafer backside nitride is next stripped. Anisotropic etching is performed on the wafer backside using TMAH to complete the fabrication process.

The above fabrication process steps have been simulated using the IntelliSuite™ and the resulting 3-D model of a micropackage submodule is given in Figure 5-21.
Figure 5-21. 3-D model of a micropackage submodule generated by simulating the described fabrication process steps using IntelliSuite™
5.4 Microbus Card Design

MEMS technology is used to fabricate the microbus card. Gold-coated polysilicon cantilever microspring contacts on the microbus card are arranged in a matrix form where an element (microspring) of each row connects to a corresponding microrail contact in a micropackage submodule while the elements of each column are connected to an aluminum bus that runs along the whole length of the microbus card. The aluminum bus can be configured during fabrication process to establish selective connectivity among the submodules. High residual stress levels are desirable for the polysilicon microspring contacts since increased deformation will result in increased contact force that will decrease the contact resistance. For this reason, the polysilicon cantilever springs are required to be heat treated after releasing the cantilever structures during fabrication process to introduce additional stress [69]. The thickness of the microbus card is dependent on the available dimensions of the interconnection channel. The dimensions and locations of the interconnection channel in a micropackage submodule are necessary to be optimized to minimize the routing trace lengths for all the micropackage submodules in the stack. The optimum dimensions and geometry (square, rectangular or circular) of a micropackage submodule is determined by the available application area and die size. To comply with commercially available silicon wafers and limitations of the DRIE fabrication process technologies, a thickness of 400 µm for the microbus card substrate is determined. To provide sufficient tolerance in the vertical direction and a good width to length ratio, a 100 µm length for a
polysilicon cantilever spring is chosen (height of the interconnection channel is 300 μm). A 50 μm pitch for the cantilever microsprings with a spacing of 25μm is selected to conform to the microrail contacts in the interconnection channel. A thickness of 1.0 μm for the aluminum bus is chosen to provide reduced resistance.

The tip deflection of a bimorph cantilever beam (gold-polysilicon) can be expressed as [70]:

\[
\delta_s = \frac{3B_{s1}B_{s2}E_{s1}E_{s2}t_{s1}t_{s2}(t_{s1} + t_{s2})(\alpha_{s2} - \alpha_{s1})\Delta T L_s^2}{(E_{s1}B_{s1}t_{s1}^2)^2 + (E_{s2}B_{s2}t_{s2}^2)^2 + 2B_{s1}B_{s2}E_{s1}E_{s2}t_{s1}t_{s2}(2t_{s1}^2 + 3t_{s1}t_{s2} + 2t_{s2}^2)}
\]  

(5-4)

where, \(B_s\) is the width, \(E_s\) is the Young's modulus, \(t_s\) is the thickness, \(\alpha_s\) is the coefficient of thermal expansion, and \(L_s\) is the length of the cantilever beam. Suffix 1 and 2 refer to the polysilicon and the gold layers respectively (Figure 5-12).

The equivalent spring constant of the bimorph beam can be expressed as [69]:

\[
K_{eq} = \left(\frac{3}{L_s^3}\right) \frac{t_{s1}t_{s2}B_{s2}E_{s1}E_{s2}}{12(E_{s1}t_{s1} + E_{s2}t_{s2})} \left(k_s\right)
\]  

(5-5)

where,

\[
k_s = \left[4 + 6 \frac{t_{s2}}{t_{s1}} + 4 \left(\frac{t_{s2}}{t_{s1}}\right)^2 + \frac{E_{s2}}{E_{s1}} \left(\frac{t_{s2}}{t_{s1}}\right)^3 + \frac{E_{s1}t_{s1}}{E_{s2}t_{s2}}\right]
\]  

(5-6)
Thus, the contact force (spring force) can be expressed as:

$$ F_{\text{contact}} = K_{eq} \delta_s $$  \hspace{1cm} (5-7)

To evaluate the contact resistance, it is required to find the effective contact area following Hertzian contact area evaluation method as given in the following equation:

$$ A_{\text{eff}} = \sqrt[3]{ \frac{3}{4} F_{\text{contact}} \left( \frac{1 - \nu_1^2}{E_1} + \frac{1 - \nu_2^2}{E_2} \right) \left( \frac{1}{r_{c1}} + \frac{1}{r_{c2}} \right)^{-1} } $$  \hspace{1cm} (5-8)

where, $\nu$, $E$ and $r_c$ refer to Poisson's ratio, Young's modulus and the radius of the actual contacting surfaces, $A_{\text{eff}}$ is the effective area of contact and $F$ represents the contact force. The contact resistance $R_c$ then can be evaluated from the following expression:

$$ R_c = \frac{\rho}{2 A_{\text{eff}}} $$  \hspace{1cm} (5-9)

where $\rho$ is the resistivity of the contact members. Thermomechanical simulation of one of the cantilevered microspring contact was carried out using IntelliSuite™ mechanical simulation module. The simulation results are shown in Figure 5-22.

Table 5-3 summarizes the design specifications for a microbus card designed for use in a hearing instrument.
Figure 5-22. (a) FEA result showing the deflection profile of a gold-coated polysilicon microspring contact after performing heat treatment at 160 °C. (b) Deformed shape of the microspring contact. The spring bends upwards in the +Z direction due to increased stress.
Table 5-4. Microbus card design specifications

<table>
<thead>
<tr>
<th>Design Parameters</th>
<th>Value</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Cantilever microspring dimensions (L x W x T):</td>
<td>100 x 25 x 2.5</td>
<td>μm³</td>
</tr>
<tr>
<td>Gold conductor thickness:</td>
<td>500</td>
<td>nm</td>
</tr>
<tr>
<td>Polysilicon thickness:</td>
<td>2</td>
<td>μm</td>
</tr>
<tr>
<td>Aluminum bus dimensions (W x T):</td>
<td>25 x 1</td>
<td>μm²</td>
</tr>
<tr>
<td>Rectangular retaining clip Insertion hole:</td>
<td>250 x 250</td>
<td>μm²</td>
</tr>
<tr>
<td>Microbus card width</td>
<td>2</td>
<td>mm</td>
</tr>
<tr>
<td>Microbus card thickness</td>
<td>400</td>
<td>μm</td>
</tr>
<tr>
<td>Microspring tip deflection at 200 °C:</td>
<td>6</td>
<td>μm</td>
</tr>
<tr>
<td>Contact force per microspring:</td>
<td>31</td>
<td>μN</td>
</tr>
<tr>
<td>Contact resistance per microspring:</td>
<td>248</td>
<td>mΩ</td>
</tr>
</tbody>
</table>

5.4.1 Microbus Card Fabrication

In this section, the process steps associated with the fabrication of a microbus card have been described. For better visualization and understanding the thickness and widths of some layers have been exaggerated. Some common but necessary steps like Piranha or RCA cleaning, photoresist curing, solvent removing, promoter layers, etc. have been omitted while major fabrication steps are highlighted. The whole fabrication process sequences of the microbus card have been grouped into seven steps and are described below:
Step 1

A 70 nm thick silicon nitride layer is deposited on the backside of a 400 μm thick Czochralski silicon wafer by a PECVD method. A 200 μm thick aluminum layer is then deposited on the wafer topside using E-beam evaporation method. The aluminum layer is then patterned using a negative photoresist and etched dry using \( \text{Cl}_2 \). The wafer is then etched dry using inductively coupled plasma-reactive ion etching (ICP-RIE) method using the top aluminum layer as the etch mask through all the thickness to create the grip openings and the holes for rectangular retaining clip at the bottom. Silicon nitride layer on the wafer backside is then patterned and etched selectively. The wafer is then patterned again with an aluminum mask and etched to create the alignment keys on the two lateral sides. Aluminum masks on the wafer top and backside are then stripped.

Step 2

The wafer topside is then patterned using a photoresist and etched dry using \( \text{SF}_6 \) plasma to create required number of 27 μm wide, 1.2 μm deep trenches.
Figure 5-24. Microbus card fabrication: step 2

A 30 nm thick LPCVD silicon nitride layer is then deposited in the trenches which is followed by deposition of a 1.0 μm thick layer of E-beam evaporated aluminum. The aluminum layer is then patterned and wet etched to create 25 μm wide aluminum bus. The result of this process step is shown in Figure 5-24.

Step 3

Figure 5-25. Microbus card fabrication: Step 3

A 2 μm thick layer of silicon oxide is then deposited on the wafer topside by PECVD process. The oxide layer is then patterned with a photoresist and etched dry. The result of this process step is shown in Figure 5-25.
Step 4

Figure 5-26. Microbus card fabrication: Step 4

A 2 μm thick layer of polysilicon is then deposited over the patterned thermal oxide. The polysilicon layer is patterned using a photoresist and etched dry to create the arrays of cantilever beam structures. In the Figure 5-26, two of the polysilicon cantilever structures are shown.

Step 5

Figure 5-27. Microbus card fabrication: Step 5

The thermal oxide layer is then etched dry using SF₆ plasma as shown in Figure 5-27 above.
Step 6

A 500 nm thick layer of gold is then E-beam evaporated over the polysilicon cantilever beam array structures using a 30 nm thick layer of chromium as an adhesion layer. The gold layer is then patterned and lifted-off as shown in Figure 5-28.

Step 7

Figure 5-28. Microbus card fabrication: step 6

Figure 5-29. Microbus card fabrication: step 7
The oxide layer is then wet etched sacrificially using a buffered oxide etch (BOE). Finally, the whole structure is heat treated at 160°C to introduce thermal stress that bend the polysilicon cantilever beams upwards as shown in Figure 5-29.

Figure 5-30 shows the 3-D model of the microbus card before heat treatment generated by IntelliSuite™ after simulating the developed fabrication processes. The slots at the microbus card top enables it to be inserted or removed using a micro grip and bottom slots are to be used for a rectangular retaining clip to hold the card in position against any vibrational or acceleratory motion. Figure 5-31 shows a 3-D illustration of stacked micropackage submodules including the sensor microarray. Figure 5-32 shows a blow-up view of the interconnection channel along with the microbus card that illustrates the connectivity between gold-coated polysilicon cantilever springs and platinum coated microrail contacts inside the interconnection channel.
Figure 5-30. 3-D model of the microbus card before heat treatment
Figure 5-31. Illustration of vertical stacking of the micropackage submodules using IntelliSuite™ generated 3-D models of the micropackage submodules and the sensor microarray after simulating the fabrication processes.
Figure 5-32. Illustration of microbus card connectivity using IntelliSuite™ generated 3-D models of the interconnection channel and the microbus card after simulating the fabrication processes.
5.5 Electrical Analysis of the Microbus Card Connectivity System

In this section, the electrical characteristics of a single interconnect path between two adjacent micropackage submodules is evaluated. Electrical performance of interconnects between non-adjacent submodules can be evaluated using a similar procedure as in those cases only the length of the aluminum bus on the microbus card will vary while all the other circuit components will remain the same.

It is assumed that a mixed signal implementation is necessary to carry out all the required signal processing that may include, capacitive readout, signal conditioning, Sigma-delta A/D conversion, beamforming and digital signal processing. High clock rate switched capacitor circuits will be required for capacitive readout and also for biasing of the opamp to be used in the charge integrator for reliable and stable operation. Thus, the interconnection path must provide sufficient signal integrity while routing a high-speed signal from one package submodule to another while keeping the effects of the frequency variant circuit parameters to a minimum.

The micropackage interconnects should be modeled as on-chip interconnects instead of PCB interconnects as the micropackage interconnects are being fabricated on a silicon wafer like conventional IC interconnects. The frequency dependent losses (skin effect and dielectric losses) of the circuit parameters become significant for high-speed, high frequency signals. Substrate
conductance becomes significant at high frequencies and cannot be neglected. Fringe field capacitance and change of capacitance due to dielectric loss of the dielectric materials at high frequencies must be accounted for to evaluate the high frequency response.

A drawing of an interconnection path between two adjacent micropackage submodules is shown in Figure 5-33. For a high-speed signal with a clock rate of 10 GHz, the propagation delay through an interconnect on a micropackage submodule is greater than the pulse rise time (10 ps). Thus, the buried microstrip model of transmission line is necessary to adopt to carry out the electrical analysis of a micropackage interconnect through the length of the copper trace parallel to the substrate [71]. The vertical trace at the inner wall of the package submodule and the platinum conductor inside an interconnection channel should be modeled as a via [71]. The signal path through the length of the microbus card should also be modeled as a microstrip transmission line. Pads on the package submodule and the die pads are to be modeled as capacitances while a gold bonding wire should be modeled as an inductor [71]. A via should be modeled as an inductor as well [71]. Thus the electrical equivalent circuit of the interconnect path as shown in Figure 5-33 can be schematically drawn as shown in Figure 5-34. $Z_{01}$ represents the characteristic impedance of an interconnect on the package submodule and $Z_{02}$ represents the characteristic impedance of a microbus card interconnect. Due to short length, the cantilever microspring contact is assumed to contribute as an inductance.
Figure 5-33: Connectivity path between two adjacent micropackage submodules

Figure 5-34: Electrical circuit representation of the connectivity path
Figure 5-35. RLCG conversion of the micropackage interconnect

First step of the analysis is to evaluate the characteristic impedances associated with the microstrip transmission line models, viz. $Z_{01}$ and $Z_{02}$.

The equivalent distributed circuit model of a transmission line consists of an infinite number of RLCG segments as shown in Figure 5-35. For practical purposes, a sufficient number of RLCG segments can be determined based on the minimum rise time and fall time as given as [71]:

$$\text{Segments} \geq 10 \left( \frac{x}{T_r v_p} \right)$$  \hspace{1cm} (5-10)

where $x$ is the length of the transmission line, $T_r$ is the signal rise time and $v_p$ is the propagation velocity. The rise or fall time is defined as the amount of time it takes a signal to transition between its minimum and maximum magnitude. Rise times are typically measured between the 10% and 90% values of the maximum swing. While simulating a digital system, it is usually sufficient to choose the
values so that the time delay ($TD = \sqrt{LC}$) of the shortest RLCG segment is no larger than one-tenth of the system minimum rise time or fall time that arises from the condition specified in equation (5-10). Following the above method, it was found that the $Z_{01}$ will have 5 (five) RLCG segments and $Z_{02}$ will have 3 (three) RLCG segments and the characteristic impedance of a buried microstrip line was evaluated as 167 $\Omega$. Thus, it is now required to evaluate the frequency dependent resistance, inductance, capacitance, and conductance associated with the RLCG segments.

To evaluate frequency variant parameters, the buried microstrip transmission line shown in Figure 5-36, is modeled as an equivalent electrical circuit as shown in Figure 5-37. In the figure, $C_1$ represents the oxide capacitance, $C_2$ represents the capacitance of the substrate, and $G_s$ represents the substrate conductance. The objective now is to model the circuit of Figure 5-37 into the RLCG model as shown in Figure 5-35 while incorporating frequency variant parameters [71].
5.5.1 Frequency Variant Resistance Modeling

As frequency increases, conductor resistance becomes controlled by the skin effect. For microstrip, the DC resistance per unit length of a single trace is given by [72]:

\[ R_{DC} = \frac{\rho}{w t_{lc}} \]  \hspace{1cm} (5-11)

where \( \rho \), \( w \), and \( t_{lc} \) represent the resistivity, width, and the thickness of the conductor, respectively.

The onset of skin effect occurs when the skin depth is equal to the thickness of the conductor at a frequency, \( f_{\text{skin}} \), as given by:

\[ f_{\text{skin}} = \frac{\rho}{t_{lc}^2 \pi \mu_0} \]  \hspace{1cm} (5-12)

Using \( R_{DC} \) and \( f_{\text{skin}} \), the resistance per unit length above \( f_{\text{skin}} \) is given by [73]:
\[ R_{AC} = r_s (1 + j) \sqrt{\omega} \quad (5-13) \]

where:

\[ r_s = \frac{2R_{DC}}{\sqrt{2\pi} \sigma_{\text{skin}}} \quad (5-14) \]

The factor of 2 is added to approximate the resistance of the return path. Thus, the total frequency variant resistance per unit length can now be expressed as:

\[ R_{\text{total}} = \sqrt{R_{DC}^2 + R_{AC}^2} \quad (5-15) \]

The calculated variation of the resistance with frequency for a micropackage RLCG segment is given in Figure 5-38.

### 5.5.2 Frequency Variant Inductance Modeling

The self inductance of a rectangular interconnect line of length \( l \) without skin effect is given by:

\[ L = \frac{\mu l}{2\pi} \left[ \ln \frac{2l}{w + t_c} + \frac{w + t_c}{4l} + .5 \right] \quad (5-16) \]

where \( \mu = \mu_0 \mu_r \) represents magnetic permeability. At high frequency, the skin depth is given by

\[ \delta = \frac{\rho}{\sqrt{\pi \nu \mu}} \quad (5-17) \]
The frequency dependent inductance, thus can be given by [73]:

$$L_{\text{skin}} = \frac{\mu l}{2\pi} \left[ \ln \frac{2l}{w + t_{ic}} + .5 + \frac{w + t_{ic}}{4l} + .028 \ln \frac{\min(w, t_{ic}, \delta)}{\min(w, t_{ic})} \right]$$

(5-18)

The variation of the inductance with frequency is given in figure 5-39.

![Resistance Variation with Frequency](image)

Figure 5-38: Variation of resistance with frequency
Figure 5-39: Variation of inductance with frequency
5.5.3 Capacitance and Conductance Modeling

Following [74], the DC (static) capacitance between a rectangular conductor and insulated substrate separated by a dielectric as shown in Figure 5-36 can be expressed as:

\[ C = \varepsilon \left[ \frac{w}{h_{ic}} + 0.77 + 1.06 \left( \frac{w}{h_{ic}} \right)^{0.25} + 1.06 \left( \frac{t_{ic}}{h_{ic}} \right)^{0.5} \right] \]  \hspace{1cm} (5-19)

However, at high frequencies, dielectric loss changes the dielectric constant and thus affects a change in the capacitance between the conductor and the substrate. As the dielectric constants of the substrate and the silicon dioxide insulation layer are in series, the average dielectric constant \( \varepsilon_r \) is given by [75]:

\[ \varepsilon_r = \frac{\varepsilon_{r1} \varepsilon_{r2}}{\varepsilon_{r1} + \varepsilon_{r2}} \]  \hspace{1cm} (5-20)

Thus, the effective dielectric constant for a microstrip is calculated as [5-17]:

\[ \varepsilon_{eff} = \frac{\varepsilon_r + 1}{2} + \frac{\varepsilon_r - 1}{2} \left( 1 + \frac{12h_{ic}}{w} \right)^{-2} + F - 0.217(\varepsilon_r - 1) \frac{t_{ic}}{\sqrt{wh_{ic}}} \]  \hspace{1cm} (5-21)

where

\[ F = \begin{cases} 
0.02(\varepsilon_r - 1) \left( 1 - \frac{w}{h_{ic}} \right)^2 & \text{for } \frac{w}{h_{ic}} < 1 \\
0 & \text{for } \frac{w}{h_{ic}} > 1 
\end{cases} \]  \hspace{1cm} (5-22)
For a buried microstrip as shown in Figure 5-36, the effective dielectric constant in further modified as [76]:

\[
\varepsilon_{\text{eff-buried}} = \varepsilon_{\text{eff}} e^{(-2b_{lc}/h_{lc})} + \left[1 - e^{(-2b_{lc}/h_{lc})}\right]
\]  

(5-23)

where \( b_{lc} \) refers to the height of the dielectric layer as shown in Figure 5-36.

Thus the static capacitance for a buried microstrip following equation (5-19) is necessary to express as:

\[
C = \varepsilon_{\text{eff-buried}} \left[ \frac{w}{h_{lc}} + 0.77 + 1.06 \left(\frac{w}{h_{lc}}\right)^{0.25} + 1.06 \left(\frac{t_{lc}}{h_{lc}}\right)^{0.5} \right]
\]  

(5-24)

Following Figure 5-36, the substrate conductance is given by [75]:

\[
G_s = \frac{\sigma_{si} \left[1 + (1 + 10h_2/w)^{-1/2}\right]}{2F(h_2, w)}
\]  

(5-25)

where: \( \sigma_{si} \) is the conductivity of the substrate and

\[
F(h_2, w) = \begin{cases} 
\frac{1}{2\pi} \ln(8h_2/w + w/4h_2) & \text{for } h_2/w \geq 1 \\
\frac{1}{w/h_2 + 2.42 - 0.44h_2/w + (1 - h_2/w)^6} & \text{for } h_2/w \leq 1 
\end{cases}
\]  

(5-26)

The capacitances, \( C_1 \) and \( C_2 \) in Figure 5-37 can be evaluated following equation (5-24). After manipulation, the frequency dependent capacitance per unit length of an RLCG segment can be expressed as:
\[ C = \frac{\omega^2 C_1 C_2 (C_1 + C_2) + C_1 G_s^2}{G_s^2 + \omega^2 (C_1 + C_2)^2} \tag{5-27} \]

The frequency dependent conductance can be expressed as:

\[ G = \frac{\omega^2 C_1^2 G_s}{G_s^2 + \omega^2 (C_1 + C_2)^2} \tag{5-28} \]

Figures 5-40 and 5-41 show the plots of the capacitance and conductance calculated following equations (5-27) and (5-28) for a RLCG segment of a buried microstrip line for different frequency values.

### 5.5.4 Time Domain and Frequency Domain Response

The propagation constant of a transmission line is expressed as:

\[ \gamma = \sqrt{(R + j\omega L)(G + j\omega C)} \tag{5-29} \]

And the frequency domain transfer function of the transmission line is expressed as:

\[ H(\omega) = e^{-\gamma} \tag{5-30} \]
Figure 5-40: Variation of capacitance with frequency
Figure 5-41: Variation of conductance with frequency
A well-behaved step function can be defined as [72]:

\[ g = \frac{1}{2} (1 + \text{erf}(b_1(t - t_1))) \]  \hspace{1cm} (5-31)

where, \( t_1 \) and \( b_1 \) are parameters giving the starting time and the steepness of the step respectively. A pulse can be defined as the difference between two step functions with different starting times. This input function is then Fourier transformed to \( G(\omega) \) and combined with the transmission line response function \( H(\omega) \) to form the output response \( H(\omega)G(\omega) \). Finally, the time domain output response is found from the inverse Fourier transform of \( H(\omega)G(\omega) \). Figure 5-42 shows the time domain response of an interconnect line to a 10 GHz pulse and Figure 5-43 shows the frequency response. From the figures it is evident that the signal attenuation up to 10 GHz is very low, thus ensuring that the electrical performance of the micropackage provides excellent signal integrity at frequencies up to 10 GHz.

Similar analysis can be carried out to evaluate signal integrity for higher number of package submodules. In those cases, on the transmission line segments in the microbus card will be higher whereas all other parameters will remain the same.
Figure 5-42: 10 GHz pulse Response
Figure 5-43: Frequency response of the micropackage interconnect
5.6 Summary

The design of a MEMS-based modular micropackaging solution for the sensor microarray is presented. The silicon-based modular micropackaging solution enables reliable non-permanent electrical integration of the sensor microarray to the microelectronics circuitry and a power supply while providing a robust mechanical protection and excellent thermal management. Two different schemes of electrical interconnectivity have been demonstrated. The first scheme uses cantilevered bridge-type microspring contacts using wafer-through-hole aluminum-via-interconnects to establish the necessary electrical connectivity among the sensor microarray and the microelectronics circuitry and a power supply that are contained in different micropackage submodules. Two different types of microspring contacts are designed. The square-shaped contacts are designed for a low force application (1.35 mN/microspring) while the Z-shaped contacts can support higher force (5 mN/microspring). Both the springs exhibit excellent stability, low contact resistance and conform to the International Technology Roadmap for Semiconductors (ITRS), 1999 edition recommendations. The second scheme is based on a novel MEMS-based microbus card connectivity system to establish the necessary intermodular electrical connectivity. The microbus card, which is a removable insert, establishes connectivity between package submodules when inserted in an interconnection channel that is present in each of the package submodules. Detailed design, simulation and fabrication of the structures have been presented.
Chapter 6

Conclusions

A design methodology and fabrication procedures for a MEMS-based square planar acoustical sensor microarray that enables a beamforming and steering capability with a reasonably constant beamwidth for use in a hearing instrument has been developed. A 3-D custom application specific MEMS-based modular micropackaging solution has been developed for integration of the sensor microarray with the necessary microelectronics circuitry and a power supply battery to realize a complete working system in a micropackage.

A new beamforming concept pertaining to a MEMS realization of closely spaced square planar array of acoustical sensors has been developed. The beamforming algorithm is based on the classical delay-and-sum beamforming techniques, but incorporates a new electronic delay term, in addition to the delay due to physical array element spacing, to satisfy Nyquist rate of spatial sampling requirements. The algorithm is also capable of maintaining a reasonably constant beamwidth over the desired audio frequency range. The resulting beam is steerable and can facilitate a speaker tracking capability for a hearing instrument.
An analytical model has been developed that provides a better approximation to the pull-in voltage of a MEMS capacitive-type acoustical sensor having a square diaphragm. The model incorporates the spring softening effect associated with electrostatic force and also the spring hardening effect associated with a rigidly clamped diaphragm with built-in residual stress. The model was validated by comparing the predicted pull-in voltage with finite element analysis results and also by comparing with published experimental results. The model can be extended to determine the pull-in voltage for both fixed-fixed beams and cantilever beams under electrostatic load. The use of this new model has improved the acoustical sensor microarray design methodology.

The sensor microarray, consisting of nine acoustical sensors in a 3 x 3 planar layout has a footprint area of 4.6 x 4.6 mm². The geometry of the microarray has been optimized for a space-constraint application area. Polysilicon-germanium was used as the diaphragm material to realize an increased sensitivity of 10.3 mV/Pa for each array sensor element. A detailed fabrication process table has been developed to fabricate the array. The process table has been simulated using IntelliSuite™ MEMS design tools to verify the resulting geometry and corresponding process steps. The 3-D model generated by the fabrication process simulation matches the design expectations.

A new silicon based modular micropackaging solution has been developed that enables a reliable non-permanent electrical integration of the sensor microarray to the microelectronics circuitry and a power supply battery, while providing a robust mechanical protection and excellent thermal management.
Two different schemes for electrical interconnectivity have been developed. The first scheme uses pressure-dependent platinum coated cantilevered bridge-type microspring contacts that use wafer-through-hole aluminum-via-interconnects to establish the necessary electrical connectivity among the sensor microarray, the microelectronics circuitry, and the power supply battery contained in different micropackage submodules. In this scheme, the microsprings are integral parts of a package submodule and are incorporated in the package submodule fabrication process. The second scheme is based on a conceptually new MEMS-based microbus card connectivity system to establish the necessary intermodular electrical connectivity. The microbus card is a removable insert fabricated out of a silicon wafer using MEMS technology that has heat-treated, gold-coated polysilicon cantilevered microspring contacts fabricated on it. Connectivity is achieved when the microbus card is inserted into the interconnection channel formed by stacking of the package submodules. The bent microsprings on the microbus card will push against the platinum coated microrails inside the interconnection channel to provide the required contact force. Platinum coated microrail contacts in the interconnection channel are connected to a die’s metal I/O pads using copper traces and gold bonding wires.

Both the schemes offer excellent reliable temporary electrical connectivity comparing to existing connectivity mechanisms. The complete design procedure, simulation, fabrication, and electrical characterization of the proposed micropackaging solution are presented. The micropackage solution exhibits excellent signal integrity for high-speed inter-modular electrical connectivity. Use
of silicon as the packaging material enables better thermal management than conventional epoxy resin based packaging solutions.

The proposed MEMS-based modular 3-D integration can be adopted for System-on-Chip (SoC) applications, where dies of different technological origin (0.18 μm or 0.08 μm) can be placed on different package submodules or dies of different functionality, such as digital, memory, analog, RF, etc. can be located in different modules. The modular integration technique also helps to reduce overall chip area and allows for batch fabrication using MEMS fabrication technology. The packaging system can also be used to provide connectivity among dies or devices that are being fabricated using non-compatible fabrication technologies, such as MEMS, photonics, CMOS, fluidics, etc.

The microspring contact pads and modular packaging solution can also be used for die testing purposes by slightly modifying the package submodule geometries to allow a SoC implementation of a die/device Tester-on-Chip (ToC) to temporarily probe other dies/devices for the purpose of testing.

The fabrication process and design methodology was developed through the extensive use of simulation tools. The actual fabrication processes have been simulated and the resulting microstructures have been analyzed using three-dimensional electromechanical finite element analysis (FEA). The finite element analysis results closely match theoretical values predicted by the design methodology.
The acoustical sensor microarray and the micropackaging geometry are ready for physical prototyping. The design has been sent for analysis and prototype fabrication costing to the Corning-IntelliSense Corporation. The design was found to be robust and a price quotation for the microarray fabrication has been received. The physical implementation will take place when the collaborating private sector firm and a MEMS foundry have reached a confidentiality agreement.

Future Work

Work with the Gennum Corporation and the MEMS foundry they select to fabricate a working prototype as part of a technology transfer initiative. After a prototype fabrication, the test of the prototype model can be done and any design revisions can be carried out if necessary.
Appendix I

Die Testing Configuration

The establishment of temporary connectivity for testing a die without exposing the die to otherwise harmful energy sources or contaminations during the test cycles is a major technological challenge. The concept of silicon based modular MEMS micropackaging submodules and connectivity using cantilevered bridge-type microspring contacts can be utilized to develop an efficient microelectronics, MEMS or photonics die testing platform. The geometry of the MEMS micropackage submodules can be reconfigured to establish temporary connectivity for die testing without exposing the die to harmful energy sources or any contamination while carrying out necessary test procedures. Microscale features of the MEMS fabrication technology allows for testing of dies with fine pitch area array I/O pad layout. Figure A1-1 illustrates a CMOS die testing configuration using MEMS socket type structures.

In this set up, two different types of MEMS socket type structures are used: a fixed MEMS socket that is permanently connected to a Tester-on-Chip (ToC), which is virtually a die tester SoC using an enabling gold-to-gold thermosonic bonding technology and a remove socket that acts as a die specific carrier. The enabling gold-to-gold thermosonic bonding technique is graphically illustrated in
Figure A1-1. A CMOS die testing configuration
Figure A1-2. Detailed specifications of such bonding technique are available in [77].

The contact springs on both sides of the remove socket undergo deformation due to the compression mass on the top of the die and generates the necessary contact force. The compression mass and the heat sink in Figure A1-1 are to be specifically designed for insertion of thermal sensors, or an IR laser thermal probe to induce thermal stress on the die under test. It is evident from Figure A1-1 that it is also possible to test a die that is larger than the ToC by reconfiguring the geometry of the remove socket.

Figure A1-3 shows how a complete system composed of electronic dies and MEMS or photonics devices can be tested by simply by altering the remove socket geometry. It is obvious that the contact springs on the remove socket plays the crucial role in establishing connectivity and the design of the microspring contacts that satisfies the test requirements is a big challenge. The developed cantilevered bridge-type microspring contacts can provide highly efficient low resistance, short contact path connectivity while having the ability to tolerate some torsional misalignment.
Figure A1-2. Gold-to-gold thermosonic bonding
Figure A1-3. Test configuration for a system comprised of CMOS, MEMS or Photonics devices or dies
Appendix II
Acoustical Sensor Array Fabrication Process (IntelliSuite Report File)

Number of steps in Process: 123
1. Definition Si Czochralski 100
   Operation on both sides.
   t_film: 400000 nm
   diameter: 101.6 mm
   flat_dir: 110 Vector
   dope_conc: 1e+15 /cm3
   resist: 2.54 Ohm-cm

2. Etch Si Clean Pirahna
   Operation on both sides.
   H2SO4_conc: 75 %
   H2O2_conc: 25 %
   time_etch: 10 min

3. Deposition Si3N4 LPCVD SIH2CL2_NH3
   Operation on bottom side.
   T_dep: 850 deg_C
   P_dep: 0.026 Pa
   SiH2CL2_NH3_R: 3.88 ratio
   Results:
   t_film: 75 nm
   Comments:
   Wafer backside protection and base for ICP-RIE etch for wafer-through-hole

4. Deposition Al Sputter Ar-Ambient
   Operation on top side.
   Rf_Pow: 250 W
   Rf_Freq: 13.56 MHz
   P_dep: 0.1 Pa
   time_dep: 10 min
   Results:
   t_film: 200 nm
   Comments:
   Si ICP-RIE etch mask for wafer through-hole. (May need a SiO2 layer underneath to block plasma penetration through micropores in the aluminum mask)

5. Deposition PR-S1800 Spin S1813
   Operation on top side.
   Speed: 4000 rpm
   time_spin: 30 sec
T_soft: 115 deg_C
time_soft: 60 sec
lambda: 436 nm

Results:
t_film: 1300 nm
REFR_IN: 1.69 #

6. Definition UV Contact Suss
   Operation on top side.
   mask_no: 101 #
   Power: 250 W
   lambda: 436 nm
   time_exp: 10 sec

Results:
dose: 52 J

Comments:
Mask to etch the wafer-through-hole

7. Etch PR-S1800 Wet 1112A
   Operation on both sides.
   T_etch: 20 deg_C
   time_etch: 5 min

Results:
t_etch: 990000 nm

8. Etch Al RIE Cl2_Plasma
   Operation on top side.
   P_etch: 0.0133 Pa
   T_etch: 110 deg_C
   Rf_Freq: 13.56 MHz
   Rf_Pow: 1500 W

Results:
t_etch: 990000 nm

9. Etch Si Dry SF6_O2
   Operation on top side.
   Rf_Freq: 13.56 MHz
   Rf_Pow: 1000 W
   P_etch: 0.133 Pa
   time_etch: 75 min
   T_etch: -110 deg_C

Results:
t_etch: 400000 nm

Comments:
Wafer through-hole etch

10. Etch PR-S1800 Wet 1165
    Operation on both sides.
    T_etch: 20 deg_C
    time_etch: 5 min

Results:
t_etch: 990000 nm

11. Etch Al RIE Cl2_Plasma
    Operation on top side.
    P_etch: 0.0133 Pa
    T_etch: 110 deg_C
Rf_Freq: 13.56 MHz
Rf_Pow: 1500 W

Results:
   t_etch: 990000 nm

12. Deposition Al Sputter Ar-Ambient
   Operation on top side.
   Rf_Pow: 250 W
   Rf_Freq: 13.56 MHz
   P_dep: 0.1 Pa
   time_dep: 10 min

Results:
   t_film: 200 nm

Comments:
   Si ICP-RIE etch mask to etch inner cavities and air outlet ports on the wafer
   topside. May need a SiO2 layer underneath as explained in step 4

13. Deposition PR-S1800 Spin S1813
   Operation on top side.
   Speed: 4000 rpm
   time_spin: 30 sec
   T_soft: 115 deg_C
   time_soft: 60 sec
   lambda: 436 nm

Results:
   t_film: 1300 nm
   REPR_IN: 1.69 #

14. Definition UV Contact Suss
   Operation on top side.
   mask_no: 102 #
   Power: 250 W
   lambda: 436 nm
   time_exp: 10 sec

Results:
   dose: 52 J

Comments:
   Inner cavity pattern

15. Etch PR-S1800 Wet 1112A
   Operation on both sides.
   T_etch: 20 deg_C
   time_etch: 5 min

Results:
   t_etch: 990000 nm

16. Etch Al RIE Cl2_Plasma
   Operation on top side.
   P_etch: 0.0133 Pa
   T_etch: 110 deg_C
   Rf_Freq: 13.56 MHz
   Rf_Pow: 1500 W

Results:
   t_etch: 990000 nm

17. Etch Si Dry SF6_O2
   Operation on top side.
Rf_Freq: 13.56 MHz
Rf_Pow: 1000 W
P_etch: 0.133 Pa
time_etch: 75 min
T_etch: -110 deg_C

Results:
t_etch: 20000 nm

Comments:
ICP-RIE etch of wafer to create the inner cavities and air outlet ports

18. Etch PR-S1800 Wet 1165
   Operation on both sides.
   T_etch: 20 deg_C
   time_etch: 5 min

Results:
t_etch: 990000 nm

19. Etch Al RIE Cl2_Plasma
   Operation on top side.
   P_etch: 0.0133 Pa
   T_etch: 110 deg_C
   Rf_Freq: 13.56 MHz
   Rf_Pow: 1500 W

Results:
t_etch: 990000 nm

20. Etch Si Clean Pirahna
   Operation on both sides.
   H2SO4_conc: 75 %
   H2O2_conc: 25 %
   time_etch: 10 min

21. Deposition Si3N4 LPCVD SIH2CL2_NH3
   Operation on top side.
   T_dep: 850 deg_C
   P_dep: 0.026 Pa
   SiH2CL2_NH3_R: 3.88 ratio

Results:
t_film: 75 nm

Comments:
Insulation inside the wafer through-hole

22. Deposition PR-S1800 Spin S1805
   Operation on top side.
   Speed: 4000 rpm
   time_spin: 30 sec
   T_soft: 115 deg_C
   time_soft: 60 sec
   lambda: 436 nm

Results:
t_film: 500 nm

23. Definition UV Contact Suss
   Operation on top side.
   mask_no: 103 #
   Power: 250 W
   lambda: 436 nm
time_exp: 10 sec
Results: 
  dose: 52 J
Comments:
Mask to etch Si3N4 at the bottom of the wafer through-hole and wafer topside leaving Si3N4 only on the through-hole side walls

24. Etch PR-S1800 Wet 1112A
   Operation on both sides.
   T_etch: 20 deg_C
   time_etch: 5 min
Results:
  t_etch: 500 nm

25. Etch Si3N4 RIE RIE
   Operation on top side.
   time_etch: 20 min
Results:
  t_etch: 500 nm

26. Etch Si Clean Pirahna
   Operation on both sides.
   H2SO4_conc: 75 %
   H2O2_conc: 25 %
   time_etch: 10 min

27. Deposition Cr E-Beam E-Beam
   Operation on top side.
   P_vac: 45 uTorr
   Rf_Pow: 250 W
   Rf_Freq: 13.56 MHz
   time_dep: 10 min
Results:
  t_film: 70 nm
Comments:
Adhesion layer for aluminum electroplating

28. Deposition Ti Sputter Ar-Ambient
   Operation on top side.
   Rf_Pow: 250 W
   Rf_Freq: 13.56 MHz
   P_dep: 0.1 Pa
   time_dep: 10 min
Results:
  t_film: 30 nm
Comments:
Seed layer for aluminum electroplating

29. Deposition PR-KTI-820 Spin Spin1
   Operation on top side.
   Speed: 3000 rpm
   time_dep: 0.5 min
Results:
  t_film: 500 nm

30. Definition UV Contact Suss
   Operation on top side.
mask_no: 104 #  
Power: 250 W  
lambda: 436 nm  
time_exp: 10 sec  

Results:  
dose: 52 J  
Comments:  
Mask for electroplating  

31. Etch PR-KTI-820 Wet Solvent  
   Operation on both sides.  
   time_etch: 5 min  
Results:  
t_etch: 990000 nm  

32. Deposition Al Electroplat Standard  
   Operation on top side.  
   efficiency: 92 %  
Results:  
t_film: 399900 nm  
Comments:  
Wafer through-hole aluminum via-interconnect depositon (Ref. Stanford-Chow, JMEMS-6(2), 97),Frazier  

33. Etch PR-KTI-820 Wet Pirahna  
   Operation on both sides.  
   H2SO4_conc: 75 %  
   H2O2_conc: 25 %  
   time_etch: 10 min  
Results:  
t_etch: 1e+06 nm  

34. Deposition PR-S1800 Spin S1805  
   Operation on top side.  
   Speed: 4000 rpm  
   time_spin: 30 sec  
   T_soft: 115 deg_C  
   time_soft: 60 sec  
   lambda: 436 nm  
Results:  
t_film: 500 nm  

35. Definition UV Contact Suss  
   Operation on top side.  
   mask_no: 105 #  
   Power: 250 W  
   lambda: 436 nm  
   time_exp: 10 sec  
Results:  
dose: 52 J  
Comments:  
Cr Adhesion and Ti seed layer etch  

36. Etch PR-S1800 Wet 1112A  
   Operation on both sides.  
   T_etch: 20 deg_C  
   time_etch: 5 min
Results:

\[ t_{etch} : 500 \text{ nm} \]

37. Etch Ti RIE SF6/CHF4/O2
   Operation on top side.
   \[ P_{etch} : 0.00133 \text{ Pa} \]
   \[ time_{etch} : 5 \text{ min} \]
   \[ Rf_{Freq} : 13.56 \text{ MHz} \]
   \[ Rf_{Pow} : 750 \text{ W} \]

Results:

\[ t_{etch} : 30 \text{ nm} \]

38. Etch Cr Wet PAN
   Operation on top side.
   \[ H2PO4_{conc} : 75 \% \]
   \[ C2H4O2_{conc} : 15 \% \]
   \[ HNO3_{conc} : 5 \% \]
   \[ time_{etch} : 1 \text{ min} \]

Results:

\[ t_{etch} : 990000 \text{ nm} \]

39. Etch PR-S1800 Wet 1165
   Operation on both sides.
   \[ T_{etch} : 20 \text{ deg}_C \]
   \[ time_{etch} : 5 \text{ min} \]

Results:

\[ t_{etch} : 990000 \text{ nm} \]

40. Deposition SiO2 PECVD Ar
   Operation on top side.
   \[ T_{dep} : 350 \text{ deg}_C \]
   \[ P_{dep} : 200 \text{ Pa} \]
   \[ time_{dep} : 10 \text{ min} \]
   \[ Rf_{Pow} : 50 \text{ W} \]
   \[ Rf_{Freq} : 13.56 \text{ MHz} \]
   \[ tot_{fl} : 20.8 \text{ sccm} \]
   \[ O2_{pp} : 0.024 \text{ part.pr} \]
   \[ SiH4_{pp} : 0.014 \text{ part.pr} \]
   \[ Ar_{pp} : 0.962 \text{ part.pr} \]
   \[ T_{anne} : 800 \text{ deg}_C \]
   \[ time_{an} : 30 \text{ min} \]

Results:

\[ t_{film} : 20000 \text{ nm} \]

Comments:
Thick oxide to fill the inner cavities and air outlet ports

41. Deposition PR-S1800 Spin S1805
   Operation on top side.
   \[ Speed : 4000 \text{ rpm} \]
   \[ time_{spin} : 30 \text{ sec} \]
   \[ T_{soft} : 115 \text{ deg}_C \]
   \[ time_{soft} : 60 \text{ sec} \]
   \[ lambda : 436 \text{ nm} \]

Results:

\[ t_{film} : 500 \text{ nm} \]

42. Definition UV Contact Suss
Operation on top side.

mask_no: 106 #
Power: 250 W
lambda: 436 nm
time_exp: 10 sec

Results:

dose: 52 J

Comments:
Thick oxide etch mask for inner cavities and air outlet ports

43. Etch PR-S1800 Wet 1112A
Operation on both sides.

T_etch: 20 deg_C
time_etch: 5 min

Results:

t_etch: 500 nm

44. Etch SiO2 RIE Dry
Operation on top side.

T_etch: 0 deg_C
time_etch: 0 min

Results:

t_etch: 20000 nm
t_after: 0 nm

45. Etch PR-S1800 Wet 1165
Operation on both sides.

T_etch: 20 deg_C
time_etch: 5 min

Results:

t_etch: 990000 nm

46. Deposition PR-S1800 Spin S1805
Operation on top side.

Speed: 4000 rpm
time_spin: 30 sec
T_soft: 115 deg_C
time_soft: 60 sec
lambda: 436 nm

Results:

t_film: 500 nm

47. Definition UV Contact Suss
Operation on top side.

mask_no: 107 #
Power: 250 W
lambda: 436 nm
time_exp: 10 sec

Results:

dose: 52 J

Comments:
Thick oxide offset removal

48. Etch PR-S1800 Wet 1112A
Operation on both sides.

T_etch: 20 deg_C
time_etch: 5 min
Results:
  t_etch: 500 nm

49. Etch SiO2 Wet BOE
   Operation on both sides.
   time_etch: 10 min
   T_etch: 10 deg_C
Results:
  t_etch: 20000 nm

50. Etch Si Clean Pirahna
   Operation on both sides.
   H2SO4_conc: 75 %
   H2O2_conc: 25 %
   time_etch: 10 min

51. Deposition Si3N4 LPCVD SIH2CL2_NH3
   Operation on top side.
   T_dep: 850 deg_C
   P_dep: 0.026 Pa
   SiH2CL2_NH3_R: 3.88 ratio
Results:
  t_film: 1000 nm
Comments:
Backplate Si3N4

52. Deposition PR-S1800 Spin S1805
   Operation on top side.
   Speed: 4000 rpm
   time_spin: 30 sec
   T_soft: 115 deg_C
   time_soft: 60 sec
   lambda: 436 nm
Results:
  t_film: 500 nm

53. Definition UV Contact Suss
   Operation on top side.
   mask_no: 108 #
   Power: 250 W
   lambda: 436 nm
   time_exp: 10 sec
Results:  
  dose: 52 J
Comments:
Backplate nitride etch mask to expose the aluminum via-interconnect for Ti and Au deposition

54. Etch PR-S1800 Wet 1112A
   Operation on both sides.
   T_etch: 20 deg_C
   time_etch: 5 min
Results:
  t_etch: 500 nm

55. Etch Si3N4 RIE RIE
   Operation on top side.
time_etch: 20 min

Results:
  t_etch: 1000 nm

56. Etch Si Clean Pirahna
    Operation on both sides.
    H2SO4_conc: 75 %
    H2O2_conc: 25 %
    time_etch: 10 min

57. Deposition Ti Sputter Ar-Ambient
    Operation on top side.
    Rf_Pow: 250 W
    Rf_Freq: 13.56 MHz
    P_dep: 0.1 Pa
    time_dep: 10 min

Results:
  t_film: 30 nm

Comments:
  Adhesion layer for gold

58. Deposition Au E-Beam E-Beam
    Operation on top side.
    Rf_Pow: 100 W
    Rf_Freq: 13.56 MHz
    T_dep: 100 deg C
    P_vac: 10 uTorr
    time_dep: 10 min

Results:
  t_film: 30 nm

Comments:
  Gold deposition for backplate electrode

59. Deposition PR-S1800 Spin S1805
    Operation on top side.
    Speed: 4000 rpm
    time_spin: 30 sec
    T_soft: 115 deg C
    time_soft: 60 sec
    lambda: 436 nm

Results:
  t_film: 500 nm

60. Definition UV Contact Suss
    Operation on top side.
    mask_no: 109 #
    Power: 250 W
    lambda: 436 nm
    time_exp: 10 sec

Results:
  dose: 52 J

Comments:
  Back vent etch mask to etch Au, Ti and Si3N4 backplate to create acoustical ports

61. Etch PR-S1800 Wet 1112A
    Operation on both sides.
T_etch: 20 deg_C
time_etch: 5 min

Results:

t_etch: 990000 nm

62. Etch Au RIE CL2-Plasma
Operation on top side.
P_etch: 0.1333 Pa
T_etch: 110 deg_C
Rf_Freq: 13.56 MHz
Rf_Pow: 1500 W

Results:

t_film: 990000 nm

63. Etch Ti RIE SF6/CHF4_02
Operation on top side.
P_etch: 0.00133 Pa
time_etch: 5 min
Rf_Freq: 13.56 MHz
Rf_Pow: 750 W

Results:

t_etch: 990000 nm

64. Etch Si3N4 RIE RIE
Operation on top side.
time_etch: 20 min

Results:

t_etch: 990000 nm

65. Etch PR-S1800 Wet 1165
Operation on both sides.
T_etch: 20 deg_C
time_etch: 5 min

Results:

t_etch: 500 nm

66. Deposition PR-S1800 Spin S1805
Operation on top side.
Speed: 4000 rpm
time_spin: 30 sec
T_soft: 115 deg_C
time_soft: 60 sec
lambda: 436 nm

Results:

t_film: 500 nm

67. Definition UV Contact Suss
Operation on top side.
mask_no: 110 #
Power: 250 W
lambda: 436 nm
time_exp: 10 sec

Results:

dose: 52 J

Comments:
Au, Ti and backplate nitride etch to shape individual microphone backplate
68. Etch PR-S1800 Wet 1112A
   Operation on both sides.
   \[ T_{etch}: 20 \text{ deg}_C \]
   \[ \text{time}_{etch}: 5 \text{ min} \]
   Results:
   \[ t_{etch}: 990000 \text{ nm} \]

69. Etch Au RIE CL2-Plasma
   Operation on top side.
   \[ P_{etch}: 0.1333 \text{ Pa} \]
   \[ T_{etch}: 110 \text{ deg}_C \]
   \[ \text{Rf}_F\text{req}: 13.56 \text{ MHz} \]
   \[ \text{Rf}_\text{Pow}: 1500 \text{ W} \]
   Results:
   \[ t_{film}: 990000 \text{ nm} \]

70. Etch Ti RIE SF6/CHF4_O2
   Operation on top side.
   \[ P_{etch}: 0.00133 \text{ Pa} \]
   \[ \text{time}_{etch}: 5 \text{ min} \]
   \[ \text{Rf}_\text{Freq}: 13.56 \text{ MHz} \]
   \[ \text{Rf}_\text{Pow}: 750 \text{ W} \]
   Results:
   \[ t_{etch}: 990000 \text{ nm} \]

71. Etch PR-S1800 Wet 1165
   Operation on both sides.
   \[ T_{etch}: 20 \text{ deg}_C \]
   \[ \text{time}_{etch}: 5 \text{ min} \]
   Results:
   \[ t_{etch}: 990000 \text{ nm} \]

72. Etch Si3N4 RIE RIE
   Operation on top side.
   \[ \text{time}_{etch}: 20 \text{ min} \]
   Results:
   \[ t_{etch}: 990000 \text{ nm} \]

73. Deposition SiO2 LPCVD Standard
    Operation on top side.
    \[ T_{dep}: 420 \text{ deg}_C \]
    \[ \text{time}_{dep}: 120 \text{ min} \]
    Results:
    \[ t_{film}: 1060 \text{ nm} \]
    Comments:
    Filler oxide to planarize the top surface of the backplate (Planarization/Polishing)

74. Deposition PR-S1800 Spin S1805
    Operation on top side.
    \[ \text{Speed}: 4000 \text{ rpm} \]
    \[ \text{time}_{spin}: 30 \text{ sec} \]
    \[ T_{soft}: 115 \text{ deg}_C \]
    \[ \text{time}_{soft}: 60 \text{ sec} \]
    \[ \lambda: 436 \text{ nm} \]
    Results:
    \[ t_{film}: 50 \text{ nm} \]
75. Definition UV Contact Suss
   Operation on top side.
   mask_no: 111 #
   Power: 250 W
   lambda: 436 nm
   time_exp: 10 sec
Results:  dose: 52 J
Comments:
SiO2 filler oxide etch mask for polishing/planarisation of the backplate top surface

76. Etch PR-S1800 Wet 1112A
   Operation on both sides.
   T_etch: 20 deg_C
   time_etch: 5 min
Results:
   t_etch: 990000 nm

77. Etch SiO2 RIE Dry
   Operation on top side.
   T_etch: 50 deg_C
   time_etch: 50 min
Results:
   t_etch: 990000 nm

78. Etch PR-S1800 Wet 1165
   Operation on both sides.
   T_etch: 20 deg_C
   time_etch: 5 min
Results:
   t_etch: 990000 nm

79. Deposition SiO2 LPCVD Standard
   Operation on top side.
   T_dep: 420 deg_C
   time_dep: 120 min
Results:
   t_film: 3500 nm
Comments:
Airgap Oxide

80. Deposition PR-S1800 Spin S1805
   Operation on top side.
   Speed: 4000 rpm
   time_spin: 30 sec
   T_soft: 115 deg_C
   time_soft: 60 sec
   lambda: 436 nm
Results:
   t_film: 50 nm

81. Definition UV Contact Suss
   Operation on top side.
   mask_no: 112 #
   Power: 250 W
lambda: 436 nm
time_exp: 10 sec

Results:
dose: 52 J

Comments:
Airgap oxide pattern

82. Etch PR-S1800 Wet 1112A
   Operation on both sides.
       T_etch: 20 deg_C
       time_etch: 5 min
   Results:
       t_etch: 990000 nm

83. Etch SiO2 RIE Dry
   Operation on top side.
       T_etch: 50 deg_C
       time_etch: 50 min
   Results:
       t_etch: 990000 nm

84. Etch PR-S1800 Wet 1165
   Operation on both sides.
       T_etch: 20 deg_C
       time_etch: 5 min
   Results:
       t_etch: 990000 nm

85. Deposition Si3N4 PECVD Ar
   Operation on top side.
       T_dep: 275 deg_C
       P_dep: 127 Pa
       Rf_Pow: 250 W
       Rf_Freq: 13.56 MHz
       tot_fl: 1500 sccm
           Arpp: 0.959 part.pr
           NH3pp: 0.024 part.pr
           SiH4pp: 0.017 part.pr
   Results:
       t_film: 1000 nm
   Comments:
Back and front electrode isolation

86. Deposition PR-S1800 Spin S1805
   Operation on top side.
       Speed: 4000 rpm
       time_spin: 30 sec
       T_soft: 115 deg_C
       time_soft: 60 sec
       lambda: 436 nm
   Results:
       t_film: 500 nm

87. Definition UV Contact Suss
   Operation on top side.
       mask_no: 113 #
       Power: 250 W
lambda: 436 nm
time_exp: 10 sec

Results:
dose: 52 J

Comments:
Isolation PECVD nitride etch mask

88. Etch PR-S1800 Wet 1112A
Operation on both sides.
T_etch: 20 deg_C
time_etch: 5 min

Results:
t_etch: 990000 nm

89. Etch Si3N4 RIE RIE
Operation on top side.
time_etch: 20 min

Results:
t_etch: 990000 nm

90. Etch Si Clean Pirahna
Operation on both sides.
H2SO4_conc: 75 %
H2O2_conc: 25 %
time_etch: 10 min

91. Deposition PolySi LPCVD SiH4
Operation on both sides.
T_dep: 630 deg_C
P_dep: 53 Pa
time_dep: 15 min
T_anne: 1100 deg_C
time_an: 60 min

Results:
t_film: 40 nm

Comments:
Nucleation layer for Poly-SiGe. Poly-SiGe is the diaphragm material

92. Deposition PolySiGe LPCVD General
Operation on top side.
T_dep: 450 deg_C
P_dep: 40 Pa

Results:
t_film: 760 nm

Comments:
Diaphragm material

93. Deposition PR-S1800 Spin S1805
Operation on top side.
Speed: 4000 rpm
time_spin: 30 sec
T_soft: 115 deg_C
time_soft: 60 sec
lambda: 436 nm

Results:
t_film: 500 nm
94. Definition UV Contact Suss
   Operation on top side.
   mask_no: 114 #
   Power: 250 W
   lambda: 436 nm
   time_exp: 10 sec
   Results:
   dose: 52 J
   Comments:
   Diaphragm etch mask

95. Etch PR-S1800 Wet 1112A
   Operation on both sides.
   T_etch: 20 deg_C
   time_etch: 5 min
   Results:
   t_etch: 990000 nm

96. Etch PolySiGe Dry SF6-Plasma
   Operation on top side.
   P_etch: 19.998 Pa
   Power: 375 W
   time_etch: 5 min
   Results:
   t_etch: 990000 nm

97. Etch PolySi Dry SF6-Plasma
   Operation on both sides.
   time_etch: 15 min
   P_base: 0.0001 Pa
   Results:
   t_etch: 990000 nm

98. Etch PR-S1800 Wet 1165
   Operation on both sides.
   T_etch: 20 deg_C
   time_etch: 5 min
   Results:
   t_etch: 990000 nm

99. Deposition PR-S1800 Spin S1805
   Operation on top side.
   Speed: 4000 rpm
   time_spin: 30 sec
   T_soft: 115 deg_C
   time_soft: 60 sec
   lambda: 436 nm
   Results:
   t_film: 500 nm

100. Definition UV Contact Suss
     Operation on top side.
     mask_no: 115 #
     Power: 250 W
     lambda: 436 nm
     time_exp: 10 sec
     Results:
dose: 52 J

Comments:
Etch mask to etch the Si3N4 layer over the air outlet ports. Also to be used to etch the oxide in the inner cavities and airgap oxide

101. Etch PR-S1800 Wet 1112A
   Operation on both sides.
   T_etch: 20 deg_C
   time_etch: 5 min
   Results:
   t_etch: 990000 nm

102. Etch Si3N4 RIE RIE
   Operation on top side.
   time_etch: 20 min
   Results: t_etch: 990000 nm
   Comments:
   Si3N4 etching over the air outlet ports

103. Etch PR-S1800 Wet 1165
   Operation on both sides.
   T_etch: 20 deg_C
   time_etch: 5 min
   Results:
   t_etch: 990000 nm

104. Deposition SiO2 PECVD Ar
   Operation on top side.
   T_dep: 350 deg_C
   P_dep: 200 Pa
   time_dep: 10 min
   Rf_Pow: 50 W
   Rf_Freq: 13.56 MHz
   tot_fl: 20.8 sccm
   O2pp: 0.024 part.pr
   SiH4pp: 0.014 part.pr
   Arpp: 0.962 part.pr
   T_anne: 800 deg_C
   time_an: 30 min
   Results: t_film: 500 nm
   Comments:
   Protective LTO on the wafer topside

105. Deposition PR-S1800 Spin S1805
   Operation on bottom side.
   Speed: 4000 rpm
   time_spin: 30 sec
   T_soft: 115 deg_C
   time_soft: 60 sec
   lambda: 436 nm
   Results:
   t_film: 500 nm

106. Definition UV Contact Suss
   Operation on bottom side.
mask_no: 116 #
Power: 250 W
lambda: 436 nm
time_exp: 10 sec

Results:
dose: 52 J

Comments:
Si3N4 etch on the wafer backside to expose aluminum via-interconnects for subsequent contact pad connection

107. Etch PR-S1800 Wet 1112A
Operation on both sides.
T_etch: 20 deg_C
time_etch: 5 min

Results:
t_etch: 990000 nm

108. Etch Si3N4 RIE RIE
Operation on both sides.
time_etch: 20 min

Results:
t_etch: 990000 nm

109. Etch Si Clean Pirahna
Operation on both sides.
H2SO4_conc: 75 %
H2O2_conc: 25 %
time_etch: 10 min

110. Deposition Al E-Beam E-Beam
Operation on bottom side.
P_vac: 0 uTorr
Rf_Freq: 0 MHz
Rf_Pow: 0 W
time_dep: 0 min

Results:
t_film: 1000 nm

Comments:
Contact pad definition

111. Deposition PR-S1800 Spin S1805
Operation on bottom side.
Speed: 4000 rpm
time_spin: 30 sec
T_soft: 115 deg_C
time_soft: 60 sec

lambda: 436 nm

Results:
t_film: 500 nm

112. Definition UV Contact Suss
Operation on bottom side.
mask_no: 117 #
Power: 250 W
lambda: 436 nm
time_exp: 10 sec

Results:
dose: 52 J

Comments:
75 x 75 micrometer2 aluminum contact pad pattern

113. Etch PR-S1800 Wet 1112A
    Operation on both sides.
    T_etch: 20 deg_C
time_etch: 5 min

Results:
    t_etch: 990000 nm

114. Etch Al Wet PAN
    Operation on both sides.
    H2PO4_conc: 75 %
    C2H4O2_conc: 15 %
    HNO3_conc: 5 %
time_etch: 15 min

Results:
    t_etch: 990000 nm

115. Etch PR-S1800 Wet 1165
    Operation on both sides.
    T_etch: 20 deg_C
time_etch: 5 min

Results:
    t_etch: 990000 nm

116. Deposition Si3N4 PECVD Ar
    Operation on bottom side.
    T_dep: 275 deg_C
    P_dep: 127 Pa
    Rf_Pow: 250 W
    Rf_Freq: 13.56 MHz
tot_fl: 1500 sccm
    Arpp: 0.959 part.pr
    NH3pp: 0.024 part.pr
    SiH4pp: 0.017 part.pr

Results:
    t_film: 100 nm

Comments:
Passivation nitride

117. Deposition PR-S1800 Spin S1805
    Operation on bottom side.
    Speed: 4000 rpm
time_spin: 30 sec
    T_soft: 115 deg_C
time_soft: 60 sec
    lambda: 436 nm

Results:
    t_film: 500 nm

118. Definition UV Contact Suss
    Operation on bottom side.
    mask_no: 118 #
    Power: 250 W
    lambda: 436 nm
time_exp: 10 sec

Results:

dose: 52 J

Comments:
Passivation nitride pattern

119. Etch PR-S1800 Wet 1112A
Operation on both sides.
  T_etch: 20 deg_C
  time_etch: 5 min

Results:
  t_etch: 500 nm

120. Etch Si3N4 RIE RIE
Operation on bottom side.
  time_etch: 20 min

Results:
  t_etch: 990000 nm

121. Etch PR-S1800 Wet 1165
Operation on both sides.
  T_etch: 20 deg_C
  time_etch: 5 min

Results:
  t_etch: 990000 nm

122. Etch SiO2 Wet BHF
Operation on top side.
  HF_conc: 80 %
  H2Opp: 1 part.pr
  time_etch: 8 min

Results:
  t_etch: 990000 nm

Comments:
Protective LTO strip

123. Etch SiO2 Wet Sacrifice
Operation on top side.
  time_etch: 60 min
  T_etch: 72 deg_C

Results:
  t_etch: 1e+06 nm

Comments:
Airgap oxide and inner cavities oxide sacrificial etch
References


[45] Y. He, J. Machete, C. Gallegos and F. Maser, “Accurate Fully-Coupled Natural Frequency Shift of MEMS Actuators Due to Voltage Bias and Other External Forces”, in *Technical Digest of IEEE 12th International Conference*


Vita Auctoris

NAME: Sazzadur Chowdhury
PLACE OF BIRTH: Chittagong, Bangladesh
YEAR OF BIRTH: 1961
EDUCATION:
2000 – Present Ph.D. student in Electrical and Computer Engineering, University of Windsor, Windsor, Ontario.
Thesis title: A MEMS Acoustical Sensor Array and Associated Micropackage

2000 M.A.Sc. in Electrical and Computer Engineering, University of Windsor, Windsor, Ontario.
Thesis title: Microelectromechanical (MEMS) VLSI Structures for Hearing Instruments

1984 B.Sc. in Electrical and Electronics Engineering, Bangladesh University of Engineering and Technology, Dhaka, Bangladesh.
Thesis title: Computer-aided Solution of Feedback Control System Problems

EXPERIENCE:
1998 – Present University of Windsor, Windsor, Ontario
1. Graduate Assistant
   • Assisted professor in conducting computer aided laboratory experiments for the first and second year engineering students
   • Assisted professor in conducting the mid-term and final exams
   • Provided expertise to students who needed extra help
   • Conducted tutorial sessions assisting students in solving problems
   • Contributed to the formulation and delivery of the graduate course 88-590-08 (Microelectromechanical Systems)
     (i) Preparing self-based learning modules
     (ii) Supervising the computer based MEMS design methodology

2. Research Assistant (Dr. W. C. Miller)
   • Research Area: Development of the Microelectromechanical Systems (MEMS) based acoustical sensor microarray, electromagnetic microactuators
and MEMS based micropackaging solutions for integration of diverse technological origin dies or devices to a System-on-Chip (SoC) environment

- Published a research paper in the December, 2002 issue of the IEEE Sensors Journal
- Published a special invited research article in the second quarter, 2002 issue of the IEEE Circuits and Systems magazine
- Published nine refereed conference papers at national and international locations and made nine special presentations at national locations
- Engaged in a technology transfer initiative as part of a collaborative research partnership with the Gennum Corporation and the IntelliSense Corporation while in the Masters and Ph.D. programs
- Received three national awards for innovative contributions to research and development in MEMS and microelectronics in Canada
- Research work featured in the national news media, and also published on university, government and corporate web sites

1988 – 1997  Bangladesh Telegraph and Telephone Board, Bangladesh

Electrical Engineer (ten years experience as a professional engineer in planning, operation and maintenance of telecommunications network)

1988 – 1989 (June) Special course (theory, laboratory, industrial field experience, satellite communication ground station inspection, management courses) on advanced telecommunications technologies

1989 (June) – 1990 Instructor: Telecommunication Staff College, Gazipur, Bangladesh. Have developed and conducted training courses regarding digital communications and telecommunications switching technology, microprocessors, etc.

1991 – 1992 Supervising Engineer; Tangail district (county), Bangladesh. Responsibilities included operation and maintenance of telecommunications network of greater Tangail district (county) that included digital/analog telephone exchanges, cable networks and digital transmission links.


1996 Supervising Engineer; Planning Section, Bangladesh Telegraph and Telephone Board, Dhaka. Contributed to policy and structural formulation of telecom sector deregulation in Bangladesh (Recommendations are implemented by the Bangladesh Government)
1997 Supervising Engineer; Moghbazar Telephone Exchange, Dhaka. Responsibilities included operation and maintenance of outside plant networks serving Moghbazar district of Dhaka city.

PUBLICATIONS:

Refereed Publications


Special Presentations


3. Sazzadur Chowdhury, G. A. Jullien, M. Ahmadi, W. C. Miller, Nora Finch, Daniel Keating “A Surface Mountable MEMS Socket for the Integration or Temporary Connectivity of Other Devices or Dies into a CMOS Environment”, Canadian Workshop on MEMS (CWMEMS’01), Ottawa, August, 2001 (Poster session).


FIELD TRIPS:
November 22, 2001  Micralyne Inc. Edmonton, Alberta, Visited MEMS foundry and had technical meeting on device and sensor fabrication.
May 26, 2002  Columbia University’s Biosphere 2 Center, Oracle, Arizona, Ecosystem applications of MEMS.

TECHNOLOGY TRANSFER:
February 18, 2003  Gennum Corporation, Burlington, Ontario, “Design Methodology for a MEMS Capacitive Microphone Array”.
February 26, 2001  Gennum Corporation, Burlington, Ontario, “A MEMS Beamforming Microphone Array”.

SPECIAL LECTURES:
November 23, 2001  Presented MEMS Short Course at the University of Calgary, Calgary, Alberta

AWARDS:
1. **2000 Ontario Graduate Scholarship for Science and Technology (OGSST)**
   Received the Ontario Graduate Scholarship for Science and Technology (OGSST) for the year 2000 valued at $15,000 per year.

2. **MICRONET Best Paper Award 2000**
   Received the “MICRONET Best Paper Award 2000” by MICRONET, the Federal Network of Centres of Excellence on Microelectronics, Devices, Circuits and Systems in the MICRONET 10th Anniversary Workshop held in Ottawa from April 27-28, 2000. The award consists of a cash prize of $1,000 and a certificate.

3. **2001 Ontario Graduate Scholarship for Science and Technology (OGSST)**
   Received the Ontario Graduate Scholarship for Science and Technology (OGSST) for the year 2001 valued at $15,000 per year.

4. **MICRONET Best Paper Award 2001**
   Received the “MICRONET Best Paper Award 2001” by MICRONET, in the 11th MICRONET’ Annual Workshop held in Aylmer, Quebec from April 19-20, 2001. The award consists of a cash prize of $1,000 and a certificate.
5. **2001 Strategic Microelectronics Consortium Industrial Collaboration Award**

Received the “2001 Strategic Microelectronics Consortium Industrial Collaboration Award” by the Strategic Microelectronics Consortium at the Symposium on Microelectronics Research & Development in Canada (MR&DCAN 2001), Ottawa, June 2001. The award consists of a $3,000 cash prize and a certificate.

6. **2002 Ontario Graduate Scholarship for Science and Technology (OGSST)**

Received the Ontario Graduate Scholarship for Science and Technology (OGSST) for the year 2002 valued at $15,000 per year.

7. **2003 Ontario Graduate Scholarship for Science and Technology (OGSST)**

Received the Ontario Graduate Scholarship for Science and Technology (OGSST) for the year 2003 valued at $15,000 per year.

8. **Research Assistantship**

Research Assistantship of $1,800 per month from supervisor's NSERC grant.

9. **Performance Award 1993**

Received performance award for outstanding service in 1993 while working as the supervising engineer at the Central Telephone Exchange, Dhaka, Bangladesh.

10. **Performance Award 1991**

Received performance award for outstanding service in 1991 while working as the supervising engineer in Tangail, Bangladesh.