A vector generator for a computer display system.

Ting Hin Houang

University of Windsor

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A VECTOR GENERATOR FOR

A COMPUTER DISPLAY SYSTEM

by

TING HIN HOUANG

A Thesis

Submitted to the Faculty of Graduate Studies through
the Department of Electrical Engineering in Partial
Fulfillment of the Requirement for the Degree of
Master of Applied Science at the
University of Windsor

Windsor, Ontario
1972
ABSTRACT

This theses presents the design and implementation of a subsystem of a display system -- a vector generator, and associated intensity circuit for a cathode ray tube display terminal.

The vector generator is essentially two integrators which generate ramp signals; one for the vertical and the other for the horizontal deflection. It is desirable to generate a vector of any length and at any angle during a constant integration time. Also it can operate as a position generator to place a visible or invisible dot in a required position, from whence a vector may be drawn.

Four different intensity levels, dim, normal, bright, and blanked, are provided in the intensity circuit. Any of the four intensity levels can be chosen by the user. During the alphanumeric (A/N) mode three additional intensity levels are automatically selected for the user to compensate for the variation of intensity which occurs when the three different size of characters are being generated. During the vector mode the intensity of the vector is compensated automatically according to the length of the vector.
ACKNOWLEDGEMENTS

The author wishes to express his appreciation to
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CHAPTER I

INTRODUCTION

I. Introduction

In recent years great interest has developed in the area of graphical displays and graphical display systems. This interest has resulted primarily from the increasing use of large digital computers for information processing. Because these computers are capable of generating large amounts of information at high rates, it has become necessary to search for means of information display which can more nearly match their speed. In addition, there is a continual search for better means of communication between man and his machines and it is thought that some improvement can be obtained by the use of visual display technique. The aim of any graphic terminal is to maximize the information transfer between the user and the computer, preferably in an interactive way.

Modern electronic computer data displays convert computer data into visual, photographic, or electronic data. The display readout device of major importance in visual computer data display systems is the cathode ray tube (CRT). The use of a cathode ray tube as an output terminal allows computer data to be available instantly. For displays associated with computers, the common practice, is to operate the display direct from the computer. The technique becomes troublesome when the amount of information on the display becomes large because considerable computing time and memory space are used to regenerate the display. With the advent of the time-sharing concept for efficiently and conveniently utilizing computers, a local buffer
store associated with the display unit is used.

The term computer graphics refers to the concept of man
communicating with a computer by means of graphical symbols such as
lines, curves, dots and alphanumerical symbols. These graphical
symbols are accomplished by the vector, dot and alphanumeric generators.
In a sense, computer graphics can be considered as one more degree
of freedom in man-machine communication, and adds the dimension of
sketching and drawing for both input to and output from the computer.
In this thesis the cathode ray tube is used as a graphical communica-
tion device, because of the significance of being able to draw directly
on its screen via a light pen, light buttons or physical switches.
The graphic terminal gives the user a picture and at the same time
permits him to select an area of the display and modify it or obtain
the attention of the computer for man and machine interaction.
Computer graphics has a large number of other uses besides its use
in engineering design, such as computer aided instruction, data
analysis, process control and as a teaching aid. These applications
can be grouped into two main areas, computer-aided design and command
and control systems.

II. Visual Computer Data Displays

There are three main categories of cathode ray tube displays,
alphanumeric, graphic and situation displays. The alphanumeric
display provides a formatted typewriter-like presentation. In graphic
display, lines may be presented along with randomly placed alphanumerics
and symbols. A situation display contains alphanumerics, symbols,
and lines, along with some form of background information.
Figure 1.1 Relationship between the Visual Display and Man-Machine System.

Figure 1.1 shows a typical display and its relationship to a man-machine system. The display contains signal processing circuits, computer communication devices, and a display readout device. Data are continually presented on the readout device under control of the computer. The display operator can alter the presentation by using the computer communication devices to send data via the signal processing circuits to the computer. In the computer, the communication device commands are processed and new data are sent to the display. These new computer data cause a new presentation on the readout device and the computer-display communication cycle can be repeated as often as necessary.
In the man-machine system of Figure 1.1, the display operator uses the display as a means for interacting with the computer. This interaction of display and computer involves both electronics and human factors. Human factors involves the physiological and psychological factors associated with the operation of the display system, the ability of the eye to respond to dynamically displayed data, the movements of the display operator as he performs his job, the layout of switches and readout devices on the panel of the display console, and the amount of data that an operator can assimilate.

III. Cathode Ray Tube Display System

![Diagram of Cathode Ray Tube Display System]

Figure 1.2 Cathode Ray Tube Display System.
Figure 1.2 shows the basic subsystems and devices which make up the signal processing circuit and communication device of a typical cathode ray tube computer data display.

Based on the research previously carried out in the Electrical Engineering Department of the University of Windsor, three main subsystems have been designed and installed. They are a digital controller and high speed refresh memory, an alphanumeric text generator, and a dot generator. The vector generator and intensity control circuit are dealt with in this thesis.

The vector generator would give the output terminal the capacity of drawing blank, solid or dashed lines of any length and at any angle on the cathode ray tube. This would then give the desirable ability to draw graphs, plots or other objects. With the aid of software, this generator could be made to draw circles and sectors.

In the output terminal, a Hewlett Packard X-Y display model 1300A is used. The intensity circuit would be designed to have the capability of representing characters at three different brightness levels, as well as having a blanked mode which will allow for the positioning of the beam, and to overcome the problem of inconsistent character and line intensification as the character size or length of vector varied. In the alphanumeric (A/N) mode, when small letters are drawn, they appear brighter than the normal size characters, due to the increased packing density of the dots; similarly, when large letters are drawn, due to decreased packing density of the dots they appear dull. In the vector mode, when longer lines are drawn, they appear duller than the shorter, due to the constant integration time.
Thus, compensating intensity levels have to be incorporated into the intensity selection circuits.

IV. Implementation

The circuitry which will be described in the remainder of this thesis was constructed from Digital Equipment Corporation (DEC) modules. The majority of the logic was implemented using Digital Equipment Corporation 'R' series logic modules which can operate up to a frequency of 2 MHz. These modules use negative NAND logic in which 0 volt represents a '0' state and -3 volts represents a '1' state. In the integration circuit, the operational amplifiers were made by Burr-Brown Research Corporation and the analog switches were DEC module A124.
CHAPTER 2
VECTOR GENERATOR

I. Introduction

Vector generators provide the signals required to produce vector presentation on a cathode ray tube. The vector generation signals can be obtained by a variety of methods employing either digital, analog, or a combination of both techniques.

When a vector generator is controlled by a computer, the data are usually transmitted to the display in one of two formats. In one format, the coordinates of the end points of the vector are specified. In the other format, the X and Y vector components of the line are specified. This vector component method was adopted in the data flow control system. In the vector generation circuitry itself, the length and direction of the X and Y vector components are used to generate the vector.

In the vector generation process, positive or negative slope, X and Y ramps of the same time duration are developed. The ramp signals are converted into a line on the cathode ray tube because of the 90-degree relationship between X and Y axes of the deflection subsystem. The length and direction of the vector are determined by the amplitude and polarity of the X and Y ramp signals. The length of the vector is proportional to \( \sqrt{\Delta x^2 + \Delta y^2} \), where \( \Delta x \) is the \( X \) vector component and \( \Delta y \) is the \( Y \) vector component of the line. The direction of the vector depends on the angle that the vector makes with the horizontal axis. This angle is equal to \( \tan^{-1}(\Delta y/\Delta x) \).

Since \( \Delta x \) or \( \Delta y \) can be either positive or negative, the direction of the
### Instruction Word

<table>
<thead>
<tr>
<th>Bit10</th>
<th>Bit11</th>
<th>Intensity</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>NORMAL</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>DIM</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>NO LIGHT</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>BLANKED</td>
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</tbody>
</table>

### Type:

<table>
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<tr>
<th>Bit7</th>
<th>Bit8</th>
<th>Vector Type</th>
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<td>0</td>
<td>0</td>
<td>POSITION</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>DOT POSITION</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>BASH LINE</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>SOLID LINE</td>
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### Int:

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<th>Intensity</th>
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<td>0</td>
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<td>NORMAL</td>
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<tr>
<td>0</td>
<td>1</td>
<td>DIM</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>NO LIGHT</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>BLANKED</td>
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### Data Word

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<th>10-Bit X Data</th>
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</thead>
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<td>0</td>
<td>0</td>
<td></td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Bit0</th>
<th>Bit1</th>
<th>10-Bit Y Data</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td></td>
</tr>
</tbody>
</table>

### Z:

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<th>Bit0</th>
<th>Override Option</th>
</tr>
</thead>
<tbody>
<tr>
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<td>NORMAL</td>
</tr>
<tr>
<td>1</td>
<td>BLANKED</td>
</tr>
</tbody>
</table>

---

**Figure 2.1 Instruction and Data Word Configuration**
vector depends on the polarity of the X and Y ramp signals.

For the vector component method, the computer must specify both the direction and length of the ΔX and ΔY components. One bit can be used to specify the direction of the X component and one bit can be used to specify the direction of the Y component. The length of the X and Y vector components can be specified by any number of bits, the greater the number of bits, the greater the accuracy of the generated vector. After a vector instruction is received, all the following output from the memory is considered data (ΔX and ΔY). This process of outputting data to the vector generator continues until a new instruction is encountered.

A 10-bit register was used for digital-to-analog (D/A) converter, there are 1024 distinct positions along each axis. A 8 x 10 -inch screen[5] was used, the raster unit being about 0.01 inch. The minimum increment of X and Y is thus 0.01 inch. The word formats are shown in Figure 2.1.

To draw a vector, the initial position data are received from the computer. Then, the ΔX and ΔY vector component data are received and the vector is generated by developing the proper ramp signals. While the vector is being generated the Z-axis is unblanked, producing a visible line on the cathode ray tube.

II. Digital Vector Generator with Rate Multiplier

This digital method of vector generator, (9) (10) shown in Figure 2.2, has a single D/A converter and counter for each X and Y vector generators, and two rate multiplier circuits have been used.

The operation of the rate multiplier can be best explained...
Figure 2.2 Digital Vector Generator Using Rate Multiplier.
by looking at a typical configuration. Figure 2.3 shows the logic circuit for one axis of a four bit rate multiplier, and in Figure 2.4 the timing diagram associated with the logic is shown. The logic notations are shown in Appendix 1.

The rate multiplier is used to control the number of clock pulses which drive the counter. The weighted gating signals in the timing diagram are labeled Bit 0, Bit 1, Bit 2, and Bit 3. The 4-bit counter clock is also shown in the diagram. During a 15-clock pulse period, either 1, 2, 4, or 8 clock pulses can be obtained from gating signals Bit 3, Bit 2, Bit 1, or Bit 0. For this period, from 0 to 15 clock pulses can be generated using a combination of gating signals. The control of the gating signals is obtained from control lines which are weighted in the same manner as the gating signals.

The control lines come from computer input data which have been processed by the input storage and decode logic. In the logic diagram Figure 2.3, NAND gate 1 to 4 accept the control line and gating signals. The output of these four gates are combined in NAND gate 5. The output of this NAND gate contains those gating signals that have been turned on by their associated control lines. When the output signal of NAND gate is ANDed with the counter clock, the counter will move the number of steps corresponding to the computer input data.

The rate multiplier can be extended to any number of stages by following the same pattern. That is, each lesser significant bit gating signal controls one-half as many clock pulses as the previous bit.

The output of the D/A converter may not consist of equal
Figure 2.5 Rate Multiplier Logic Circuit.
Figure 2.4 Counter Clock and Rate Multiplier Signals.
time increment steps since the gated clock pulse may not occur at equal time intervals. This is shown in Figure 2.5, where the D/A converter output has moved nine steps. The fact that the D/A output may result in an uneven series of steps is one of the drawbacks of the rate multiplier approach.

![Figure 2.5 Output of D/A Converter for 9 Counter Steps.](image)

For a generated vector, the X and Y staircases may not have the same number of steps, causing an irregular arrangement of dots. Figure 2.6 shows the cathode ray tube output for a vector generated with five X counts and nine Y counts. A large number of closely spaced dots may be necessary to provide a smooth line appearance with this approach.

The Z-axis gating signal for this approach is obtained from the clock pulse train. The gating signal should go to the '1' state slightly after the first clock pulse, and then '0' state after the last clock pulse. When done this way, every dot will be intensified during the vector generation time.

In Figure 2.6 it is easy to find out that the digital technique
generates a vector that only approximates the ideal straight line. This type of vector generator tends to be slow, since a series of counters are used. Since speed is important to the display system the analog technique has an advantage here. Therefore the analog vector generator is adopted in our display system. However, a certain amount of digital circuitry is required since the data output from the core memory is in digital form and must be converted into analog form by using D/A converters.

Figure 2.6 D/A Converter Staircases and Resulting Vector on Cathode Ray Tube
III. Analog Vector Generator

The analog vector generator, shown in Figure 2.7, employs an X and Y integrator to produce the required ramp signals. Figure 2.7 also shows the relationship between the data flow controller (2) and the vector generator which consists of a temporary X-register, X and Y registers, D/A converters, integration circuits, integration timing and control circuit, and intensity control circuit. The amplitude and direction of the ramp signals are controlled by the computer data. Each D/A converter receives the computer data via the input storage and the decode logic. The outputs of the D/A converters vary from 0 volts to -10 volts.

(1) Integration Circuit

Figure 2.8 shows the integration circuit which is used by the analog vector generators. (7) (10) It is built in duplicate, as separate circuits are needed for the X and Y deflection plates.

When the display system is not in the vector mode, the switch SW7 is closed and the others are opened. The analog outputs from the D/A converters bypass the integration circuit, directly going to the X and Y deflection plate amplifiers.

If a vector instruction is received, the switch SW6 is closed and SW7 will be opened. (The switch is closed if the control signal is -5 volts, '1' state, and the switch is opened if the control signal is 0 volts, '0' state.) As it was mentioned before, in the vector instruction word Bit 7 and 8 control the type of vector, shown in Figure 2.1. There are four different types, POSITION (POS), DOT POSITION (TIP), DASH LINE (DASH), and SOLID LINE (SOL).

For a POSITION of DOT POSITION instruction the switches SW2,
Figure 2.7 Block Diagram of Analog Vector Generation System.
Figure 2.8 Integration Circuit.
Figure 2.9 The Actual Circuit during POS or TIP Mode.
SW4, and SW5 are closed and the others are opened. The actual circuit is shown in Figure 2.9. The output of the integration circuit is as the same as the analog output of the D/A converter. Because of the same value in the resistors R1, R3, R6, and R7, the capacitor C will be charged up to the value of the analog output of the D/A converter. The integration circuit, in POS or TIP mode, acts as a position generator to set up the initial value of the integration.

When a DASH LINE or SOLID LINE instruction is encountered switch SW1 is closed and switches SW2, SW4, and SW5 are opened. Switch SW3 will be closed during the integration time of 100 µsec. The actual circuit is shown in Figure 2.10. The first operational amplifier A1 circuit is a summing network. Since the resistors R1, R2, and R3 are of the same value, the output of the network is equal to -(Vi + 5) volts. And Vi is the output of the D/A converter varying between 0 and -10 volts. Therefore the output (Vi + 5) will vary between +5 and -5 volts. It controls the direction of the ramp signals. The analog voltages represented in digital number based on octal is shown in Appendix 2. The second operational amplifier A2 circuit is an integrator. During the integration time switch SW5 will be closed and SW4 will be opened, the circuit begins integration of the input signal at the initial value Vc which is stored in the capacitor C. After 100 µsec the switch SW3 is opened to stop the integration, the switch SW5 is closed. The output of the integrator will hold its latest value (Vi + Vc + 5) volts. Figure 2.11 shows the truth table of the switches operation. During the time when the integrator is in operation, the beam of the cathode ray tube is being displayed on the screen. The beam is intensified to produce the
Figure 2.10 The Actual Circuit During DASH or SOL Mode
<table>
<thead>
<tr>
<th>MODE</th>
<th>DOT or A/N</th>
<th>VECTOR</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>POS</td>
<td>TIP</td>
</tr>
<tr>
<td>SW1</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>SW2</td>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>SW3</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>SW4</td>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>SW5</td>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>SW6</td>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>SW7</td>
<td>1</td>
<td>0</td>
</tr>
</tbody>
</table>

Note: 1 means switch is turned on.
      0 means switch is turned off.

Figure 2.11 Switch Operation.
(a) Output of X Integrator.

(b) Output of Y Integrator.

Figure 2.12 Outputs of the X and Y Integrators.
required vector. When a simple square is drawn, the outputs of X and Y integrators are shown in Figure 2.12.

(2) Integration Timing and Control Circuit

In Figure 2.7, the data controller (2) only generated Dot, A/N and Vector mode pulses, and load data pulses. There are several signals which need to be generated. The integration timing and control circuit is built for this purpose. It directs the loading of data into the temporary X register, X and Y D/A converter registers. It also controls the opening and closing of the switches in the analog integration circuit. The logic diagram is shown in Figure 2.13. (a) and (b).

The circuit can be divided into two parts, (a) is the timing controller which generates the signals to direct the data loading and decode the type of vector. The other (b) is the counter which consisting of a up-counter generates integration time of 100 μsec. Before the mode selection pulse (Dot mode, A/N mode, or Vector mode) is sent, a clear instruction pulse (CLI) is sent out by the core memory. It will clear all the flip-flops in the circuit, except the load data flip-flop (LDFF), initialize them to '0' state at the TRUE side of flip-flop. (In the remainder of this thesis, '0' or '1' state always means '0' or '1' state at the TRUE side of the flip-flop.) Since the vector mode flip-flop (VMFF) is in '0' state, the switch SW7 is closed and SW6 is opened, the integration circuit is ready for Dot or A/N mode display, and the analog outputs of the Dot or A/N mode display bypass the integrator, going directly to the X and Y axes of the cathode ray tube.

When a vector instruction is encountered, a set vector mode
Figure 2.13 (a) Logic Diagram of Integration Control.
Figure 2.13 (b) Logic Diagram of Integration Timing Circuit.
pulse (SW1) is sent in and set WMFP to '1' state and LDFF to '0' state. At the same time Bit 7 and Bit 8 of the display buffer register (DBR) is enabled to transmit into decoder flip-flops TYP1 and TYP2. There are four possible types of vectors to be generated.

Assuming POS or TIP instruction to be used, TYP1 is in '0' state. The switch SW1 is opened and PW (Position Mode) is -5 volts. Approximately 400 nano-seconds later a data ready pulse (DRP) is received and transmitted through NAND gate 1 to set the flag flip-flop (FFF) to '1' state. The input data flag (IDF) is in GROUND level, '0' state, indicating that no more data is required. The TRUE side of FFF is ANDed with B which is used by the override option. Usually, when the override option is not used B is in '0' state. Therefore the output of NAND gate 4 is in '1' state which enables the decoder to generate the signal for POS, TIP, DASH, or SOL display. The same pulse from NAND gate 2 is used to complement the LDFF and also is delayed until the LDFF has been set. Then this delayed pulse is transmitted through NAND gate 2 which is enabled by the LDFF to produce a pulse that loads the temporary X register and clears the FFF and the load initial condition flip-flop 2 (LIC2). Now IDF is in '1' state indicating that more data is required. The X and Y D/A converter registers and LIC1 are cleared by this same pulse which is further delayed until the temporary X register has been loaded.

About 8 μsec after FFF has been cleared a second DRP pulse is received. As well as before, this pulse sets the FFF to '1' state indicating that no more data is required, and complements the LDFF to enable the delayed pulse of DRP to transmit through NAND gate 3 to
pulse amplifier PA3 which produces a pulse used to load the X and Y D/A converter registers, to clear the temporary X register and set LIC1 to '1' state. Now the X and Y D/A converter registers are loaded with data via the display buffer register (DBR). These data are converted to analog voltages Vi by the D/A converters.

The TRUE side of LIC1 is ANDed with PM which indicates the type of vector to be POS or TIP since PM is in '1' state. Thus switch SW2 will be closed. The pulse, generated by the PA3, is delayed until X and Y D/A converter registers have been loaded. This delayed pulse sets LIC2 and integration flip-flop (IFF) to '1' state. The TRUE side of LIC2 is ANDed with PM to control the switch SW5.

Since the flip-flops of the counter are in '0' state and the output of NAND gate 13 is in '0' state the clock can not run, the switch SW3 is opened and SW4 is closed. This delayed pulse is further delayed and used to trigger NAND gate 9 and 10 in the vector type decoder. The signal TIP generated by NAND gate 9 is used for intensity control. The signal POS or TIP is also transmitted through an OR gate and delay unit to pulse amplifier PA6 to produce a pulse PC (Position Mode Complete) which is used to clear flip-flops FPF and IFF. Now a full cycle of POS or TIP instruction is completed. The circuit will continue in this cycle until a new instruction is sent in. The timing of pulses are shown in Figure 2.14. The first cycle is TIP and the second cycle is POS.

When the DASH or SOL instruction is encountered, the process of loading data into X and Y D/A converter registers is the same as during the POS or TIP instruction. But the flop-flop TYP1 is in '1' state, PM is in GROUND level. So the switches SW2 and SW5 will be
Figure 2.14 Timing Diagram of Pulses.
opened and switch SW1 will be closed. After the data have been loaded into the X and Y D/A converter registers they are converted into analog outputs Vix and Viy. Therefore the inputs to the X and Y integrators are (Vix + 5) and (Viy + 5) volts respectively.

The flip-flop IFF is in '1' state, IF enables the NAND gate 13. The clock starts to run sending out pulses at the rate of 230 K Hz approximately. The converted output of NAND gate 14 enables clock pulses to be transmitted to a 5 bit counter consisting of flip-flops FF1 to FF5. After the first count the output of NAND gate 15 turns the switch SW3 on and turns the switch SW4 off. Thus the integrators start integration. When the counter counts up to 24, the output of NAND gate 14 prohibits clock pulses from being transmitted to the counter and pulse amplifier PA7 produces a pulse to clear the flip-flops FF1 to FF5. Since the counter is pulsed at a rate of 230 K Hz, it takes approximately 104 nsec to complete its count. At the same time an integration complete pulse (IC) is generated by the NAND gate 16, indicating the integration is completed. This pulse clears the flip-flops IFF and PPP. Therefore the switch SW3 is closed approximately 100 nsec being the same as the time constant of the integrator. Now a full cycle of DASH or SOL instruction is accomplished. The same cycle will be generated next, unless a new instruction is received. Figure 2.15 shows the integration timing diagram.

Generally a vector is drawn by the following procedures. First a POS or TIP instruction is used. Then the X and Y data are sent to set the starting point from where the required vector is drawn. Second a SOL instruction is used and the X and Y components
Figure 2.15 Integration Timing Diagram.
are loaded. Then another POS or TIP instruction is used to terminate the integration. Now a required vector is drawn on the screen of the cathode ray tube.

Although the analog integrator is a linear device, its maximum rate of change of output signal can lead to slew rate distortion for signals of relatively high frequency and large amplitude. Another limitation usually much more restrictive, is that placed on the rate of change of capacitor voltage by the output current limits of the amplifier. The time required for the amplifier to reset to initial conditions is limited by the RC time constant.
CHAPTER 3

THE INTENSITY CIRCUIT

I. Introduction

The presentation of data on a cathode ray tube is accomplished by controlling the electron beam in three axes. Control of the deflection of the electron beam is achieved in the X and Y axes of the cathode ray tube. Control of the intensity of the electron beam is achieved in the Z axes. There are two methods used to control the brightness on the screen of a cathode ray tube.

One method is the pulse width modulation. The pulse amplitude is kept constant, and the pulse width is varied. When the pulse width is wider the intensity of the display becomes brighter. This method can only be used in a relatively slow rate of changing in control signals. The A/N generator constructed at the Electrical Engineering Department operates at a frequency of 2 mega-Hz. The period of each control signal is 500 nano-seconds, and the D/A converters which are used in the display system need about 300 nano-seconds to settle to their final values. Therefore only 200 nano-seconds is left for the pulse width modulation. Thus the pulse width is not wide enough to generate three distinct intensity levels. This method is impossible to be used in the intensity circuit design.

The second method is pulse amplitude modulation. The pulse width is kept constant, and the pulse amplitude is varied. It was mentioned, the pulse width is limited by the A/N generator. While keeping the pulse width constant, the pulse amplitude can be set to one of three distinct voltages. When the pulse amplitude increases,
the intensity increases. It is the method used in the intensity circuit design.

II. Intensity Generation

(1) DOT POSITION Intensity Generation

During TIP mode a bright dot is required to show on the screen of the cathode ray tube. After the digital data have been loaded into the X and Y D/A converter registers and converted into analog voltages they are passed to the X and Y axes of the cathode ray tube. A pulse (TIP) is generated by NAND gate 9, shown in Figure 2.13. This pulse is sent to a pulse amplifier for standardizing the pulse in amplitude and width. A 100 nano-seconds pulse is produced. A delay unit is used to control the pulse width which can be widened up to a desirable brightness of the dot. Figure 3.1 illustrates the configuration of the TIP (DOT POSITION) intensity generation. The output (TINT) of the circuit will be sent to the intensity control circuit for the purpose of generating four different intensity levels.

(2) Vector Intensity Generation

Since the integration time is constant, 100 micro-seconds, an intensity pulse with 100 micro-seconds width should be generated during the integration. To generate a constant amplitude pulse with 100 micro-seconds width is easier to achieve. But the problem is that when different lengths of the lines are drawn the brightness of the lines are different. A shorter line is brighter than a longer one, so that pulse amplitude modulation is used. The output of the switch SW3, shown in Figure 2.8, is used. There are two reasons for choosing
Figure 3.1 TIP Intensity Generation.

Figure 3.2 Vector Intensity Generation.
the output of switch SW3. First, it gives a pulse with 100 microseconds width and varied amplitude between +5 and -5 volts. Second, the amplitudes of the pulse are equal to the X and Y components of a vector. If the X and Y components increase, the length of the vector increases. So the relationship, between the X and Y components and the length of a vector, is as same as the relationship between the amplitude of the intensity pulse with constant width and the length of the line drawn on the screen. When a longer line is drawn the pulse amplitude needs to increase to keep a consistant brightness on the screen.

The value of the output from switch SW3 varies between +5 and -5 volts. Because the control signal for Z axis is negative. Two absolute value circuits, one for X and one for Y illustrated in Figure 3.2, are used to invert the positive outputs into the negative values with same magnitude. The inputs XINT and YINT are from the X and Y integration circuits respectively. The negative output VINT, in magnitude, is equal to the sum of the absolute values XINT and YINT. When the X and Y components of a vector increase the value of VINT increases. In other words, when the length of a vector increases the pulse amplitude increases. So the intensity of the lines is compensated automatically by the circuit. A consistant brightness display will be achieved.

In Figure 3.5, the pictures show the results of the circuit. Figure 3.3 (a) represents the different length of lines with consistant brightness on the screen. In Figure 3.3 (b), the lower signal shows the different amplitude of intensity pulses, the upper signal is the associated ramp signals during integration. When the ramp signal
(a) Different Length of Vectors with Consistant Brightness.

(b) The Intensity Pulses and Associated Ramp Signals.

Figure 5.3 Vector Intensity Generation.
Figure 3.4 Light Output vs Input Voltage (5)
increases the amplitude of the intensity pulse increases.

III. Intensity Control Circuit

Hewlett Packard Model 1300A X - Y Display is a wild-band, large screen oscilloscope. (5) A 20 mega-Hz band width Z-axis amplifier gives full trace intensity with -1 volt input, and complete blanding is obtained with +1 volt input. Maximum input is ± 500 volts (dc + peak ac). A vernier gives 2.5 : 1 reduction. Figure 3.4(5) is a plot of the intensity response of the Model 1300A to an analog signal at the Z-axis input. It is relatively easy to generate such low amplitude intensity pulse.

The intensity generated by the intensity generation circuits shown in Figure 3.1 and Figure 3.2 gives only one intensity level. There are four distinct intensity levels required to be produced. In order to achieve this requirement a preset voltage divider is used. In Figure 3.5, the lower part of the circuit is the divider which generates three distinct voltage levels, dim, normal, and bright, controlled by the switches, SW1, SW2, and SW3 respectively. The logic diagram for the switches control is illustrates in Figure 3.6. When one of the display instructions is sent in, the flip-flops INT1 and INT2 are cleared by CLI pulse. Then a SVM pulse, or SAM (set A/N mode), or SDM (set dot mode), according to which instruction is being used, enables the instruction word Bit10 and Bit11 to transmit into flip-flops INT1 and INT2 from the display buffer register, and is decoded to produce the proper signal. This signal turns on the proper switch. Thus a certain brightness level specified by the instruction word will be obtained. The switch SW4 is only closed during the period of integration. So a blanked vector is generated by prohibiting the
Figure 3.5 Intensity Control Circuit.
<table>
<thead>
<tr>
<th>INTENSITY LEVEL</th>
<th>DBR Bit10</th>
<th>Bit11</th>
</tr>
</thead>
<tbody>
<tr>
<td>NORMAL</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>DIM</td>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>BRIGHT</td>
<td>1</td>
<td>0</td>
</tr>
<tr>
<td>BLANKED</td>
<td>1</td>
<td>1</td>
</tr>
</tbody>
</table>

Figure 3.6 Logic Diagram for Intensity Levels.
<table>
<thead>
<tr>
<th>CHARACTER SIZE</th>
<th>DBR Bit2</th>
<th>DBR Bit3</th>
</tr>
</thead>
<tbody>
<tr>
<td>NORMAL</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>CAPITAL</td>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>SUBSCRIPT</td>
<td>1</td>
<td>0</td>
</tr>
<tr>
<td>SUPERSCRIPT</td>
<td>1</td>
<td>1</td>
</tr>
</tbody>
</table>

Figure 3.7 Character Intensity Control.
signal transmitted through NAND gate 5 to turn the switch SW4 on.

The problem introduced during the A/N mode is the inconsistent brightness of different sizes of characters due to the packing density of the dots. The upper part of the circuit in Figure 3.5 is designed to solve the problem. The voltage divider creates three distinct positive potential for small size, normal size, and capital size characters. They are controlled by the switches SW5, SW6, and SW7. The associated logic diagram is shown in Figure 3.7. Each time when a character is sent in, the Bit2 and Bit3 of the display buffer register is also transmitted into the flip-flops CS1 and CS2, then decoded to generate the proper signal to turn on the corresponding switch. For instance, a capital size character is written on the screen, the Bit2 and Bit3 are transmitted into CS1 and CS2 enabled by TELP. AM (A/N mode) is in '1' state. So the switch SW7 is closed.

This causes the dots composing the letter to be brighter than normal, thus compensating for the fact that the dots are spread further apart than normal. The truth table for the switches is shown in Figure 3.8.

The dots which are generated during Dot mode or TIP mode are treated as bright as normal size character. The switch SW6 is closed when the Dot or TIP instruction is used.

The last feature of the intensity circuit remains to be mentioned. This is the intensity override option which is available only when the vector generator is used. This option allows one to position a blanked starting point from where a vector will be drawn. This option is incorporated for the convenience of the programmer, as it allows the operator to draw any vector from a new starting point without giving a new instruction. This feature saves core
<table>
<thead>
<tr>
<th>SWITCH</th>
<th>VECTOR</th>
<th>DOT</th>
<th>A/N</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>TIP</td>
<td>SOL</td>
<td>SMALL</td>
</tr>
<tr>
<td>SW4</td>
<td>0</td>
<td>1</td>
<td>0</td>
</tr>
<tr>
<td>SW5</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>SW6</td>
<td>1</td>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>SW7</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
</tbody>
</table>

Figure 3.8 The Truth Table of Switches.

Figure 3.9 The Override Option.
space. Bit1 of the second data word for the vector generator controls
the use of this option. The control flip-flop ZFF is shown in Figure
3.9. After the first datum has been loaded in the temporary X register,
the ZFF is cleared by LDTX pulse generated by the integration control
circuit. At the same time when the second datum is loaded in Y D/A
converter register, Bit1 is loaded in ZFF which sets B into '1' state.
B is ANDed with RZ and makes the outputs of NAND gate 5 and 6 in the
integration control circuit go to the '1' state regardless of what
type of vector which is indicated in the instruction word. B also
enables the switches SW2 and SW5 in the integration circuit to close.
So a full cycle of POS is accomplished.

The results are shown in Figure 3.10. Figure 3.10 (a) shows
the three sizes of characters on the screen before compensation. Due
to the packing density the small size looks brighter than the others.
A consistant brightness picture of characters controlled by the in-
tensity circuit is shown in Figure 3.10 (b). Figure 3.11 represents
the three distinct brightness levels controlled by intensity circuit.
Figure 3.10  A consistent Brightness of Characters.
Figure 3.11 Three Distinct Brightness Levels.
CHAPTER 4
CONCLUSIONS

I. Vector Generator

The integration timing and control circuit was tested and found to operate as expected. It directed the process of loading data into the temporary X register, X and Y D/A converter registers and controlled the opening and closing of the switches in the integration circuit.

The integration circuit was tested. Any vector can be drawn in any position of the screen. Figure 4.1 shows the outputs of the vector generator on the screen of the Hewlett Packard model 1300A X-Y display, and consists of several vectors. The associated X and Y analog outputs are represented in Figure 4.2. The vector generator has been shown capable of generating lines with reasonable success. In Figure 4.1 mismatch however does occur at the vertices. For one-inch length the mismatch is about 1/64 inches, or 1.5 percent. The angle between two parallel lines is 1.5 degrees. This problem may be improved by using better analog switches and/or operational amplifiers which would probably be more costly. This should be compared with the research\(^{(4)}\) previously carried out in the Electrical Engineering Department in which the equipment proved unable to generate any satisfactory lines. Furthermore the integration circuit here uses only two operational amplifiers and thus the circuitry is simpler than the previous design which required four operational amplifiers. The new design is much lower in cost. However the result is not as good as systems recently built by computer manufacturers. Examples of such systems are the Digital Equipment Corporation DEC-340 and IBM 2250.\(^{(13)}\)
Figure 4.1 The Output of Vector Generator.
(a) X Analog Output of the Vector Generator.

(b) Y Analog Output of the Vector Generator.

Figure 4.2 The Analog Outputs of the Vector Generator.
II. Intensity Circuit

The intensity circuit was tested and found to operate properly. That is, when the instructions are given to select Dim, Normal, Bright, or blanked intensities, the appropriate circuit is initiated. Also when the A/N generator is being used, the compensation circuits are selected as expected. A consistent brightness picture is obtained on the screen of the cathode ray tube. As is shown in Figure 5.10.

Solid line and Dot position are successfully displayed on the cathode ray tube, shown in Figure 5.3, thus indicating that the vector intensification circuits are operating properly. The override option was also tested and found to operate as expected. Whenever Bit1 of the Y coordinate data word is a '1', the integration circuit is in POS mode, no matter what instruction has been given. Any point can be positioned on the screen. And whenever the bit is a '0', the decoder of integration timing and control circuit has the control of the type of vector.

The intensity pulses for Dash lines could be produced by using the output of flip-flop FF1 of the up-counter in the integration timing and control circuit, to operate the switch SW4 in the intensity control circuit. By using the output of the counter as trigger pulses, the switch SW4 is repeatedly closed for a period of time, and then opened for the same period of time, thus creating a Dash line. But this method generates the Dash lines with different length of dash. When a longer vector is drawn, the length of dash appears longer than the short. When a short vector is drawn, the Dash line may become a dot line; this is because any length of vector is divided into the
same number of line segments and this feature was not further considered.

It is therefore concluded that the intensity circuit was constructed successfully.
APPENDIX I

LOGIC NOTATION

(1) Preferred Pulse Input:
   Positive Pulse →
   Negative Pulse →

(2) Preferred Level Input:
   Positive Level →
   Negative Level →

(3) Interconnections:
   Input →
   Output →

(4) NAND Gate:

(5) OR Gate:

(6) Inverter:

(7) Pulse Amplifier:

(8) DCD Gate:
   PULSE INPUT → LEVEL INPUT
   OUTPUT
   Level must be present at least 400 nsec before gate is pulsed.

This gate acts as an AND gate. It provides a logical delay.
which is essential for sampling flip-flops at the time they are changing.

(9) Flip-flop:

![Flip-flop diagram]

(10) Delay:

![Delay diagram]

(11) Clock:

![Clock diagram]

A is an enable level which allows the clock to operate.

Output is a series of 100 nsec pulses, the frequency of which may be varied.

(12) Switch:

When the control signal is GROUND level the switch is opened.

When the control signal is held at -3 volts the switch is closed.
# APPENDIX II

## BINARY CODED INTEGRATOR

## OUTPUTS

<table>
<thead>
<tr>
<th>OCTAL NUMBERS</th>
<th>D/A CONVERTER OUTPUTS</th>
<th>VECTOR GENERATOR OUTPUTS</th>
</tr>
</thead>
<tbody>
<tr>
<td>0000</td>
<td>0 volt</td>
<td>+5 volts</td>
</tr>
<tr>
<td>0500</td>
<td>-2.5 volts</td>
<td>+2.5 volts</td>
</tr>
<tr>
<td>1000</td>
<td>-5 volts</td>
<td>0 volt</td>
</tr>
<tr>
<td>1500</td>
<td>-7.5 volts</td>
<td>-2.5 volts</td>
</tr>
<tr>
<td>1777</td>
<td>-10 volts</td>
<td>-5 volts</td>
</tr>
</tbody>
</table>
REFERENCES


(2) Murray, B. L.; A Data Flow Controller and Refresh Memory for a computer Display System, a thesis submitted to the Department of Electrical Engineering at the University of Windsor (1970).


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